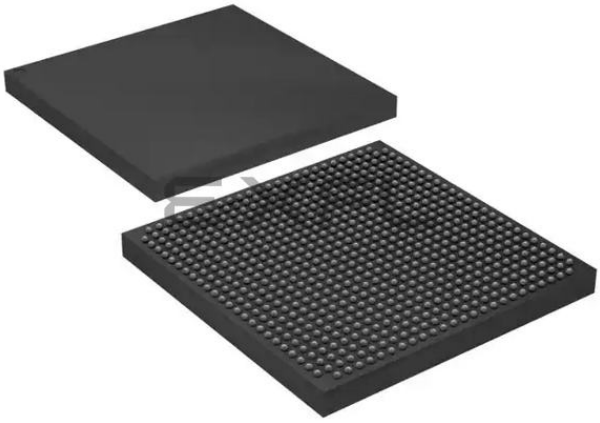

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	492
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s60f672c3n

Visual Cue	Meaning
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>*.**pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
WARNING	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Stratix II devices are available in space-saving FineLine BGA® packages (see Tables 1–2 and 1–3).

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 *(3)*	334		492		718	
EP2S90 *(3)*		308		534	758	902
EP2S130 *(3)*				534	742	1,126
EP2S180 *(3)*					742	1,170

Notes to Table 1–2:

(1) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(2) The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not available as general-purpose I/O pins. The `PLL_ENA` pin can only be used to enable the PLLs within the device.

(3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

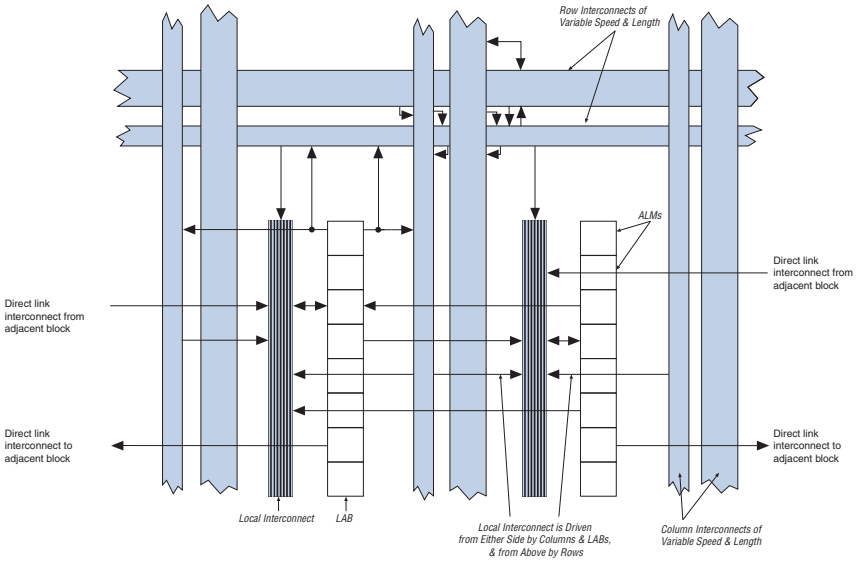
Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm2)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

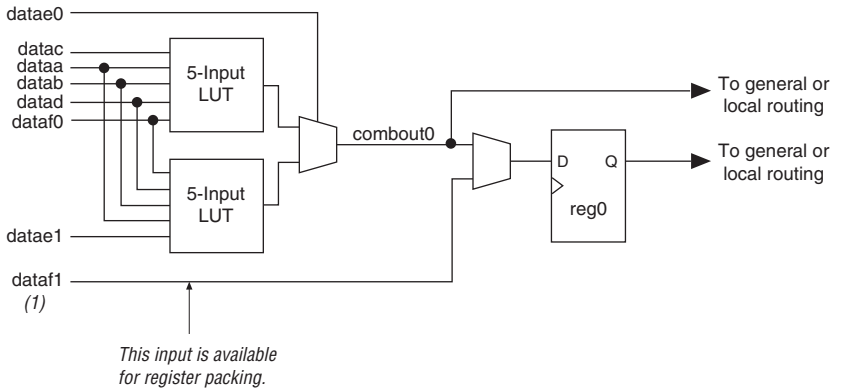
Figure 2–2. Stratix II LAB Structure



LAB Interconnects

The LAB local interconnect can drive ALMs in the same LAB. It is driven by column and row interconnects and ALM outputs in the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, M-RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each ALM can drive 24 ALMs through fast local and direct link interconnects. Figure 2–3 shows the direct link connection.

Figure 2–10. Template for Supported Seven-Input Functions in Extended LUT Mode



Note to Figure 2–10:

(1) If the seven-input function is unregistered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of two four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–11, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or unregistered versions of the adder outputs.

Table 2–5 shows the number of DSP blocks in each Stratix II device.

Table 2–5. DSP Blocks in Stratix II Devices *Note (1)*

Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP2S15	12	96	48	12
EP2S30	16	128	64	16
EP2S60	36	288	144	36
EP2S90	48	384	192	48
EP2S130	63	504	252	63
EP2S180	96	768	384	96

Note to Table 2–5:

(1) Each device has either the numbers of 9 × 9-, 18 × 18-, or 36 × 36-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block depending on the configuration. This makes routing to ALMs easier, saves ALM routing resources, and increases performance, because all connections and blocks are in the DSP block. Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications, and DSP blocks support Q1.15 format rounding and saturation.

Figure 2–28 shows the top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

Figure 2–28. DSP Block Diagram for 18 × 18-Bit Configuration

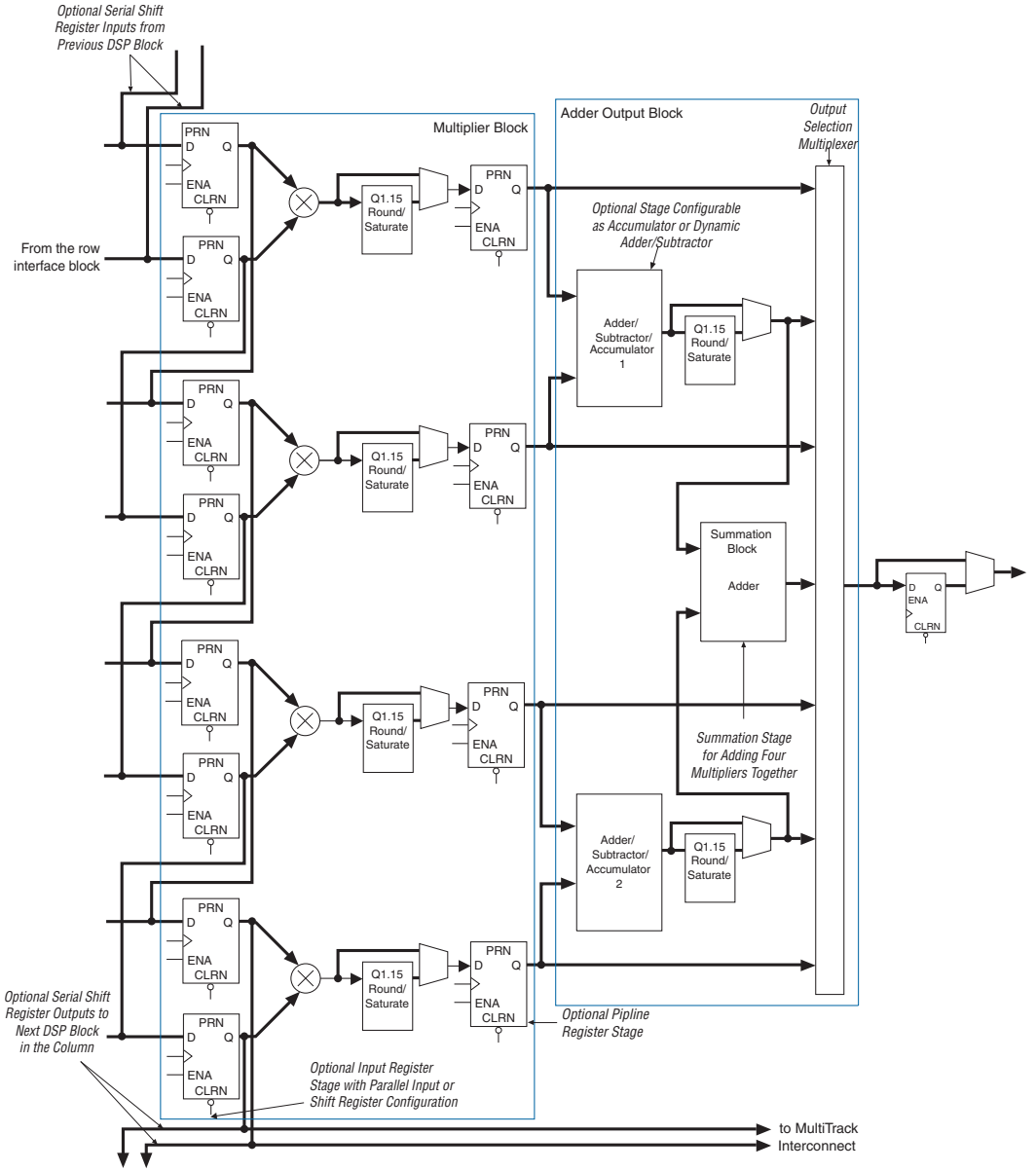
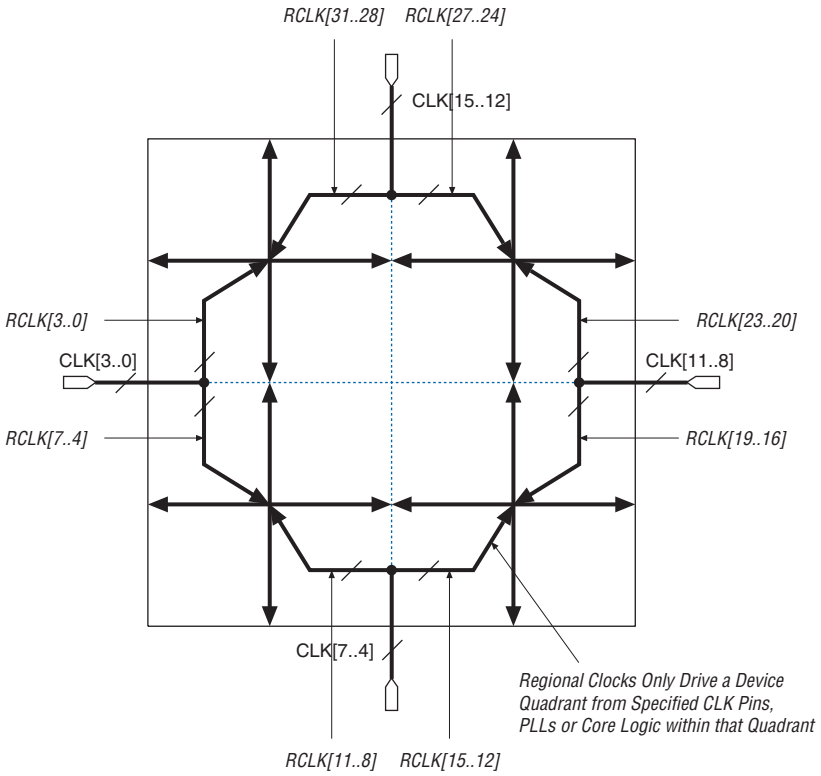


Figure 2–32. Regional Clocks

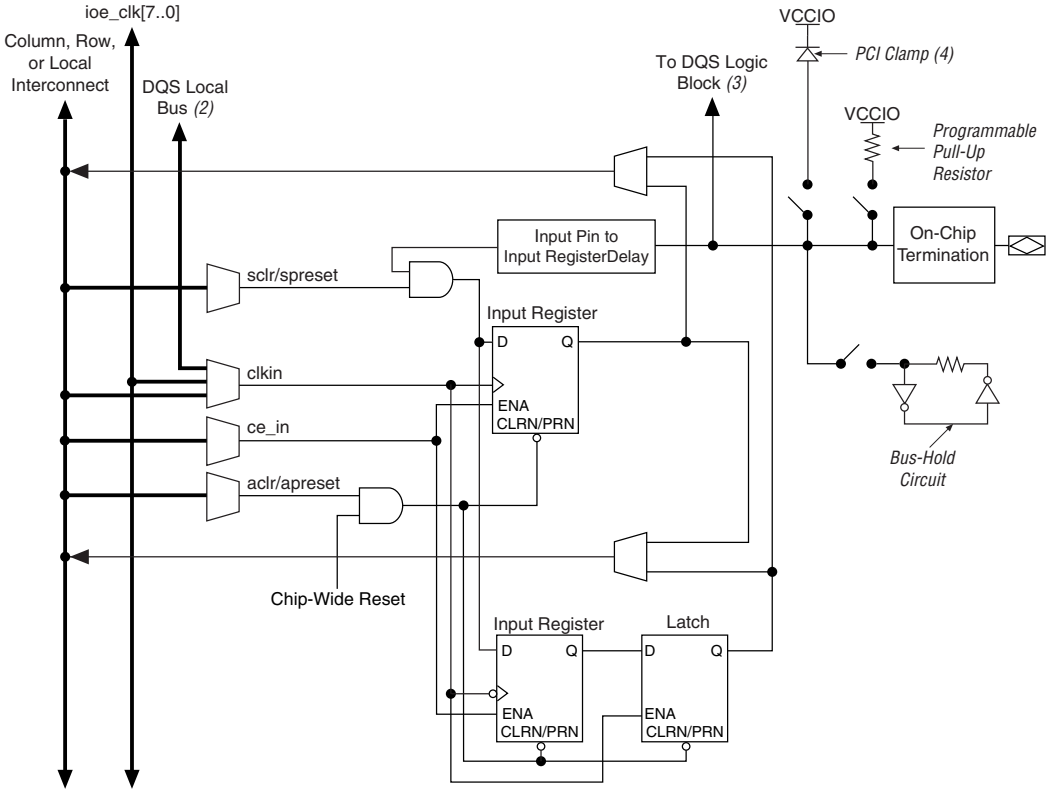


Dual-Regional Clock Network

A single source (CLK pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines in adjacent quadrants (one from each quadrant). This allows logic that spans multiple quadrants to utilize the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in Figure 2–33. Corner PLLs cannot drive dual-regional clocks.

When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–52 shows an IOE configured for DDR input. Figure 2–53 shows the DDR input timing diagram.

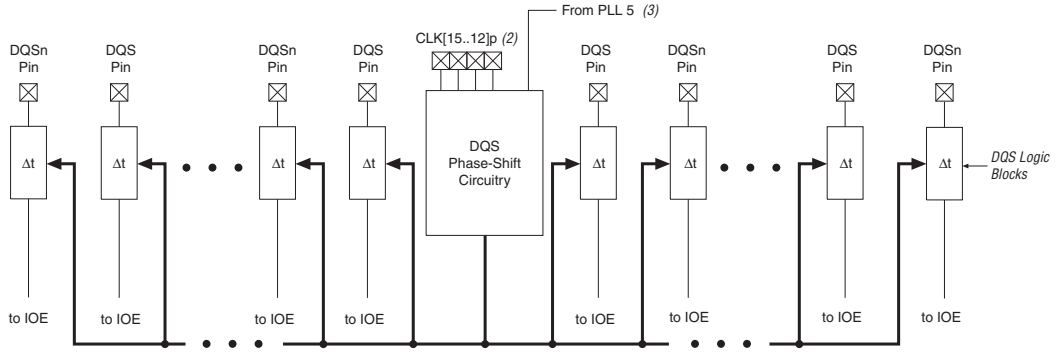
Figure 2–52. Stratix II IOE in DDR Input I/O Configuration *Notes (1), (2), (3)*



Notes to Figure 2–52:

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.
(4) The optional PCI clamp is only available on column I/O pins.

Figure 2–56. DQS Phase-Shift Circuitry *Notes (1), (2), (3), (4)*



Notes to Figure 2–56:

(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The Δt module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phase-shift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

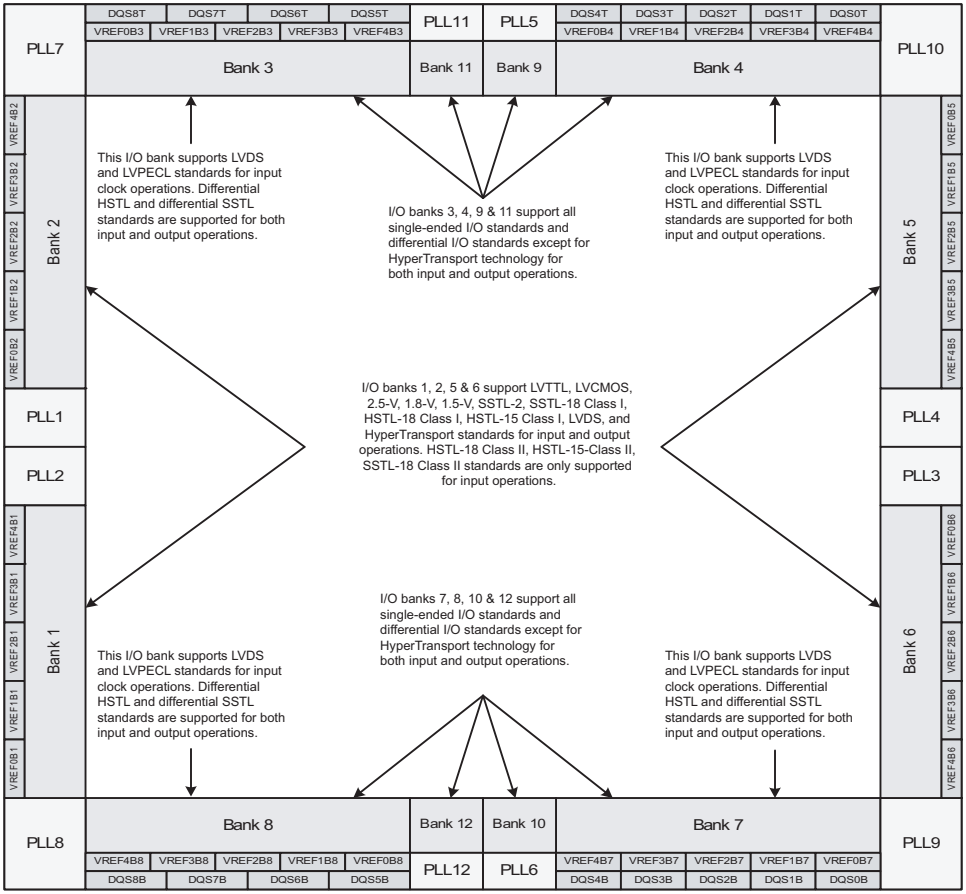
These dedicated circuits combined with enhanced PLL clocking and phase-shift ability provide a complete hardware solution for interfacing to high-speed memory.

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Programmable Drive Strength

The output buffer for each Stratix II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that the user can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Figure 2–57. Stratix II I/O Banks *Notes (1), (2), (3), (4)*



Notes to Figure 2–57:

(1) Figure 2–57 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

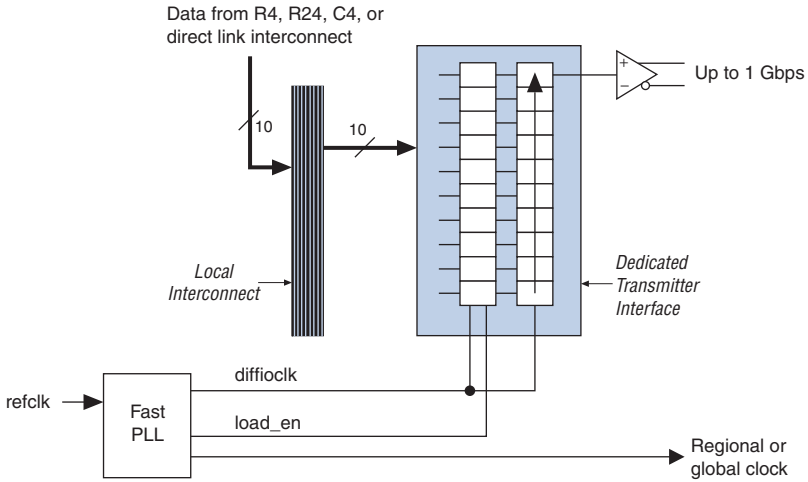
(3) Banks 9 through 12 are enhanced PLL external clock output banks. These PLL banks utilize the adjacent V_{REF} group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at VREFB7 is the reference voltage level for the SSTL input.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high speed differential I/O standards. See the *High Speed Differential I/O Interfaces in Stratix II & Stratix II GX Devices* chapter of the *Stratix II Device Handbook, Volume 2* or the *Stratix II GX Device Handbook, Volume 2* for more information on differential I/O standards.

Dedicated Circuitry with DPA Support

Stratix II devices support source-synchronous interfacing with LVDS or HyperTransport signaling at up to 1 Gbps. Stratix II devices can transmit or receive serial channels along with a low-speed or high-speed clock. The receiving device PLL multiplies the clock by an integer factor W = 1 through 32. For example, a HyperTransport technology application where the data rate is 1,000 Mbps and the clock rate is 500 MHz would require that W be set to 2. The SERDES factor *J* determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor *J* can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these *J* factor values. For a *J* factor of 1, the Stratix II device bypasses the SERDES block. For a *J* factor of 2, the Stratix II device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. Figure 2–58 shows the block diagram of the Stratix II transmitter channel.

Figure 2–58. Stratix II Transmitter Channel

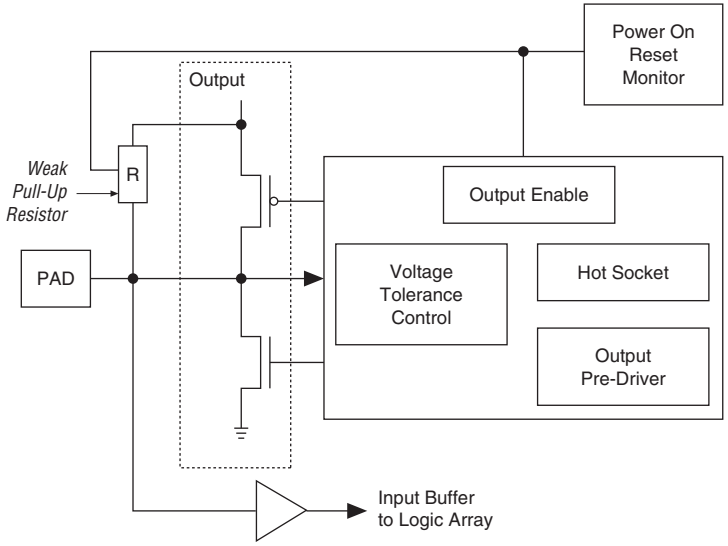


Each Stratix II receiver channel features a DPA block for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel. In addition, you can dynamically switch between using the DPA block or bypassing the block via a control signal from the logic array. Figure 2–59 shows the block diagram of the Stratix II receiver channel.

Table 3–7. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
April 2006, v4.1	Updated "Device Security Using Configuration Bitstream Encryption" section.	—
December 2005, v4.0	Updated "Software Interface" section.	—
May 2005, v3.0	• Updated "IEEE Std. 1149.1 JTAG Boundary-Scan Support" section. • Updated "Operating Modes" section.	—
January 2005, v2.1	Updated JTAG chain device limits.	—
January 2005, v2.0	Updated Table 3–3.	—
July 2004, v1.1	• Added "Automated Single Event Upset (SEU) Detection" section. • Updated "Device Security Using Configuration Bitstream Encryption" section. • Updated Figure 3–2.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Figure 4–1. Hot Socketing Circuit Block Diagram for Stratix II Devices



The POR circuit monitors V_{CCINT} voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is present to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} and/or V_{CCPD} are powered, and it prevents the I/O pins from driving out when the device is not in user mode. The hot socket circuit prevents I/O pins from internally powering V_{CCIO}, V_{CCINT}, and V_{CCPD} when driven by external signals before the device is powered.

Figure 4–2 shows a transistor level cross section of the Stratix II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. There is no current path from signal I/O pins to V_{CCINT} or V_{CCIO} or V_{CCPD} during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

Table 5–14. 3.3-V PCI Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low-level input voltage		–0.3		$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–15. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.30		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–16. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		$V_{REF} – 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.125$			V
V_{IL} (DC)	Low-level DC input voltage				$V_{REF} – 0.125$	V
V_{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.25$			V
V_{IL} (AC)	Low-level AC input voltage				$V_{REF} – 0.25$	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	$V_{TT} + 0.475$			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			$V_{TT} – 0.475$	V

Note to Table 5–16:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–23. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 5–23:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–24. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 5–24:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–39. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade *(1)*		-3 Speed Grade *(2)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min *(3)*	Max	Min *(3)*	Max	Min *(4)*	Max	Min *(3)*	Max	
t_{SU}	Input, pipeline, and output register setup time before clock	50		52		57 57		67		ps
t_{H}	Input, pipeline, and output register hold time after clock	180		189		206 206		241		ps
t_{CO}	Input, pipeline, and output register clock-to-output delay	0	0	0	0	0 0	0	0	0	ps
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode	1,312	2,030	1,312	2,030	1,250 1,312	2,334	1,312	2,720	ps
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode	1,302	2,010	1,302	2,110	1,240 1,302	2,311	1,302	2,693	ps
$t_{INREG2PIPE36}$	Input register to DSP block pipeline register in 36 × 36-bit mode	1,302	2,010	1,302	2,110	1,240 1,302	2,311	1,302	2,693	ps
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode	924	1,450	924	1,522	880 924	1,667	924	1,943	ps
$t_{PIPE2OUTREG4ADD}$	DSP block pipeline register to output register delay in four-multipliers adder mode	1,134	1,850	1,134	1,942	1,080 1,134	2,127	1,134	2,479	ps
t_{PD9}	Combinational input to output delay for 9 × 9	2,100	2,880	2,100	3,024	2,000 2,100	3,312	2,100	3,859	ps
t_{PD18}	Combinational input to output delay for 18 × 18	2,110	2,990	2,110	3,139	2,010 2,110	3,438	2,110	4,006	ps
t_{PD36}	Combinational input to output delay for 36 × 36	2,939	4,450	2,939	4,672	2,800 2,939	5,117	2,939	5,962	ps
t_{CLR}	Minimum clear pulse width	2,212		2,322		2,543 2,543		2,964		ps

Table 5–76. Stratix II I/O Output Delay for Row Pins (Part 3 of 3)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
1.8-V HSTL Class I	4 mA	t_{OP}	972	1019	1610	1689	1850	1956	ps
		t_{DIP}	930	976	1555	1632	1787	1883	ps
	6 mA	t_{OP}	975	1022	1580	1658	1816	1920	ps
		t_{DIP}	933	979	1525	1601	1753	1847	ps
	8 mA	t_{OP}	958	1004	1576	1653	1811	1916	ps
		t_{DIP}	916	961	1521	1596	1748	1843	ps
	10 mA	t_{OP}	962	1008	1567	1644	1801	1905	ps
		t_{DIP}	920	965	1512	1587	1738	1832	ps
	12 mA (1)	t_{OP}	953	999	1566	1643	1800	1904	ps
		t_{DIP}	911	956	1511	1586	1737	1831	ps
1.5-V HSTL Class I	4 mA	t_{OP}	970	1018	1591	1669	1828	1933	ps
		t_{DIP}	928	975	1536	1612	1765	1860	ps
	6 mA	t_{OP}	974	1021	1579	1657	1815	1919	ps
		t_{DIP}	932	978	1524	1600	1752	1846	ps
	8 mA (1)	t_{OP}	960	1006	1572	1649	1807	1911	ps
		t_{DIP}	918	963	1517	1592	1744	1838	ps
LVDS		t_{OP}	1018	1067	1723	1808	1980	2089	ps
		t_{DIP}	976	1024	1668	1751	1917	2016	ps
HyperTransport		t_{OP}	1005	1053	1723	1808	1980	2089	ps
		t_{DIP}	963	1010	1668	1751	1917	2016	ps

Notes to Table 5–76:
(1) This is the default setting in the Quartus II software.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Maximum Input & Output Clock Toggle Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

Table 5–80. Maximum DCD for Non-DDIO Output on Row I/O Pins (Part 2 of 2) *Note (1)*

Row I/O Output Standard	Maximum DCD for Non-DDIO Output		
	-3 Devices	-4 & -5 Devices	Unit
1.8 V	180	180	ps
1.5-V LVCMOS	165	195	ps
SSTL-2 Class I	115	145	ps
SSTL-2 Class II	95	125	ps
SSTL-18 Class I	55	85	ps
1.8-V HSTL Class I	80	100	ps
1.5-V HSTL Class I	85	115	ps
LVDS/ HyperTransport technology	55	80	ps

Note to Table 5–80:
(1) The DCD specification is based on a no logic array noise condition.

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 5–80). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3745 ps

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3745ps/2 – 95ps) / 3745ps = 47.5% (for low boundary)

(T/2 + DCD) / T = (3745ps/2 + 95ps) / 3745ps = 52.5% (for high boundary)

PLL Timing Specifications

Tables 5–92 and 5–93 describe the Stratix II PLL specifications when operating in both the commercial junction temperature range (0 to 85 °C) and the industrial junction temperature range (–40 to 100 °C).

Table 5–92. Enhanced PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	2		500	MHz
f_{INPFD}	Input frequency to the PFD	2		420	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback input clock duty cycle	40		60	%
$t_{INJITTER}$	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth ≤ 0.85 MHz		0.5		ns (p-p)
	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth > 0.85 MHz		1.0		ns (p-p)
$t_{OUTJITTER}$	Dedicated clock output period jitter			250 ps for ≥ 100 MHz `outclk` 25 mUI for < 100 MHz `outclk`	ps or mUI (p-p)
t_{FCOMP}	External feedback compensation time			10	ns
f_{OUT}	Output frequency for internal global or regional clock	1.5 *(2)*		550.0	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%).	45	50	55	%
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for enhanced PLLs		$174/f_{SCANCLK}$		ns
f_{OUT_EXT}	PLL external clock output frequency	1.5 *(2)*		550.0 *(1)*	MHz

Table 5–100. DQS Phase Offset Delay Per Stage Notes (1), (2), (3)			
Speed Grade	**Min**	**Max**	**Unit**
-3	9	14	ps
-4	9	14	ps
-5	9	15	ps

Notes to Table 5–100:
(1) The delay settings are linear.
(2) The valid settings for phase offset are -64 to +63 for frequency mode 0 and -32 to +31 for frequency modes 1, 2, and 3.
(3) The typical value equals the average of the minimum and maximum values.

Table 5–101. DDIO Outputs Half-Period Jitter Notes (1), (2)			
Name	**Description**	**Max**	**Unit**
$t_{OUTHALFJITTER}$	Half-period jitter (PLL driving DDIO outputs)	200	ps

Notes to Table 5–101:
(1) The worst-case half period is equal to the ideal half period subtracted by the DCD and half-period jitter values.
(2) The half-period jitter was characterized using a PLL driving DDIO outputs.

JTAG Timing Specifications

Figure 5–10 shows the timing requirements for the JTAG signals.

Figure 5–10. Stratix II JTAG Waveforms