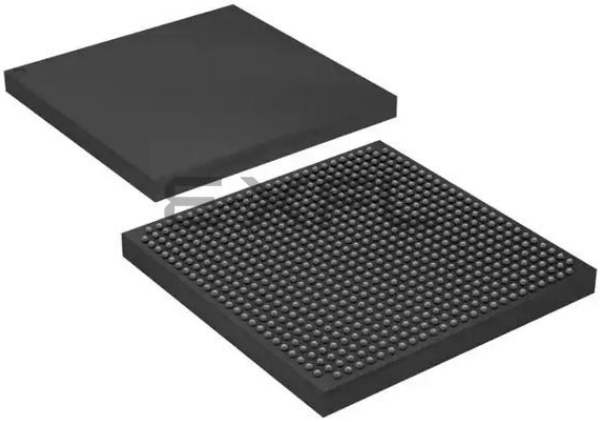


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	492
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s60f672c4n

One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see Figure 2–6). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

See the *Performance & Logic Efficiency Analysis of Stratix II Devices White Paper* for more information on the efficiencies of the Stratix II ALM and comparisons with previous architectures.

ALM Operating Modes

The Stratix II ALM can operate in one of the following modes:

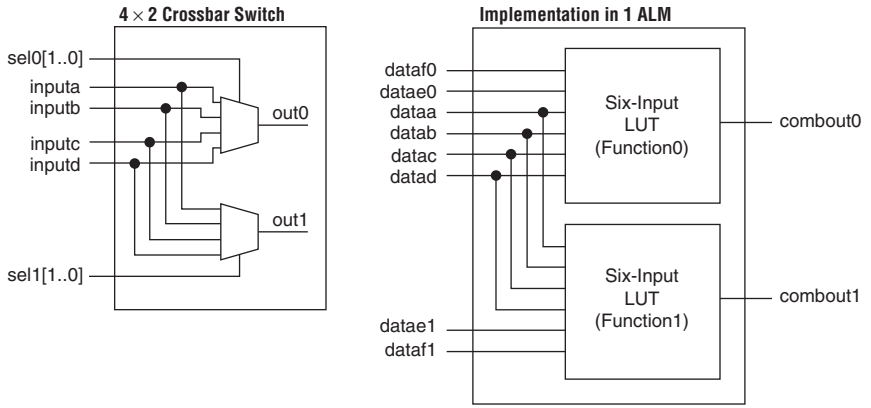
- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. In each mode, eleven available inputs to the ALM--the eight data inputs from the LAB local interconnect; `carry-in` from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection--are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear,

For the packing of two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

In the case of implementing two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–8. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

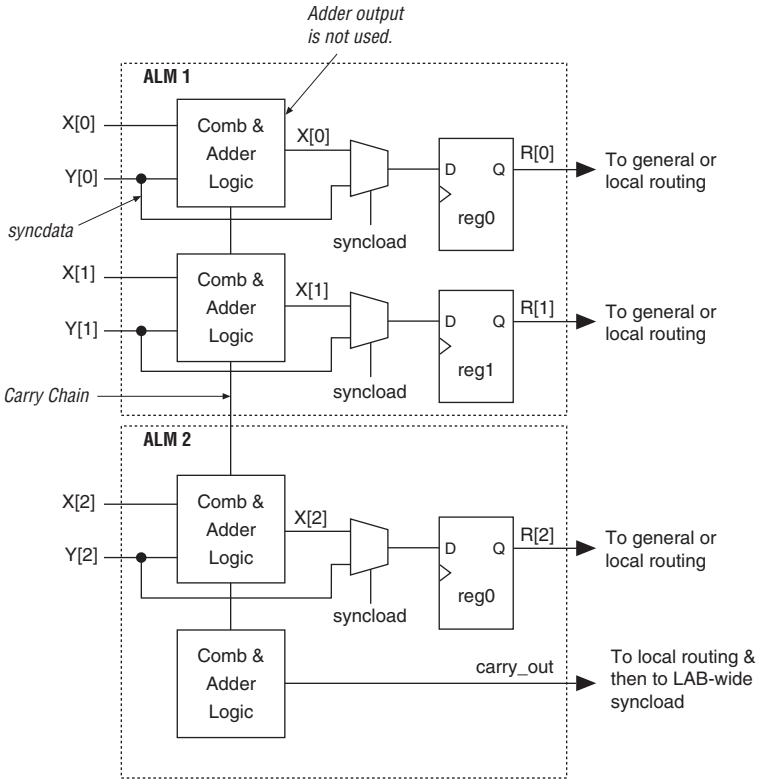
Figure 2–8. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that could be placed into one ALM may be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments.

Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are utilized, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (see Figure 2–9). If

Figure 2–12. Conditional Operation Example

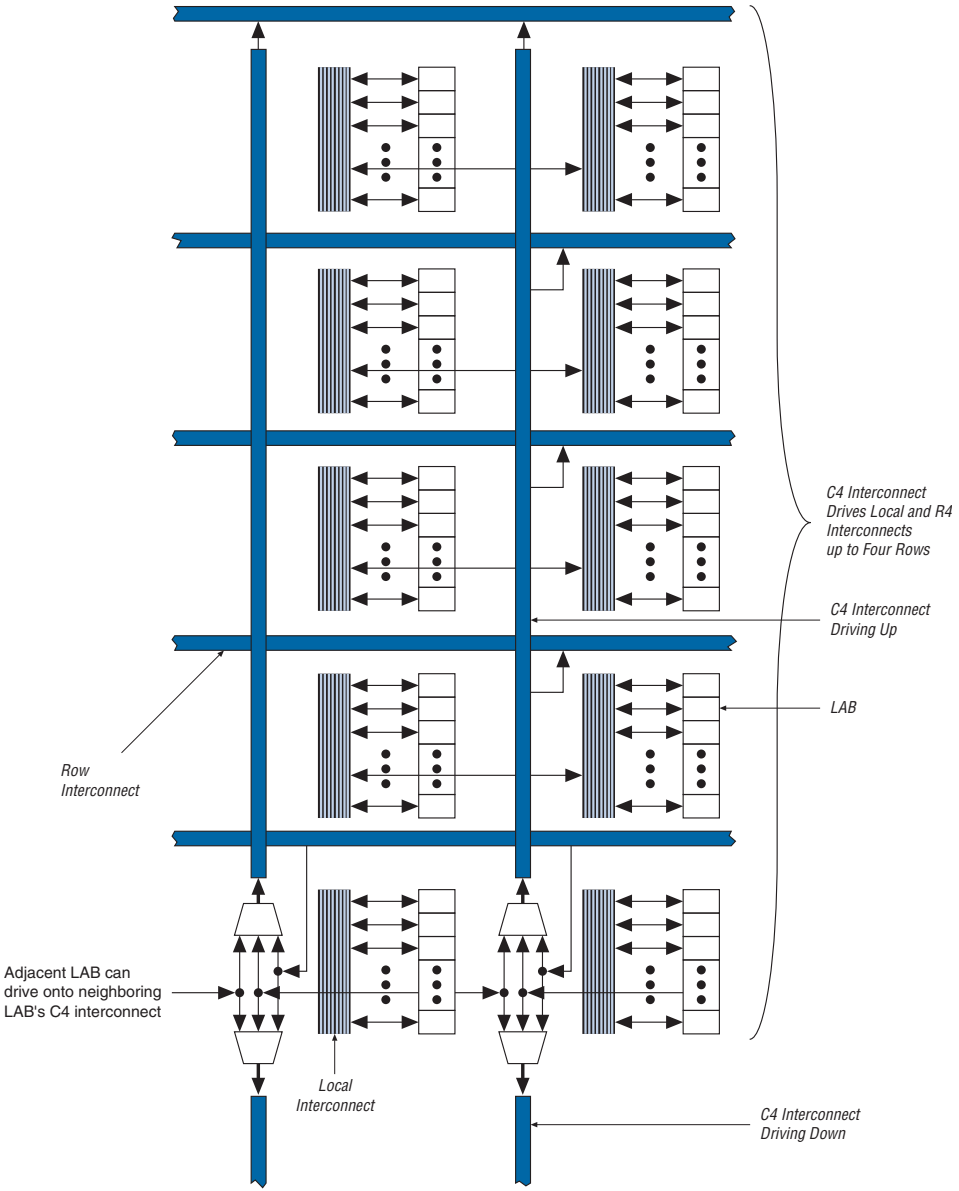


The arithmetic mode also offers clock enable, counter enable, synchronous up/down control, add/subtract control, synchronous clear, synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up/down and add/subtract control signals. These control signals are good candidates for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

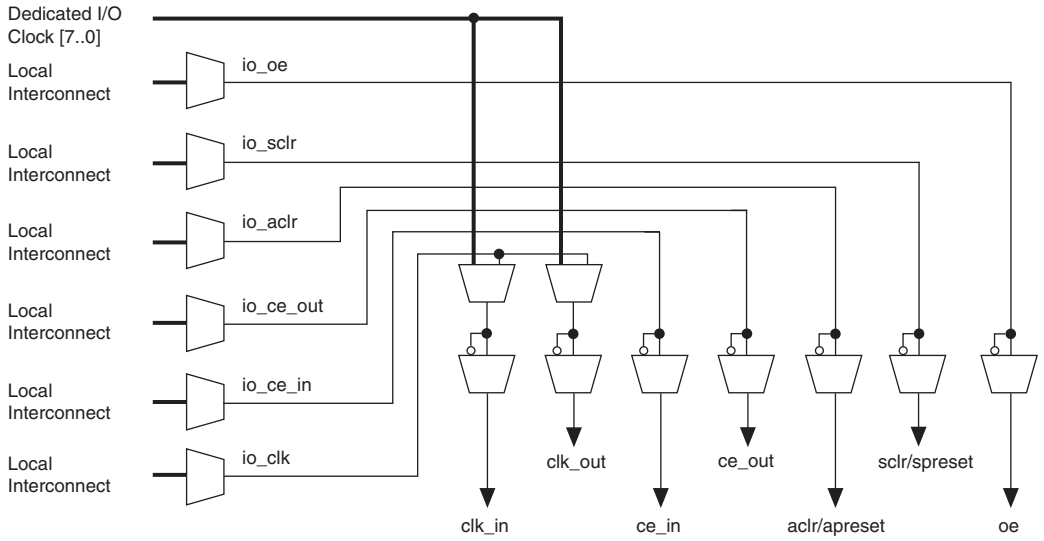
The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in an LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

Figure 2–18. C4 Interconnect Connections *Note (1)*



Note to Figure 2–18:
(1) Each C4 interconnect can drive either up or down four rows.

Figure 2–50. Control Signal Selection per IOE



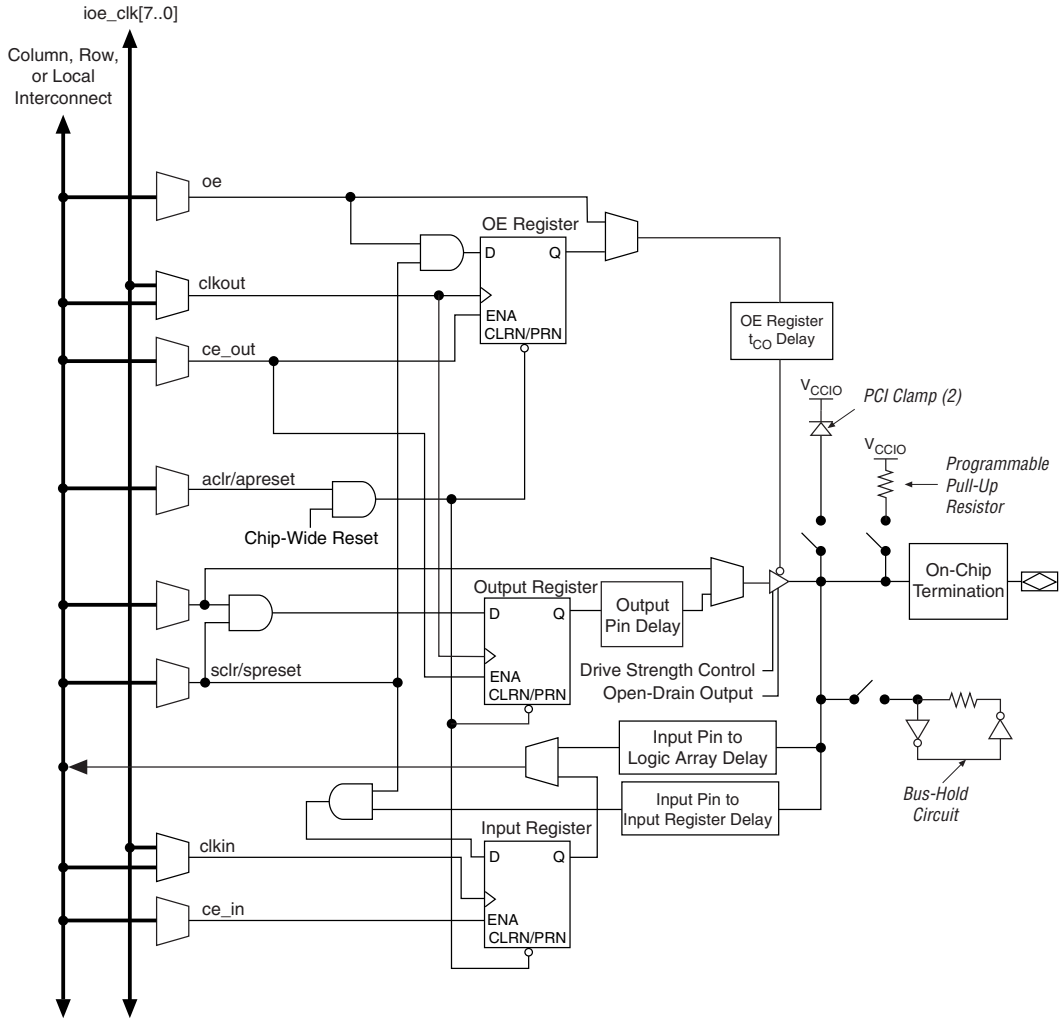
Notes to Figure 2–50:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects.

Figure 2–51 shows the IOE in bidirectional configuration.

Figure 2–51. Stratix II IOE in Bidirectional I/O Configuration *Note (1)*

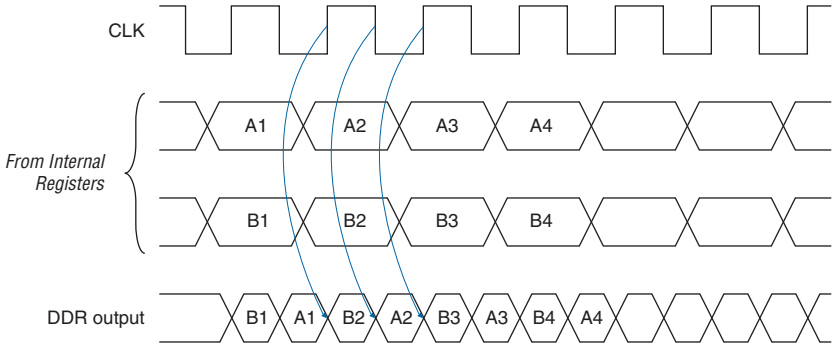


Notes to Figure 2–51:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The optional PCI clamp is only available on column I/O pins.

Figure 2–55. Output TIming Diagram in DDR Mode



The Stratix II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Stratix II devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces. Stratix II devices support DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM memory interfaces. In every Stratix II device, the I/O banks at the top (banks 3 and 4) and bottom (banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–14 shows the number of DQ and DQS buses that are supported per device.

Table 2–14. DQS & DQ Bus Mode Support (Part 1 of 2) *Note (1)*

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2S15	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S30	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
EP2S60	484-pin FineLine BGA	8	4	0	0
	672-pin FineLine BGA	18	8	4	0
	1,020-pin FineLine BGA	36	18	8	4

Document Revision History

Table 2–27 shows the revision history for this chapter.

Table 2–27. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.3	Updated "Clock Control Block" section.	—
	Updated note in the "Clock Control Block" section.	—
	Deleted Tables 2-11 and 2-12.	—
	Updated notes to: • Figure 2–41 • Figure 2–42 • Figure 2–43 • Figure 2–45	—
	Updated notes to Table 2–18.	—
	Moved Document Revision History to end of the chapter.	—
August 2006, v4.2	Updated Table 2–18 with note.	—
April 2006, v4.1	• Updated Table 2–13. • Removed Note 2 from Table 2–16. • Updated "On-Chip Termination" section and Table 2–19 to include parallel termination with calibration information. • Added new "On-Chip Parallel Termination with Calibration" section. • Updated Figure 2–44.	• Added parallel on-chip termination description and specification. • Changed RCLK names to match the Quartus II software in Table 2–13.
December 2005, v4.0	Updated "Clock Control Block" section.	—
July 2005, v3.1	• Updated HyperTransport technology information in Table 2–18. • Updated HyperTransport technology information in Figure 2–57. • Added information on the asynchronous clear signal.	—
May 2005, v3.0	• Updated "Functional Description" section. • Updated Table 2–3. • Updated "Clock Control Block" section. • Updated Tables 2–17 through 2–19. • Updated Tables 2–20 through 2–22. • Updated Figure 2–57.	—
March 2005, 2.1	• Updated "Functional Description" section. • Updated Table 2–3.	—

For more information on JTAG, see the following documents:

- The *IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing for Stratix II & Stratix II GX Devices* chapter of the *Stratix II Device Handbook, Volume 2* or the *Stratix II GX Device Handbook, Volume 2*
- Jam Programming & Test Language Specification

SignalTap II Embedded Logic Analyzer

Stratix II devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA® packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix II architecture are configured with CMOS SRAM elements. Altera® FPGA devices are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Stratix II devices are configured at system power-up with data stored in an Altera configuration device or provided by an external controller (e.g., a MAX® II device or microprocessor). Stratix II devices can be configured using the fast passive parallel (FPP), active serial (AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. The Stratix II device's optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix II devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

In addition to the number of configuration methods supported, Stratix II devices also offer the design security, decompression, and remote system upgrade features. The design security feature, using configuration bitstream encryption and AES technology, provides a mechanism to protect your designs. The decompression feature allows Stratix II FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of your Stratix II designs. For more information, see "Configuration Schemes" on page 3–7.

error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

RSC is supported in the following Stratix II configuration schemes: FPP, AS, PS, and PPA. RSC can also be implemented in conjunction with advanced Stratix II features such as real-time decompression of configuration data and design security using AES for secure and efficient field upgrades.

See the *Remote System Upgrades With Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information about remote configuration in Stratix II devices.

Configuring Stratix II FPGAs with JRunner

JRunner is a software driver that configures Altera FPGAs, including Stratix II FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File **(.rbf)** format. JRunner also requires a Chain Description File **(.cdf)** generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information on the JRunner software driver, see the *JRunner Software Driver: An Embedded Solution to the JTAG Configuration White Paper* and the source files on the Altera web site **(www.altera.com)**.

Programming Serial Configuration Devices with SRunner

A serial configuration device can be programmed in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit in different embedded systems. SRunner is able to read a **.rpd** file (Raw Programming Data) and write to the serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time when using the Quartus II software.

For more information about SRunner, see the *SRunner: An Embedded Solution for EPCS Programming* White Paper and the source code on the Altera web site at **www.altera.com**.

For more information on programming serial configuration devices, see the Serial Configuration Devices (EPCS1 & EPCS4) Data Sheet in the *Configuration Handbook*.

Figure 3–1. External Temperature-Sensing Diode

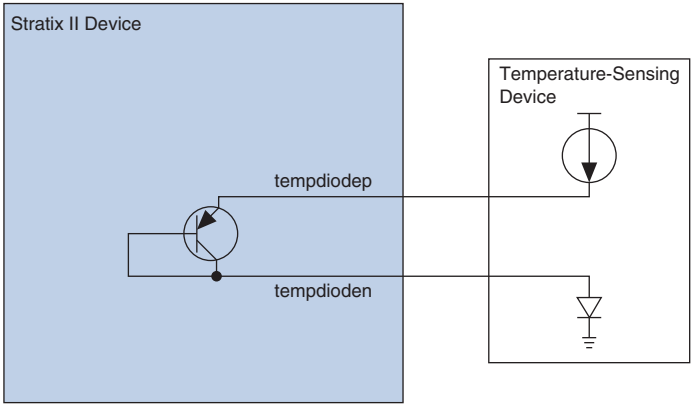


Table 3–6 shows the specifications for bias voltage and current of the Stratix II temperature sensing diode.

Table 3–6. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
IBIAS high	80	100	120	µA
IBIAS low	8	10	12	µA
VBP - VBN	0.3		0.9	V
VBN		0.7		V
Series resistance			3	Ω

Table 5–2. Maximum Duty Cycles in Voltage Transitions				
Symbol	**Parameter**	**Condition**	**Maximum Duty Cycles**	**Unit**
V_I	Maximum duty cycles in voltage transitions	V_I = 4.0 V	100	%
		V_I = 4.1 V	90	%
		V_I = 4.2 V	50	%
		V_I = 4.3 V	30	%
		V_I = 4.4 V	17	%
		V_I = 4.5 V	10	%

Recommended Operating Conditions

Table 5–3 contains the Stratix II device family recommended operating conditions.

Table 5–3. Stratix II Device Recommended Operating Conditions (Part 1 of 2) Note (1)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
V_{CCINT}	Supply voltage for internal logic	100 µs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCIO}	Supply voltage for input and output buffers, 3.3-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*, *(6)*	3.135 (3.00)	3.465 (3.60)	V
	Supply voltage for input and output buffers, 2.5-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	2.375	2.625	V
	Supply voltage for input and output buffers, 1.8-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	1.425	1.575	V
	Supply voltage for input and output buffers, 1.2-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	1.14	1.26	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers.	100 µs ≤ risetime ≤ 100 ms *(4)*	3.135	3.465	V
V_{CCA}	Analog power supply for PLLs	100 µs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCD}	Digital power supply for PLLs	100 µs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_I	Input voltage (see Table 5–2)	*(2)*, *(5)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V

Table 5–14. 3.3-V PCI Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Low-level input voltage		–0.3		$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–15. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.30		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			$0.1 \times V_{CCIO}$	V

Table 5–16. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Reference voltage		0.855	0.900	0.945	V
V_{TT}	Termination voltage		$V_{REF} – 0.04$	V_{REF}	$V_{REF} + 0.04$	V
V_{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.125$			V
V_{IL} (DC)	Low-level DC input voltage				$V_{REF} – 0.125$	V
V_{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.25$			V
V_{IL} (AC)	Low-level AC input voltage				$V_{REF} – 0.25$	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	$V_{TT} + 0.475$			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			$V_{TT} – 0.475$	V

Note to Table 5–16:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–23. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 5–23:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–24. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 5–24:

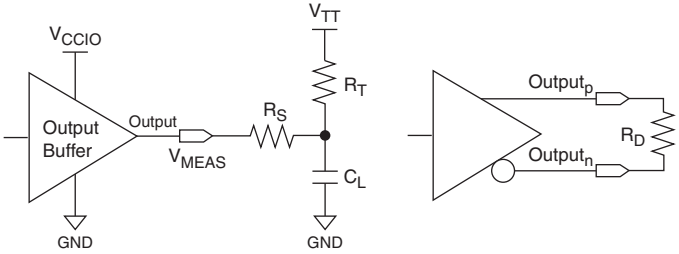
(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

4. Record the time to V_{MEAS}.

5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 5–34 using the above equation. Figure 5–4 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 5–4. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 5–4:

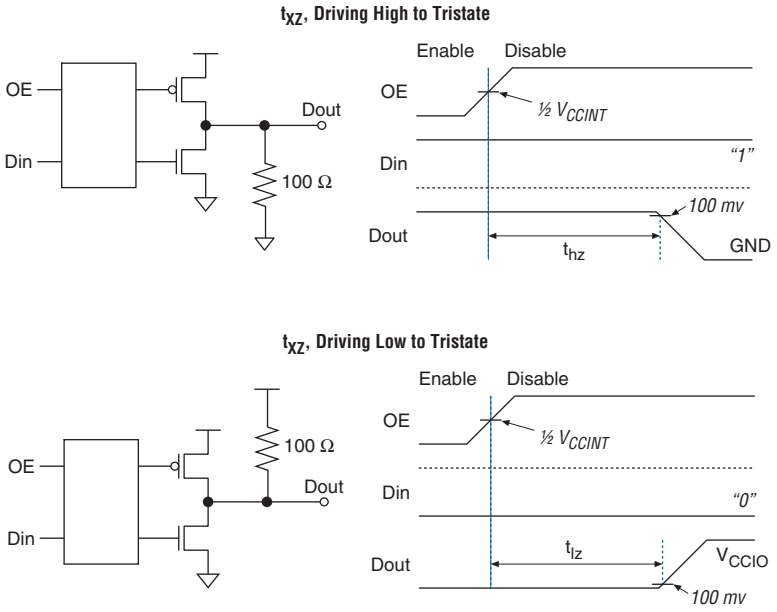
(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

(2) V_{CCPD} is 3.085 V unless otherwise specified.

(3) V_{CCINT} is 1.12 V unless otherwise specified.

Figures 5–5 and 5–6 show the measurement setup for output disable and output enable timing.

Figure 5–5. Measurement Setup for t_{xz} *Note (1)*



Note to Figure 5–5:
(1) V_{CCINT} is 1.12 V for this measurement.

Table 5–73. Stratix II I/O Input Delay for Column Pins (Part 3 of 3)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.2-V HSTL	t_{PI}	645	677	1194	1252	-	-	ps
	t_{PCOUT}	379	398	758	795	-	-	ps

Notes for Table 5–73:
(1) These I/O standards are only supported on DQS pins.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Table 5–74. Stratix II I/O Input Delay for Row Pins (Part 1 of 2)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (1)	-3 Speed Grade (2)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
LVTTL	t_{PI}	715	749	1287	1350	1477	1723	ps
	t_{PCOUT}	391	410	760	798	873	1018	ps
2.5 V	t_{PI}	726	761	1273	1335	1461	1704	ps
	t_{PCOUT}	402	422	746	783	857	999	ps
1.8 V	t_{PI}	788	827	1427	1497	1639	1911	ps
	t_{PCOUT}	464	488	900	945	1035	1206	ps
1.5 V	t_{PI}	792	830	1498	1571	1720	2006	ps
	t_{PCOUT}	468	491	971	1019	1116	1301	ps
LVCMOS	t_{PI}	715	749	1287	1350	1477	1723	ps
	t_{PCOUT}	391	410	760	798	873	1018	ps
SSTL-2 Class I	t_{PI}	547	573	879	921	1008	1176	ps
	t_{PCOUT}	223	234	352	369	404	471	ps
SSTL-2 Class II	t_{PI}	547	573	879	921	1008	1176	ps
	t_{PCOUT}	223	234	352	369	404	471	ps
SSTL-18 Class I	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
SSTL-18 Class II	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
1.5-V HSTL Class I	t_{PI}	602	631	1056	1107	1212	1413	ps
	t_{PCOUT}	278	292	529	555	608	708	ps

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 6 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
Differential SSTL-2 Class I	8 mA	t_{OP}	913	957	1715	1799	1971	2041	ps
		t_{DIP}	933	979	1781	1869	2047	2131	ps
	12 mA	t_{OP}	896	940	1672	1754	1921	1991	ps
		t_{DIP}	916	962	1738	1824	1997	2081	ps
Differential SSTL-2 Class II	16 mA	t_{OP}	876	918	1609	1688	1849	1918	ps
		t_{DIP}	896	940	1675	1758	1925	2008	ps
	20 mA	t_{OP}	877	919	1598	1676	1836	1905	ps
		t_{DIP}	897	941	1664	1746	1912	1995	ps
	24 mA	t_{OP}	872	915	1596	1674	1834	1903	ps
		t_{DIP}	892	937	1662	1744	1910	1993	ps
Differential SSTL-18 Class I	4 mA	t_{OP}	909	953	1690	1773	1942	2012	ps
		t_{DIP}	929	975	1756	1843	2018	2102	ps
	6 mA	t_{OP}	914	958	1656	1737	1903	1973	ps
		t_{DIP}	934	980	1722	1807	1979	2063	ps
	8 mA	t_{OP}	894	937	1640	1721	1885	1954	ps
		t_{DIP}	914	959	1706	1791	1961	2044	ps
	10 mA	t_{OP}	898	942	1638	1718	1882	1952	ps
		t_{DIP}	918	964	1704	1788	1958	2042	ps
	12 mA	t_{OP}	891	936	1626	1706	1869	1938	ps
		t_{DIP}	911	958	1692	1776	1945	2028	ps
Differential SSTL-18 Class II	8 mA	t_{OP}	883	925	1597	1675	1835	1904	ps
		t_{DIP}	903	947	1663	1745	1911	1994	ps
	16 mA	t_{OP}	894	937	1578	1655	1813	1882	ps
		t_{DIP}	914	959	1644	1725	1889	1972	ps
	18 mA	t_{OP}	890	933	1585	1663	1821	1890	ps
		t_{DIP}	910	955	1651	1733	1897	1980	ps
	20 mA	t_{OP}	890	933	1583	1661	1819	1888	ps
		t_{DIP}	910	955	1649	1731	1895	1978	ps

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 1 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	4 mA	270	225	210	270	225	210	270	225	210
	8 mA	435	355	325	435	355	325	435	355	325
	12 mA	580	475	420	580	475	420	580	475	420
	16 mA	720	594	520	-	-	-	720	594	520
	20 mA	875	700	610	-	-	-	875	700	610
	24 mA	1,030	794	670	-	-	-	1,030	794	670
3.3-V LVCMOS	4 mA	290	250	230	290	250	230	290	250	230
	8 mA	565	480	440	565	480	440	565	480	440
	12 mA	790	710	670	-	-	-	790	710	670
	16 mA	1,020	925	875	-	-	-	1,020	925	875
	20 mA	1,066	985	935	-	-	-	1,066	985	935
	24 mA	1,100	1,040	1,000	-	-	-	1,100	1,040	1,000
2.5-V LVTTL/LVCMOS	4 mA	230	194	180	230	194	180	230	194	180
	8 mA	430	380	380	430	380	380	430	380	380
	12 mA	630	575	550	630	575	550	630	575	550
	16 mA	930	845	820	-	-	-	930	845	820
1.8-V LVTTL/LVCMOS	2 mA	120	109	104	120	109	104	120	109	104
	4 mA	285	250	230	285	250	230	285	250	230
	6 mA	450	390	360	450	390	360	450	390	360
	8 mA	660	570	520	660	570	520	660	570	520
	10 mA	905	805	755	-	-	-	905	805	755
	12 mA	1,131	1,040	990	-	-	-	1,131	1,040	990
1.5-V LVTTL/LVCMOS	2 mA	244	200	180	244	200	180	244	200	180
	4 mA	470	370	325	470	370	325	470	370	325
	6 mA	550	430	375	-	-	-	550	430	375
	8 mA	625	495	420	-	-	-	625	495	420
SSTL-2 Class I	8 mA	400	300	300	-	-	-	400	300	300
	12 mA	400	400	350	400	350	350	400	400	350
SSTL-2 Class II	16 mA	350	350	300	350	350	300	350	350	300
	20 mA	400	350	350	-	-	-	400	350	350
	24 mA	400	400	350	-	-	-	400	400	350

Therefore, the DCD percentage for the 267 MHz SSTL-2 Class II DDIO row output clock on a –3 device ranges from 48.4% to 51.6%.

Table 5–83. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -4 & -5 Devices *Notes (1), (2)*

Row DDIO Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS/ HyperTransport Technology	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	3.3 V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps
LVDS/ HyperTransport technology	180	180	180	180	180	ps

Notes to Table 5–83:
(1) Table 5–83 assumes the input clock has zero DCD.
(2) The DCD specification is based on a no logic array noise condition.

Table 5–84. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 1 of 2) *Notes (1), (2)*

DDIO Column Output I/O Standard	Maximum DCD Based on I/O Standard of Input Feeding the DDIO Clock Port (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	1.2-V HSTL	
	3.3/2.5 V	1.8/1.5 V	2.5 V	1.8/1.5 V	1.2 V	
3.3-V LVTTL	260	380	145	145	145	ps
3.3-V LVCMOS	210	330	100	100	100	ps
2.5 V	195	315	85	85	85	ps