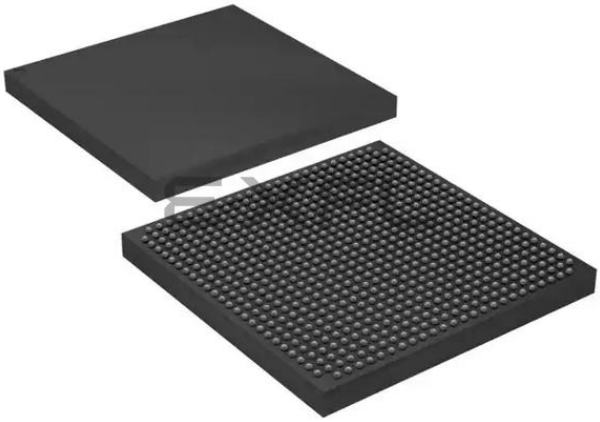

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	492
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s60f672i4

Chapter Revision Dates

The chapters in this book, *Stratix II Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction
Revised: *May 2007*
Part number: *SII51001-4.2*

Chapter 2. Stratix II Architecture
Revised: *May 2007*
Part number: *SII51002-4.3*

Chapter 3. Configuration & Testing
Revised: *May 2007*
Part number: *SII51003-4.2*

Chapter 4. Hot Socketing & Power-On Reset
Revised: *May 2007*
Part number: *SII51004-3.2*

Chapter 5. DC & Switching Characteristics
Revised: *April 2011*
Part number: *SII51005-4.5*

Chapter 6. Reference & Ordering Information
Revised: *April 2011*
Part number: *SII51006-2.2*

Stratix II devices are available in space-saving FineLine BGA® packages (see Tables 1–2 and 1–3).

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 *(3)*	334		492		718	
EP2S90 *(3)*		308		534	758	902
EP2S130 *(3)*				534	742	1,126
EP2S180 *(3)*					742	1,170

Notes to Table 1–2:

(1) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(2) The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not available as general-purpose I/O pins. The `PLL_ENA` pin can only be used to enable the PLLs within the device.

(3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm2)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

Document Revision History

Table 1–6 shows the revision history for this chapter.

Table 1–6. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.2	Moved Document Revision History to the end of the chapter.	—
April 2006, v4.1	• Updated "Features" section. • Removed Note 4 from Table 1–2. • Updated Table 1–4.	—
December 2005, v4.0	• Updated Tables 1–2, 1–4, and 1–5. • Updated Figure 2–43.	—
July 2005, v3.1	• Added vertical migration information, including Table 1–4. • Updated Table 1–5.	—
May 2005, v3.0	• Updated "Features" section. • Updated Table 1–2.	—
March 2005, v2.1	Updated "Introduction" and "Features" sections.	—
January 2005, v2.0	Added note to Table 1–2.	—
October 2004, v1.2	Updated Tables 1–2, 1–3, and 1–5.	—
July 2004, v1.1	• Updated Tables 1–1 and 1–2. • Updated "Features" section.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

2. Stratix II Architecture

SII51002-4.3

Functional Description

Stratix® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures (M512 RAM, M4K RAM, and M-RAM blocks), and digital signal processing (DSP) blocks.

Each LAB consists of eight adaptive logic modules (ALMs). An ALM is the Stratix II device family's basic building block of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

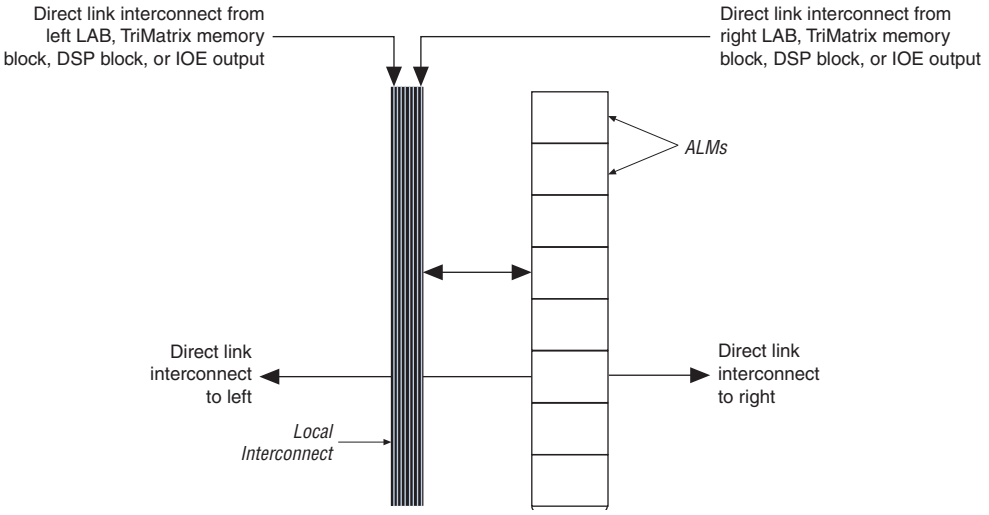
M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 500 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 550 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 420 MHz. Several M-RAM blocks are located individually in the device's logic array.

DSP blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. The DSP blocks support Q1.15 format rounding and saturation in the multiplier and accumulator stages. These blocks also contain shift registers for digital signal processing applications, including finite impulse response (FIR) and infinite impulse response (IIR) filters. DSP blocks are grouped into columns across the device and operate at up to 450 MHz.

Figure 2–3. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, and synchronous load control signals. This gives a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–4. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a `NOT` gate push-back technique to achieve preset. If you disable the `NOT` gate push-up option or assign a given register to power up high using the Quartus II software, the preset is achieved using the asynchronous load

arithmetic chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column.

Similar to the carry chains, the shared arithmetic chains are also top- or bottom-half bypassable. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable.

See the "MultiTrack Interconnect" on page 2–22 section for more information on shared arithmetic chain interconnect.

Register Chain

In addition to the general routing outputs, the ALMs in an LAB have register chain outputs. The register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows an LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (see Figure 2–15). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance.

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect. These column resources include:

- Shared arithmetic chain interconnects in an LAB
- Carry chain interconnects in an LAB and from LAB to LAB
- Register chain interconnects in an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM to ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–17 shows the shared arithmetic chain, carry chain and register chain interconnects.

Table 2–2. Stratix II Device Routing Scheme (Part 2 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Column IOE					✓			✓	✓							
Row IOE					✓	✓	✓	✓								

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–3 shows the size and features of the different RAM blocks.

Table 2–3. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	500 MHz	550 MHz	420 MHz
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	
ROM	✓	✓	*(1)*
FIFO buffer	✓	✓	✓
Pack mode		✓	✓
Byte enable	✓	✓	✓
Address clock enable		✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization (**.mif**)	✓	✓	

The Stratix II clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state thereby reducing the overall power consumption of the device.

The global and regional clock networks can be powered down statically through a setting in the configuration (**.sof** or **.pof**) file. Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable/disable feature allows the internal logic to control power up/down synchronously on GCLK and RCLK nets and PLL_OUT pins. This function is independent of the PLL and is applied directly on the clock network or PLL_OUT pin, as shown in Figures 2–37 through 2–39.

The following restrictions for the input clock pins apply:

- CLK0 pin -> inclk[0] of CLKCTRL
- CLK1 pin -> inclk[1] of CLKCTRL
- CLK2 pin -> inclk[0] of CLKCTRL
- CLK3 pin -> inclk[1] of CLKCTRL

In general, even CLK numbers connect to the inclk[0] port of CLKCTRL, and odd CLK numbers connect to the inclk[1] port of CLKCTRL.

Failure to comply with these restrictions will result in a no-fit error.

Enhanced & Fast PLLs

Stratix II devices provide robust clock management and synthesis using up to four enhanced PLLs and eight fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread-spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II device's enhanced PLLs provide you with complete control of clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

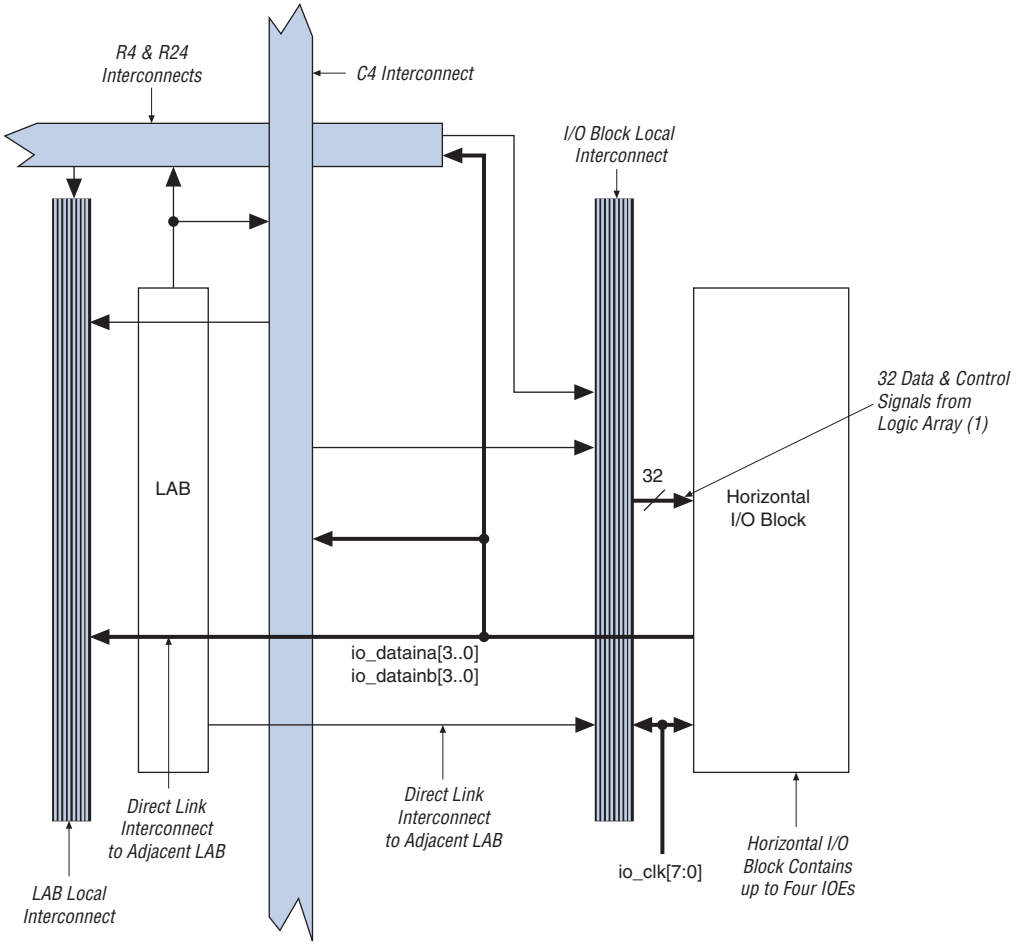
Table 2–11. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs (Part 1 of 2)

Top Side Global & Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓			✓				✓			
CLK13p	✓	✓	✓				✓						✓
CLK14p	✓			✓	✓			✓				✓	
CLK15p	✓			✓	✓				✓		✓		
CLK12n		✓				✓				✓			
CLK13n			✓				✓						✓
CLK14n				✓				✓				✓	
CLK15n					✓				✓		✓		
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										
GCLKDRV2				✓									
GCLKDRV3					✓								
RCLKDRV0						✓				✓			
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL 5 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓

- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double data rate (DDR) registers

The IOE in Stratix II devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–46 shows the Stratix II IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Figure 2–47. Row I/O Block Connection to the Interconnect *Note (1)*



Note to Figure 2–47:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

RSC is supported in the following Stratix II configuration schemes: FPP, AS, PS, and PPA. RSC can also be implemented in conjunction with advanced Stratix II features such as real-time decompression of configuration data and design security using AES for secure and efficient field upgrades.

See the *Remote System Upgrades With Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information about remote configuration in Stratix II devices.

Configuring Stratix II FPGAs with JRunner

JRunner is a software driver that configures Altera FPGAs, including Stratix II FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File **(.rbf)** format. JRunner also requires a Chain Description File **(.cdf)** generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information on the JRunner software driver, see the *JRunner Software Driver: An Embedded Solution to the JTAG Configuration White Paper* and the source files on the Altera web site **(www.altera.com)**.

Programming Serial Configuration Devices with SRunner

A serial configuration device can be programmed in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit in different embedded systems. SRunner is able to read a **.rpd** file (Raw Programming Data) and write to the serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time when using the Quartus II software.

For more information about SRunner, see the *SRunner: An Embedded Solution for EPCS Programming* White Paper and the source code on the Altera web site at **www.altera.com**.

For more information on programming serial configuration devices, see the Serial Configuration Devices (EPCS1 & EPCS4) Data Sheet in the *Configuration Handbook*.

Document Revision History

Table 4–1 shows the revision history for this chapter.

Table 4–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007, v3.2	Moved the Document Revision History section to the end of the chapter.	—
April 2006, v3.1	• Updated "Signal Pins Do Not Drive the VCCIO, VCCINT or VCCPD Power Supplies" section.	• Updated hot socketing AC specification.
May 2005, v3.0	• Updated "Signal Pins Do Not Drive the VCCIO, VCCINT or VCCPD Power Supplies" section. • Removed information on ESD protection.	—
January 2005, v2.1	Updated input rise and fall time.	—
January 2005, v2.0	Updated the "Hot Socketing Feature Implementation in Stratix II Devices", "ESD Protection", and "Power-On Reset Circuitry" sections.	—
July 2004, v1.1	• Updated all tables. • Added tables.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Table 5–36. Stratix II Performance Notes (Part 2 of 6) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
TriMatrix Memory M-RAM block	Single port RAM 4K × 144 bit	0	1	0	349.65	333.33	303.95	261.09	MHz
	Simple dual-port RAM 4K × 144 bit	0	1	0	420.16	400.00	364.96	313.47	MHz
	True dual-port RAM 4K × 144 bit	0	1	0	349.65	333.33	303.95	261.09	MHz
	Single port RAM 8K × 72 bit	0	1	0	354.60	337.83	307.69	263.85	MHz
	Simple dual-port RAM 8K × 72 bit	0	1	0	420.16	400.00	364.96	313.47	MHz
	True dual-port RAM 8K × 72 bit	0	1	0	349.65	333.33	303.95	261.09	MHz
	Single port RAM 16K × 36 bit	0	1	0	364.96	347.22	317.46	271.73	MHz
	Simple dual-port RAM 16K × 36 bit	0	1	0	420.16	400.00	364.96	313.47	MHz
	True dual-port RAM 16K × 36 bit	0	1	0	359.71	342.46	313.47	268.09	MHz
	Single port RAM 32K × 18 bit	0	1	0	364.96	347.22	317.46	271.73	MHz
	Simple dual-port RAM 32K × 18 bit	0	1	0	420.16	400.0	364.96	313.47	MHz
	True dual-port RAM 32K × 18 bit	0	1	0	359.71	342.46	313.47	268.09	MHz
	Single port RAM 64K × 9 bit	0	1	0	364.96	347.22	317.46	271.73	MHz
	Simple dual-port RAM 64K × 9 bit	0	1	0	420.16	400.0	364.96	313.47	MHz
	True dual-port RAM 64K × 9 bit	0	1	0	359.71	342.46	313.47	268.09	MHz

Table 5–38. IOE Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (3)	Max	Min (3)	Max	Min (4)	Max	Min (3)	Max	
t_{SU}	IOE input and output register setup time before clock	122		128		140 140		163		ps
t_{H}	IOE input and output register hold time after clock	72		75		82 82		96		ps
t_{CO}	IOE input and output register clock-to-output delay	101	169	101	177	97 101	194	101	226	ps
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinational output	410	760	410	798	391 410	873	410	1,018	ps
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinational output	428	787	428	825	408 428	904	428	1,054	ps
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinational output pin	1,101	2,026	1,101	2,127	1,049 1,101	2,329	1,101	2,439	ps
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinational output pin	991	1,854	991	1,946	944 991	2,131	991	2,246	ps
t_{CLR}	Minimum clear pulse width	200		210		229 229		268		ps
t_{PRE}	Minimum preset pulse width	200		210		229 229		268		ps
t_{CLKL}	Minimum clock low time	600		630		690 690		804		ps
t_{CLKH}	Minimum clock high time	600		630		690 690		804		ps

Notes to Table 5–38:

(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.

(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

(3) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.

(4) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 5 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.2-V Differential HSTL	OCT 50 Ω	280	-	-	-	-	-	280	-	-

Notes to Table 5–78:

(1) The toggle rate applies to 0-pF output load for all I/O standards except for LVDS and HyperTransport technology on row I/O pins. For LVDS and HyperTransport technology on row I/O pins, the toggle rates apply to load from 0 to 5pF.
(2) 1.2-V HSTL is only supported on column I/O pins in I/O banks 4, 7, and 8.
(3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.
(4) HyperTransport technology is only supported on row I/O and row dedicated clock input pins.
(5) LVPECL is only supported on column clock pins.
(6) Refer to Tables 5–81 through 5–91 if using SERDES block. Use the toggle rate values from the clock output column for PLL output.

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 1 of 5)

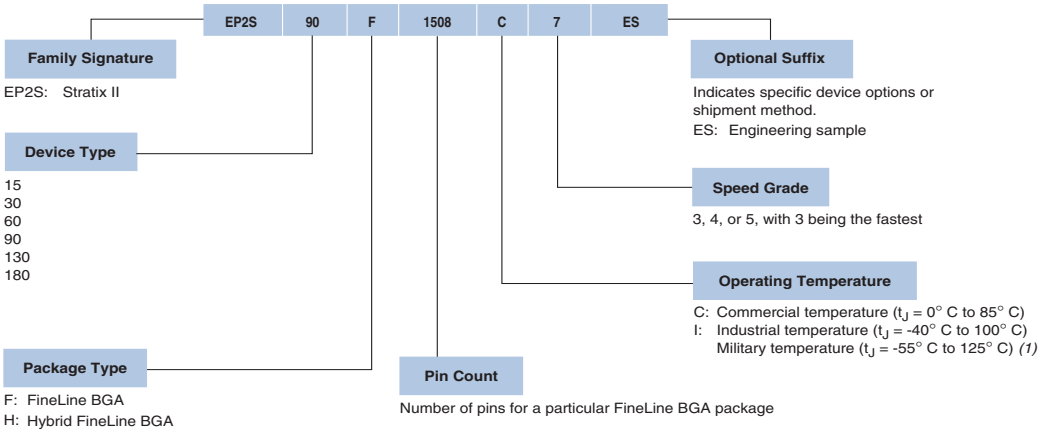
I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	4 mA	478	510	510	478	510	510	466	510	510
	8 mA	260	333	333	260	333	333	291	333	333
	12 mA	213	247	247	213	247	247	211	247	247
	16 mA	136	197	197	-	-	-	166	197	197
	20 mA	138	187	187	-	-	-	154	187	187
	24 mA	134	177	177	-	-	-	143	177	177
3.3-V LVCMOS	4 mA	377	391	391	377	391	391	377	391	391
	8 mA	206	212	212	206	212	212	178	212	212
	12 mA	141	145	145	-	-	-	115	145	145
	16 mA	108	111	111	-	-	-	86	111	111
	20 mA	83	88	88	-	-	-	79	88	88
	24 mA	65	72	72	-	-	-	74	72	72
2.5-V LVTTL/LVCMOS	4 mA	387	427	427	387	427	427	391	427	427
	8 mA	163	224	224	163	224	224	170	224	224
	12 mA	142	203	203	142	203	203	152	203	203
	16 mA	120	182	182	-	-	-	134	182	182

Table 5–93. Fast PLL Specifications

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (for -3 and -4 speed grade devices)	16.08		717	MHz
	Input clock frequency (for -5 speed grade devices)	16.08		640	MHz
f_{INPFD}	Input frequency to the PFD	16.08		500	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤ 2 MHz		0.5		ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 2 MHz		1.0		ns (p-p)
f_{VCO}	Upper VCO frequency range for –3 and –4 speed grades	300		1,040	MHz
	Upper VCO frequency range for –5 speed grades	300		840	MHz
	Lower VCO frequency range for –3 and –4 speed grades	150		520	MHz
	Lower VCO frequency range for –5 speed grades	150		420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875		550	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
f_{OUT_IO}	PLL clock output frequency to regular I/O pin	4.6875		*(1)*	MHz
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs		$75/f_{SCANCLK}$		ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5.00	28.00	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration		0.03	1.00	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift			±15	ps
t_{ARESET}	Minimum pulse width on areset signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500			ns

Note to Table 5–93:
(1) Limited by I/O f_{MAX}. See Table 5–77 on page 5–67 for the maximum.

Figure 6–1. Stratix II Device Packaging Ordering Information



Note to Figure 6–1:
(1) Applicable to I4 devices. For more information, refer to the *Stratix II Military Temperature Range Support* technical brief.

Document Revision History

Table 6–1 shows the revision history for this chapter.

Table 6–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
April 2011, v2.2	Updated Figure 6–1.	Added operating junction temperature for military use.
May 2007, v2.1	Moved the Document Revision History section to the end of the chapter.	—
January 2005, v2.0	Contact information was removed.	—
October 2004, v1.1	Updated Figure 6–1.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—