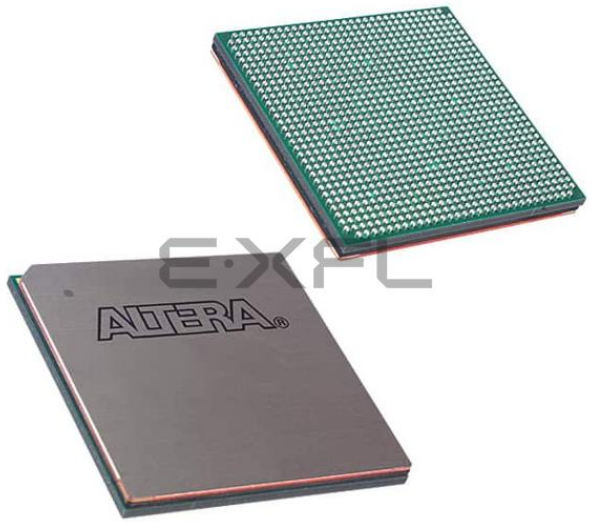

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520488
Number of I/O	758
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s90f1020c3

Chapter 3. Configuration & Testing

Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC & Switching Characteristics

Chapter 6. Reference & Ordering Information

Section I. Stratix II Device Family Data Sheet

This section provides the data sheet specifications for Stratix® II devices. This section contains feature definitions of the internal architecture, configuration and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Stratix II devices.

This section contains the following chapters:

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

Stratix II devices are available in up to three speed grades, -3, -4, and -5, with -3 being the fastest. Table 1–5 shows Stratix II device speed-grade offerings.

Table 1–5. Stratix II Device Speed Grades

Device	Temperature Grade	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S30	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S60	Commercial	-3, -4, -5		-3, -4, -5		-3, -4, -5	
	Industrial	-4		-4		-4	
EP2S90	Commercial		-4, -5		-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S130	Commercial				-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S180	Commercial					-3, -4, -5	-3, -4, -5
	Industrial					-4	-4

2. Stratix II Architecture

SII51002-4.3

Functional Description

Stratix® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures (M512 RAM, M4K RAM, and M-RAM blocks), and digital signal processing (DSP) blocks.

Each LAB consists of eight adaptive logic modules (ALMs). An ALM is the Stratix II device family's basic building block of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

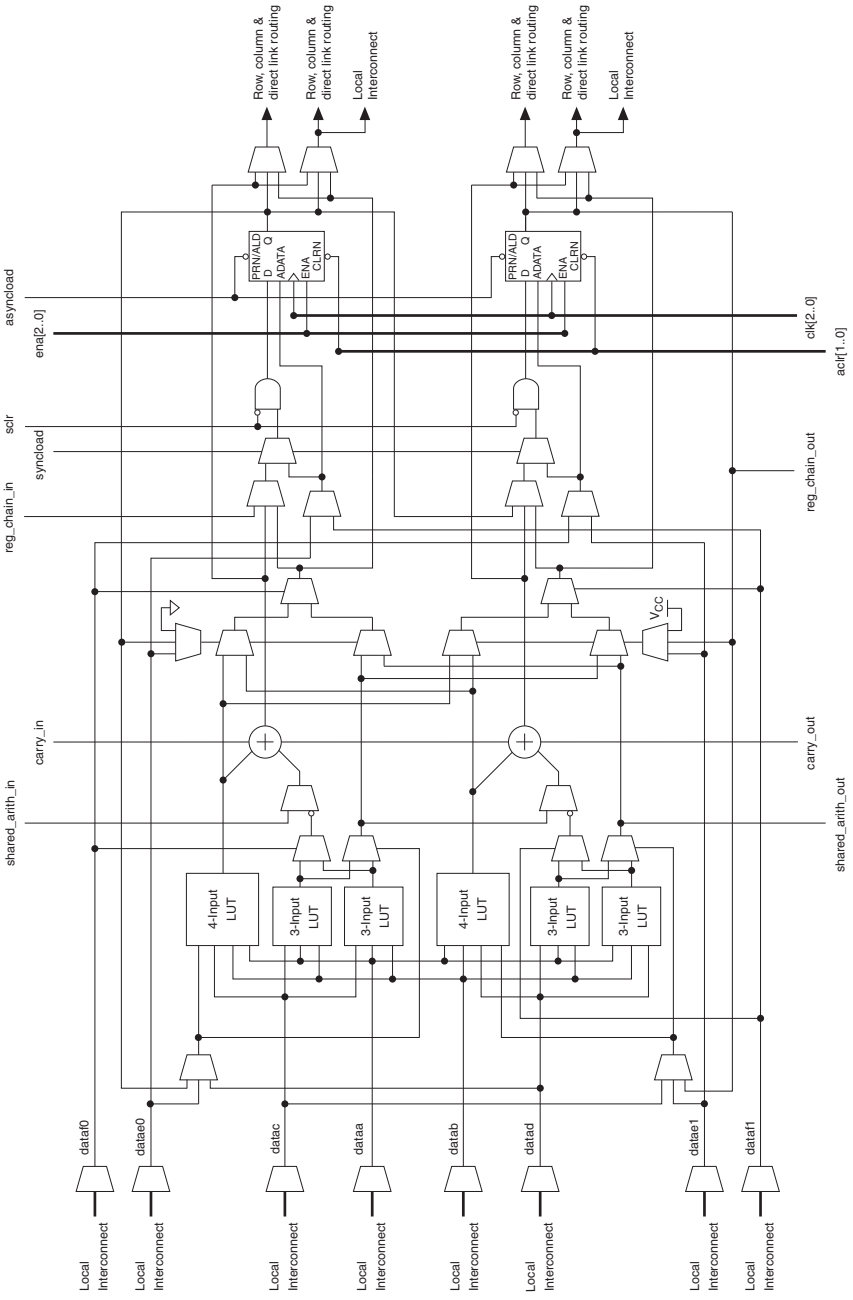
M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 500 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 550 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 420 MHz. Several M-RAM blocks are located individually in the device's logic array.

DSP blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. The DSP blocks support Q1.15 format rounding and saturation in the multiplier and accumulator stages. These blocks also contain shift registers for digital signal processing applications, including finite impulse response (FIR) and infinite impulse response (IIR) filters. DSP blocks are grouped into columns across the device and operate at up to 450 MHz.

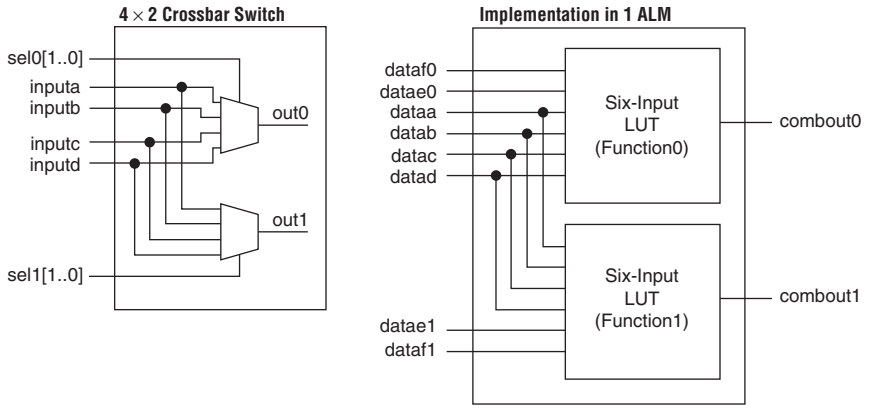
Figure 2–6. Stratix II ALM Details



For the packing of two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

In the case of implementing two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–8. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–8. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that could be placed into one ALM may be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments.

Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are utilized, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (see Figure 2–9). If

Table 2–3. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support		✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Notes to Table 2–3:

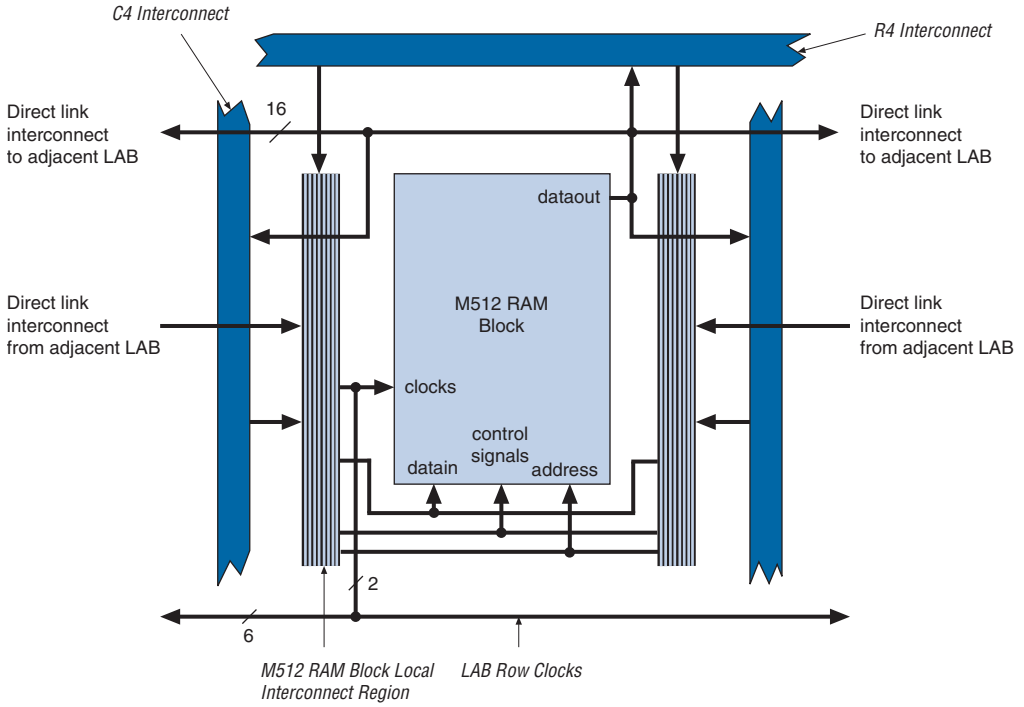
(1) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix II device must write to the dual-port memory once and then disable the write-enable ports afterwards.

Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

When applied to input registers, the asynchronous clear signal for the TriMatrix embedded memory immediately clears the input registers. However, the output of the memory block does not show the effects until the next clock edge. When applied to output registers, the asynchronous clear signal clears the output registers and the effects are seen immediately.

Figure 2–20. M512 RAM Block LAB Row Interface



M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–6 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions. The DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18 × 18-bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9 × 9-bit multipliers in simple multiplier mode.

Table 2–6. Multiplier Size & Configurations per DSP Block

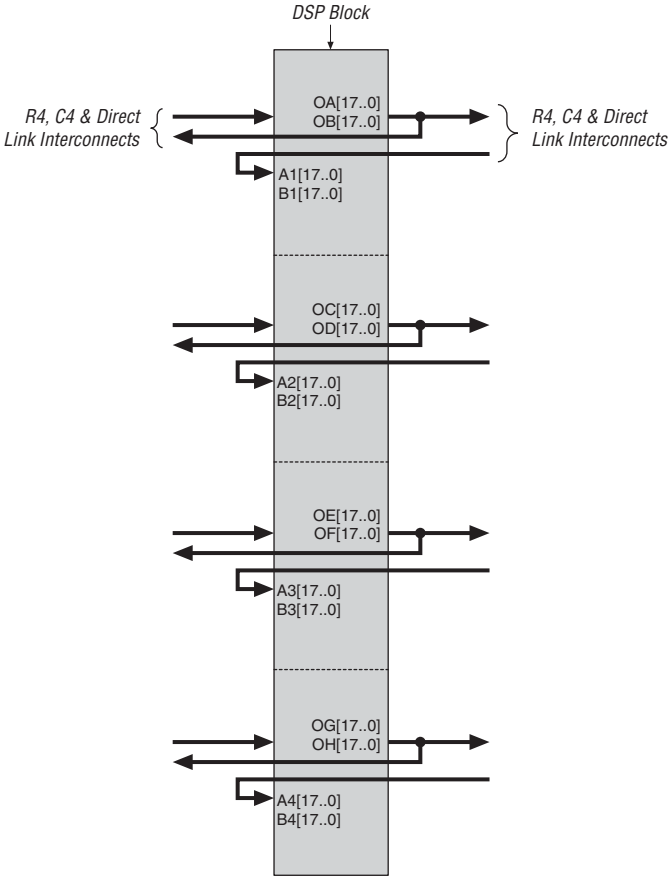
DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	-	Two 52-bit multiply-accumulate blocks	-
Two-multipliers adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	-
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	-

DSP Block Interface

Stratix II device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

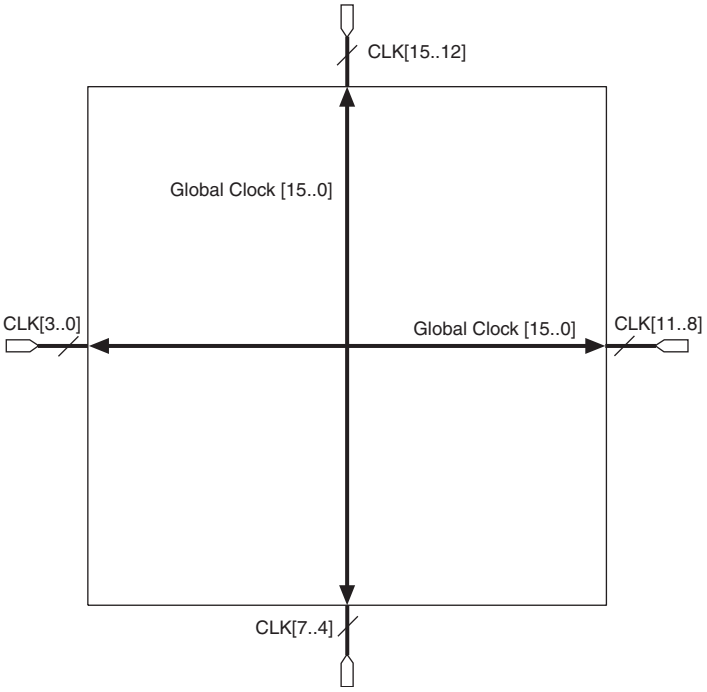
The DSP block is divided into four block units that interface with four LAB rows on the left and right. Each block unit can be considered one complete 18 × 18-bit multiplier with 36 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 16 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and eighteen can drive to the right LAB though direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing. Figures 2–29 and 2–30 show the DSP block interfaces to LAB rows.

Figure 2–29. DSP Block Interconnect Interface



global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–31 shows the 16 dedicated CLK pins driving global clock networks.

Figure 2–31. Global Clocking

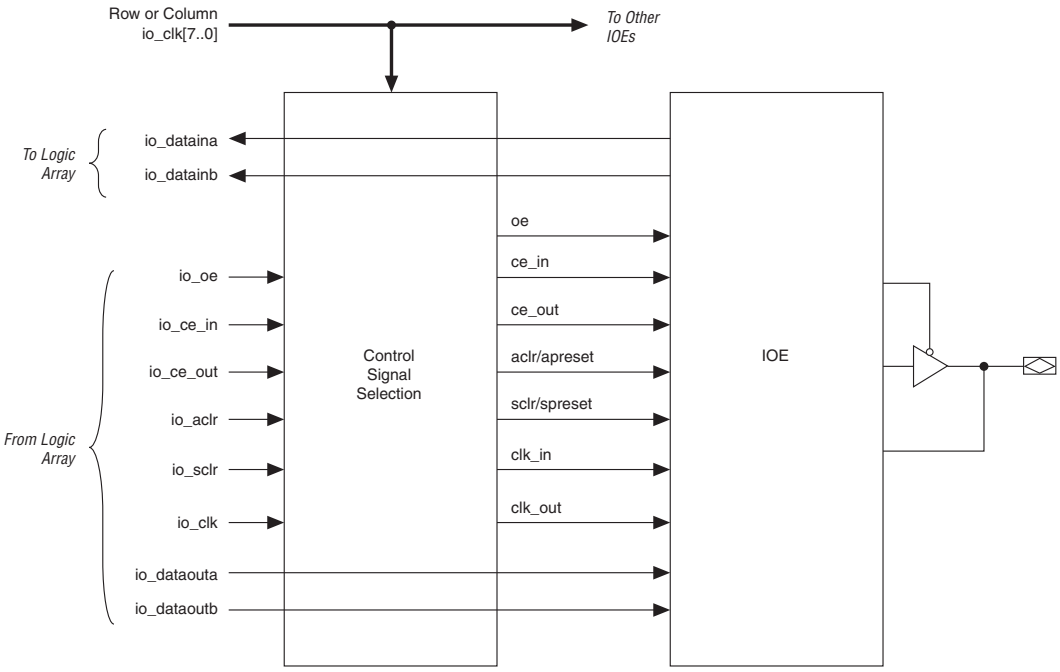


Regional Clock Network

There are eight regional clock networks RCLK[7..0] in each quadrant of the Stratix II device that are driven by the dedicated CLK[15..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK clock pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–32.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (see the "PLLs & Clock Networks" section). Figure 2–49 illustrates the signal paths through the I/O block.

Figure 2–49. Signal Path through the I/O Block



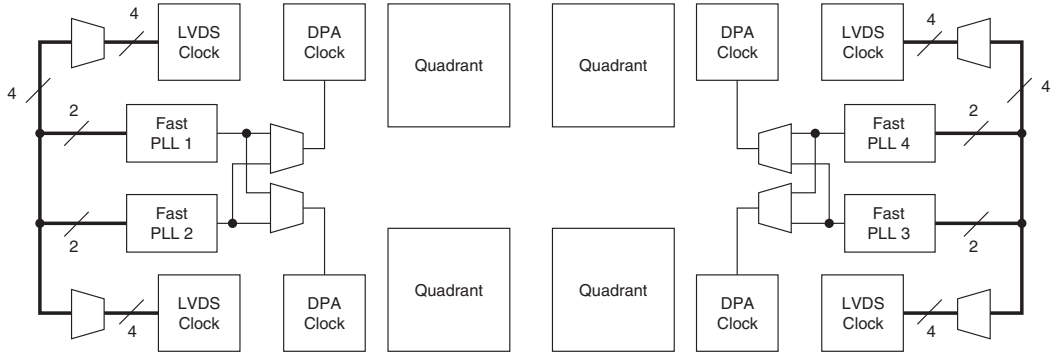
Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–50 illustrates the control signal selection.

For high-speed source synchronous interfaces such as POS-PHY 4, Parallel RapidIO, and HyperTransport, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols since the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix II device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving ALM resources. You can use an ALM-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Fast PLL & Channel Layout

The receiver and transmitter channels are interleaved such that each I/O bank on the left and right side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–60 shows the fast PLL and channel layout in the EP2S15 and EP2S30 devices. Figure 2–61 shows the fast PLL and channel layout in the EP2S60 to EP2S180 devices.

Figure 2–60. Fast PLL & Channel Layout in the EP2S15 & EP2S30 Devices *Note (1)*



Note to Figure 2–60:
(1) See Table 2–21 for the number of channels each device supports.

the Device & Pin Options dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Stratix II devices, eliminating the need for external logic. For Stratix II devices, CRC is computed by the device during configuration and checked against an automatically computed CRC during normal operation. The CRC_ERROR pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built in the Stratix II devices to perform error detection automatically. This error detection circuitry in Stratix II devices constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a re-configuration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

In the Quartus II software version 4.1 and later, you can turn on the automated error detection CRC feature in the Device & Pin Options dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

Document Revision History

Table 3–7 shows the revision history for this chapter.

Table 3–7. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.2	Moved Document Revision History section to the end of the chapter.	—
	Updated the "Temperature Sensing Diode (TSD)" section.	—

Table 5–4. Stratix II Device DC Operating Conditions (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Unit
I_{CCI00}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C	EP2S15		4.0	*(3)*	mA
			EP2S30		4.0	*(3)*	mA
			EP2S60		4.0	*(3)*	mA
			EP2S90		4.0	*(3)*	mA
			EP2S130		4.0	*(3)*	mA
			EP2S180		4.0	*(3)*	mA
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	Vi = 0; V_{CCIO} = 3.3 V		10	25	50	kΩ
		Vi = 0; V_{CCIO} = 2.5 V		15	35	70	kΩ
		Vi = 0; V_{CCIO} = 1.8 V		30	50	100	kΩ
		Vi = 0; V_{CCIO} = 1.5 V		40	75	150	kΩ
		Vi = 0; V_{CCIO} = 1.2 V		50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration				1	2	kΩ

Notes to Table 5–4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) Maximum values depend on the actual T_J and design utilization. See the Excel-based PowerPlay Early Power Estimator (available at **www.altera.com**) or the Quartus II PowerPlay Power Analyzer feature for maximum values. See the section "Power Consumption" on page 5–20 for more information.

(4) Pin pull-up resistance values are lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 5–5 through 5–32 show the Stratix II device family I/O standard specifications.

Table 5–5. LVTTL Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4		V

Table 5–19. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.500	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.250	1.313	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.18		3.00	V
V_{IL} (DC)	Low-level DC input voltage		–0.30		V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.35			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} - 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(1)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(1)*			V_{TT} – 0.57	V

Note to Table 5–19:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–20. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.500	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.188	1.250	1.313	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.18		V_{CCIO} + 0.30	V
V_{IL} (DC)	Low-level DC input voltage		–0.30		V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.35			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} - 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*			V_{TT} – 0.76	V

Note to Table 5–20:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–41. M4K Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (4)	Max	Min (4)	Max	Min (5)	Max	Min (4)	Max	
$t_{M4KDATAASU}$	A port data setup time before clock	22		23		25 25		29		ps
$t_{M4KDATAAH}$	A port data hold time after clock	203		213		233 233		272		ps
$t_{M4KADDRASU}$	A port address setup time before clock	22		23		25 25		29		ps
$t_{M4KADDRAH}$	A port address hold time after clock	203		213		233 233		272		ps
$t_{M4KDATABSU}$	B port data setup time before clock	22		23		25 25		29		ps
$t_{M4KDATABH}$	B port data hold time after clock	203		213		233 233		272		ps
$t_{M4KRADDRBSU}$	B port address setup time before clock	22		23		25 25		29		ps
$t_{M4KRADDRBH}$	B port address hold time after clock	203		213		233 233		272		ps
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers	334	524	334	549	319 334	601	334	701	ps
$t_{M4KDATACO2}$ (6)	Clock-to-output delay without output registers	1,616	2,453	1,616	2,574	1,540 1,616	2,820	1,616	3,286	ps
$t_{M4KCLKH}$	Minimum clock high time	1,250		1,312		1,437 1,437		1,675		ps
$t_{M4KCLKL}$	Minimum clock low time	1,250		1,312		1,437 1,437		1,675		ps
t_{M4KCLR}	Minimum clear pulse width	144		151		165 165		192		ps

Notes to Table 5–41:

(1) F_{MAX} of M4K Block obtained using the Quartus II software does not necessarily equal to 1/TM4KRC.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.
(4) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.
(5) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.
(6) Numbers apply to unpacked memory modes, true dual-port memory modes, and simple dual-port memory modes that use locally routed or non-identical sources for the A and B port registers.

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 7 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
1.8-V Differential HSTL Class I	4 mA	t_{OP}	912	956	1608	1687	1848	1943	ps
		t_{DIP}	932	978	1674	1757	1924	2033	ps
	6 mA	t_{OP}	917	962	1595	1673	1833	1928	ps
		t_{DIP}	937	984	1661	1743	1909	2018	ps
	8 mA	t_{OP}	896	940	1586	1664	1823	1917	ps
		t_{DIP}	916	962	1652	1734	1899	2007	ps
	10 mA	t_{OP}	900	944	1591	1669	1828	1923	ps
		t_{DIP}	920	966	1657	1739	1904	2013	ps
	12 mA	t_{OP}	892	936	1585	1663	1821	1916	ps
		t_{DIP}	912	958	1651	1733	1897	2006	ps
1.8-V Differential HSTL Class II	16 mA	t_{OP}	877	919	1385	1453	1591	1680	ps
		t_{DIP}	897	941	1451	1523	1667	1770	ps
	18 mA	t_{OP}	879	921	1394	1462	1602	1691	ps
		t_{DIP}	899	943	1460	1532	1678	1781	ps
	20 mA	t_{OP}	879	921	1402	1471	1611	1700	ps
		t_{DIP}	899	943	1468	1541	1687	1790	ps
1.5-V Differential HSTL Class I	4 mA	t_{OP}	912	956	1607	1686	1847	1942	ps
		t_{DIP}	932	978	1673	1756	1923	2032	ps
	6 mA	t_{OP}	917	961	1588	1666	1825	1920	ps
		t_{DIP}	937	983	1654	1736	1901	2010	ps
	8 mA	t_{OP}	899	943	1590	1668	1827	1922	ps
		t_{DIP}	919	965	1656	1738	1903	2012	ps
	10 mA	t_{OP}	900	943	1592	1670	1829	1924	ps
		t_{DIP}	920	965	1658	1740	1905	2014	ps
	12 mA	t_{OP}	893	937	1590	1668	1827	1922	
		t_{DIP}	913	959	1656	1738	1903	2012	