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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520488
Number of I/O	758
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s90f1020c4n



Section I. Stratix II Device Family Data Sheet

This section provides the data sheet specifications for Stratix® II devices. This section contains feature definitions of the internal architecture, configuration and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Stratix II devices.

This section contains the following chapters:

- [Chapter 1, Introduction](#)
- [Chapter 2, Stratix II Architecture](#)
- [Chapter 3, Configuration & Testing](#)
- [Chapter 4, Hot Socketing & Power-On Reset](#)
- [Chapter 5, DC & Switching Characteristics](#)
- [Chapter 6, Reference & Ordering Information](#)

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

Stratix II devices are available in space-saving FineLine BGA® packages (see [Tables 1–2](#) and [1–3](#)).

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 (3)	334		492		718	
EP2S90 (3)		308		534	758	902
EP2S130 (3)				534	742	1,126
EP2S180 (3)					742	1,170

Notes to Table 1–2:

- (1) All I/O pin counts include eight dedicated clock input pins (clk1p, clk1n, clk3p, clk3n, clk9p, clk9n, clk11p, and clk11n) that can be used for data inputs.
- (2) The Quartus II software I/O pin counts include one additional pin, PLL_ENA, which is not available as general-purpose I/O pins. The PLL_ENA pin can only be used to enable the PLLs within the device.
- (3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (FPLL7CLKp/n, FPLL8CLKp/n, FPLL9CLKp/n, and FPLL10CLKp/n) that can be used for data inputs.

Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm ²)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

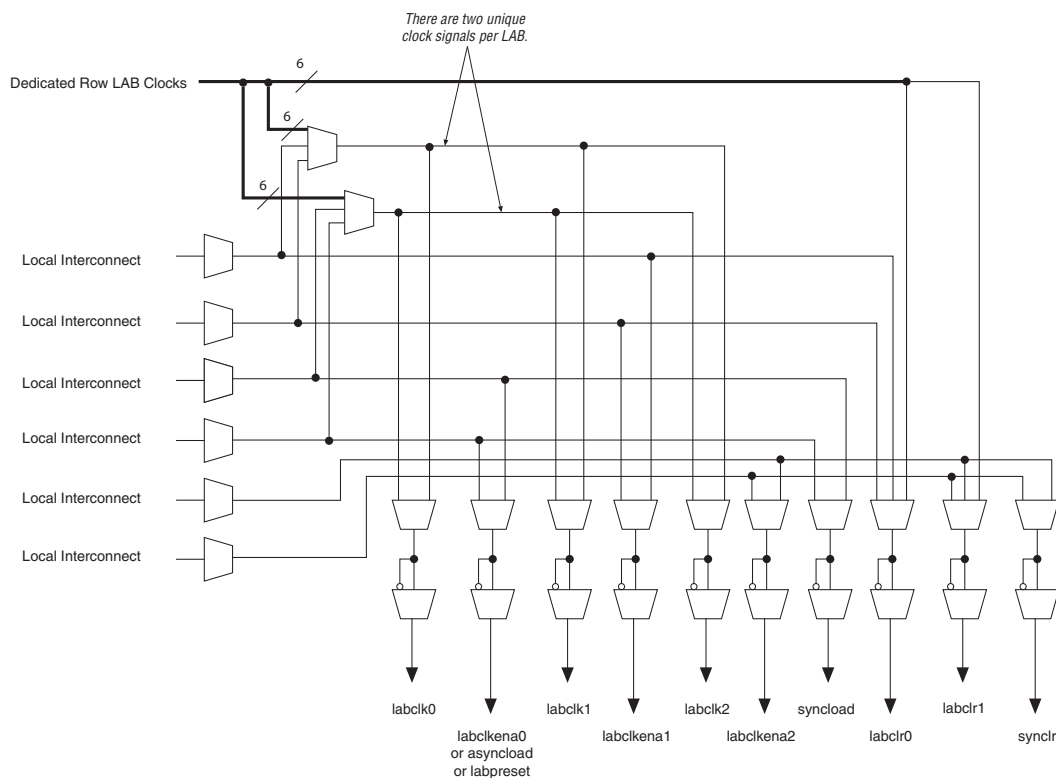
To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

signal with asynchronous load data input tied high. When the asynchronous load/preset signal is used, the `labclk0` signal is no longer available.

The LAB row clocks [5..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data.

Figure 2–4 shows the LAB control signal generation circuit.

Figure 2–4. LAB-Wide Control Signals



Adaptive Logic Modules

The basic building block of logic in the Stratix II architecture, the adaptive logic module (ALM), provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be

One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `dataae` or `dataaf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see [Figure 2-6](#)). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.



See the *Performance & Logic Efficiency Analysis of Stratix II Devices White Paper* for more information on the efficiencies of the Stratix II ALM and comparisons with previous architectures.

ALM Operating Modes

The Stratix II ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. In each mode, eleven available inputs to the ALM—the eight data inputs from the LAB local interconnect; `carry-in` from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear,

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column.

To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. This leaves the other half of the ALMs in the LAB available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB carry into the bottom half of the ALMs in the next LAB within the column. Every other column of LABs is top-half bypassable, while the other LAB columns are bottom-half bypassable.

See the [“MultiTrack Interconnect”](#) on page 2–22 section for more information on carry chain interconnect.

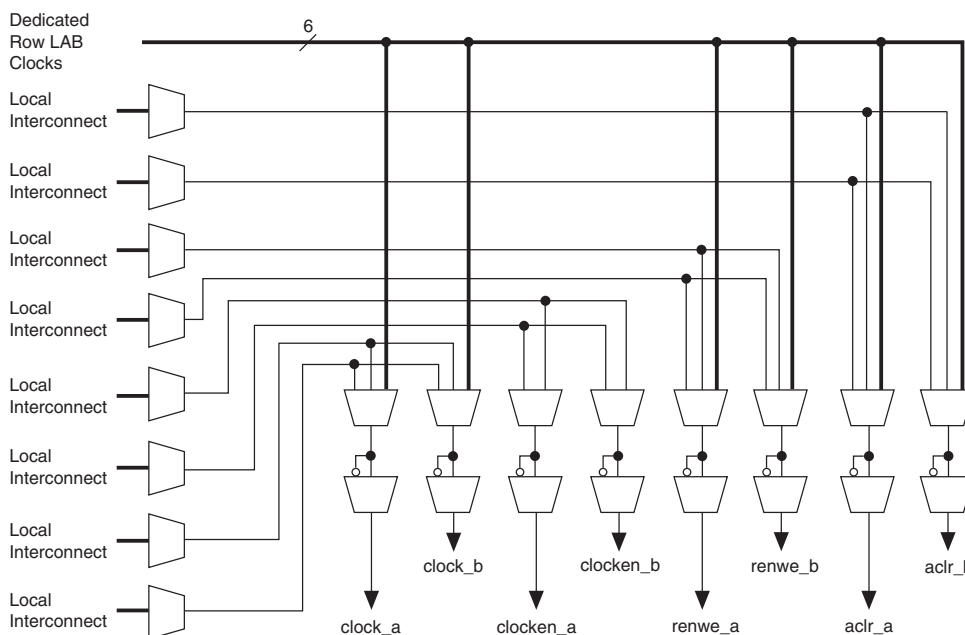
Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) via a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. [Figure 2–13](#) shows the ALM in shared arithmetic mode.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (renwe, address, byte enable, datain, and output registers). Only the output register can be bypassed. The six labclk signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. ALMs can also control the clock_a, clock_b, renwe_a, renwe_b, clr_a, clr_b, clocken_a, and clocken_b signals, as shown in Figure 2-21.

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2-22 shows the M4K RAM block to logic array interface.

Figure 2-21. M4K RAM Block Control Signals



Digital Signal Processing Block

The most commonly used DSP functions are FIR filters, complex FIR filters, IIR filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix II devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix II device has from two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Stratix II devices have up to 24 DSP blocks per column (see [Table 2–5](#)). Each DSP block can be configured to support up to:

- Eight 9×9 -bit multipliers
- Four 18×18 -bit multipliers
- One 36×36 -bit multiplier

As indicated, the Stratix II DSP block can support one 36×36 -bit multiplier in a single DSP block. This is true for any combination of signed, unsigned, or mixed sign multiplications.



This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

The DSP block is divided into four block units that interface with four LAB rows on the left and right. Each block unit can be considered one complete 18×18 -bit multiplier with 36 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 16 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and eighteen can drive to the right LAB through direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing. Figures 2-29 and 2-30 show the DSP block interfaces to LAB rows.

Figure 2-29. DSP Block Interconnect Interface

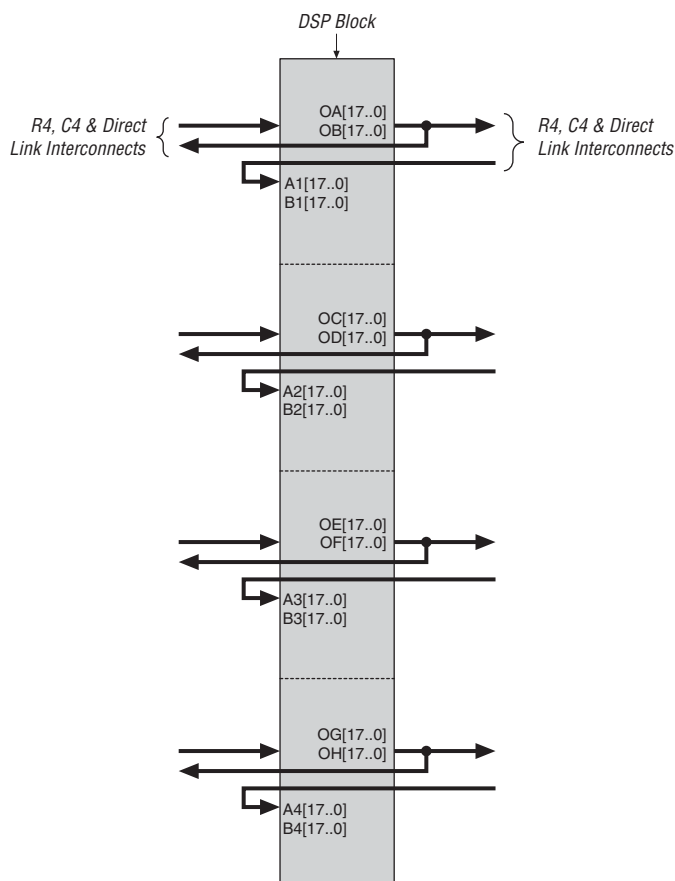
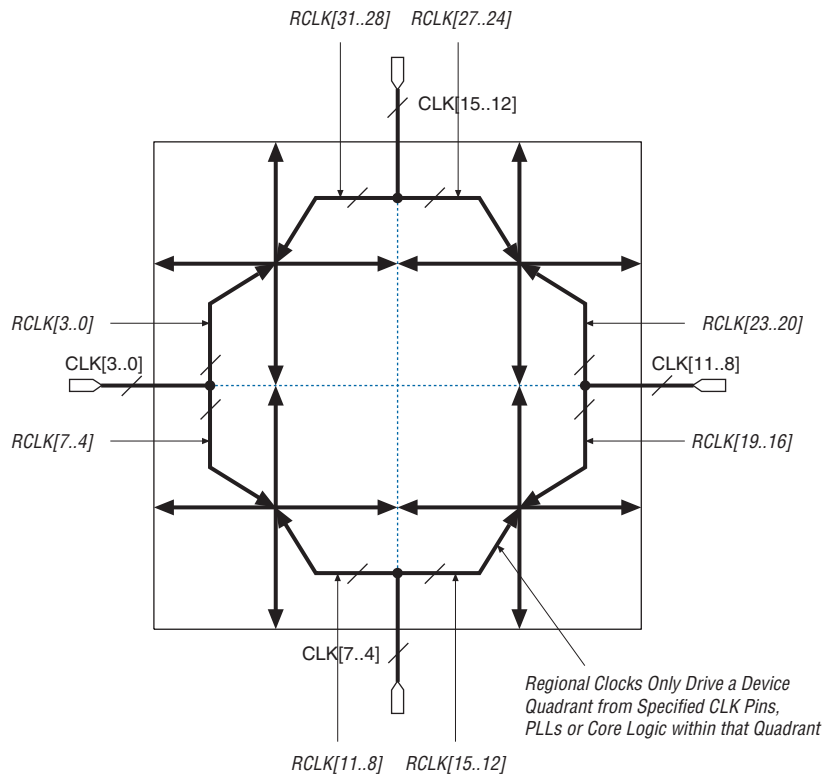


Figure 2–32. Regional Clocks

Dual-Regional Clock Network

A single source (CLK pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines in adjacent quadrants (one from each quadrant). This allows logic that spans multiple quadrants to utilize the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in [Figure 2–33](#). Corner PLLs cannot drive dual-regional clocks.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–9 shows the PLLs available for each Stratix II device and their type.

Table 2–9. Stratix II Device PLL Availability												
Device	Fast PLLs								Enhanced PLLs			
	1	2	3	4	7	8	9	10	5	6	11	12
EP2S15	✓	✓	✓	✓					✓	✓		
EP2S30	✓	✓	✓	✓					✓	✓		
EP2S60 (1)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S90 (2)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S130 (3)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S180	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes to Table 2–9:

- (1) EP2S60 devices in the 1020-pin package contain 12 PLLs. EP2S60 devices in the 484-pin and 672-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.
- (2) EP2S90 devices in the 1020-pin and 1508-pin packages contain 12 PLLs. EP2S90 devices in the 484-pin and 780-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.
- (3) EP2S130 devices in the 1020-pin and 1508-pin packages contain 12PLLs. The EP2S130 device in the 780-pin package contains fast PLLs 1–4 and enhanced PLLs 5 and 6.

- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double data rate (DDR) registers

The IOE in Stratix II devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. [Figure 2–46](#) shows the Stratix II IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Each I/O bank has its own V_{CCIO} pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated V_{REF} pins to support the voltage-referenced standards (such as SSTL-2). The PLL banks utilize the adjacent V_{REF} group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at V_{REFB7} is the reference voltage level for the SSTL input.

I/O pins that reside in PLL banks 9 through 12 are powered by the $VCC_PLL<5, 6, 11, \text{ or } 12>_OUT$ pins, respectively. The EP2S60F484, EP2S60F780, EP2S90H484, EP2S90F780, and EP2S130F780 devices do not support PLLs 11 and 12. Therefore, any I/O pins that reside in bank 11 are powered by the V_{CCIO3} pin, and any I/O pins that reside in bank 12 are powered by the V_{CCIO8} pin.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

On-Chip Termination

Stratix II devices provide differential (for the LVDS or HyperTransport technology I/O standard), series, and parallel on-chip termination to reduce reflections and maintain signal integrity. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Stratix II devices provide four types of termination:

- Differential termination (R_D)
- Series termination (R_S) without calibration
- Series termination (R_S) with calibration
- Parallel termination (R_T) with calibration

Table 2–27. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
January 2005, v2.0	<ul style="list-style-type: none"> Updated the “MultiVolt I/O Interface” and “TriMatrix Memory” sections. Updated Tables 2–3, 2–17, and 2–19. 	—
October 2004, v1.2	<ul style="list-style-type: none"> Updated Tables 2–9, 2–16, 2–26, and 2–27. 	—
July 2004, v1.1	<ul style="list-style-type: none"> Updated note to Tables 2–9 and 2–16. Updated Tables 2–16, 2–17, 2–18, 2–19, and 2–20. Updated Figures 2–41, 2–42, and 2–57. Removed 3 from list of SERDES factor <i>J</i>. Updated “High-Speed Differential I/O with DPA Support” section. In “Dedicated Circuitry with DPA Support” section, removed XSBI and changed RapidIO to Parallel RapidIO. 	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

you need to support configuration input voltages of 1.8 V/1.5 V, you should set the VCCSEL to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.



For more information on multi-volt support, including information on using TDO and nCEO in multi-volt systems, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Configuration Schemes

You can load the configuration data for a Stratix II device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II device. A configuration device can automatically configure a Stratix II device at system power-up.

You can configure multiple Stratix II devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Stratix II FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect your designs
- Remote system upgrades for remotely updating your Stratix II designs

Table 3–5 summarizes which configuration features can be used in each configuration scheme.

Table 3–5. Stratix II Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ (1)	✓ (1)	✓
	Enhanced configuration device		✓ (2)	✓
AS	Serial configuration device	✓	✓	✓ (3)
PS	MAX II device or microprocessor and flash device	✓	✓	✓
	Enhanced configuration device	✓	✓	✓
	Download cable (4)	✓	✓	

I_{IOPIN} is the current at any user I/O pin on the device. This specification takes into account the pin capacitance, but not board trace and external loading capacitance. Additional capacitance for trace, connector, and loading needs must be considered separately. For the AC specification, the peak current duration is 10 ns or less because of power-up transients. For more information, refer to the *Hot-Socketing & Power-Sequencing Feature & Testing for Altera Devices* white paper.

A possible concern regarding hot-socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot-socketed into an active system. During hot-socketing, the signal pins may be connected and driven by the active system before the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage. Nevertheless, Stratix II devices are immune to latch-up when hot-socketing.

Hot Socketing Feature Implementation in Stratix II Devices

The hot socketing feature turns off the output buffer during the power-up event (either V_{CCINT} , V_{CCIO} , or V_{CCPD} supplies) or power down. The hot-socket circuit will generate an internal `HOT_SCKT` signal when either V_{CCINT} , V_{CCIO} , or V_{CCPD} is below threshold voltage. The `HOT_SCKT` signal will cut off the output buffer to make sure that no DC current (except for weak pull up leaking) leaks through the pin. When V_{CC} ramps up very slowly, V_{CC} is still relatively low even after the POR signal is released and the configuration is finished. The `CONF_DONE`, `nCEO`, and `nSTATUS` pins fail to respond, as the output buffer can not flip from the state set by the hot socketing circuit at this low V_{CC} voltage. Therefore, the hot socketing circuit has been removed on these configuration pins to make sure that they are able to operate during configuration. It is expected behavior for these pins to drive out during power-up and power-down sequences.

Each I/O pin has the following circuitry shown in [Figure 4-1](#).

Table 5–70. Stratix II IOE Programmable Delay on Row Pins *Note (1)*

Parameter	Paths Affected	Available Settings	Minimum Timing (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade	
			Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)
Input delay from pin to internal cells	Pad to I/O dataout to logic array	8	0 0	1,697 1,782	0 0	2,876 3,020	0	3,308	0	3,853
Input delay from pin to input register	Pad to I/O input register	64	0 0	1,956 2,054	0 0	3,270 3,434	0	3,761	0	4,381
Delay from output register to output pin	I/O output register to pad	2	0 0	316 332	0 0	525 525	0	575	0	670
Output enable pin delay	t_{xz} , t_{zx}	2	0 0	305 320	0 0	507 507	0	556	0	647

Notes to Table 5–70:

- (1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.
- (2) The first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.
- (3) The first number applies to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices. The second number applies to -3 speed grade EP2S130 and EP2S180 devices.

Default Capacitive Loading of Different I/O Standards

See Table 5–71 for default capacitive loading of different I/O standards.

Table 5–71. Default Loading of Different I/O Standards for Stratix II (Part 1 of 2)

I/O Standard	Capacitive Load	Unit
LVTTTL	0	pF
LVC MOS	0	pF
2.5 V	0	pF
1.8 V	0	pF
1.5 V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL-2 Class I	0	pF

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 2 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class I	4 mA	200	150	150	200	150	150	200	150	150
	6 mA	350	250	200	350	250	200	350	250	200
	8 mA	450	300	300	450	300	300	450	300	300
	10 mA	500	400	400	500	400	400	500	400	400
	12 mA	700	550	400	-	-	-	650	550	400
SSTL-18 Class II	8 mA	200	200	150	-	-	-	200	200	150
	16 mA	400	350	350	-	-	-	400	350	350
	18 mA	450	400	400	-	-	-	450	400	400
	20 mA	550	500	450	-	-	-	550	500	450
1.8-V HSTL Class I	4 mA	300	300	300	300	300	300	300	300	300
	6 mA	500	450	450	500	450	450	500	450	450
	8 mA	650	600	600	650	600	600	650	600	600
	10 mA	700	650	600	700	650	600	700	650	600
	12 mA	700	700	650	700	700	650	700	700	650
1.8-V HSTL Class II	16 mA	500	500	450	-	-	-	500	500	450
	18 mA	550	500	500	-	-	-	550	500	500
	20 mA	650	550	550	-	-	-	550	550	550
1.5-V HSTL Class I	4 mA	350	300	300	350	300	300	350	300	300
	6 mA	500	500	450	500	500	450	500	500	450
	8 mA	700	650	600	700	650	600	700	650	600
	10 mA	700	700	650	-	-	-	700	700	650
	12 mA	700	700	700	-	-	-	700	700	700
1.5-V HSTL Class II	16 mA	600	600	550	-	-	-	600	600	550
	18 mA	650	600	600	-	-	-	650	600	600
	20 mA	700	650	600	-	-	-	700	650	600
Differential SSTL-2 Class I (3)	8 mA	400	300	300	400	300	300	400	300	300
	12 mA	400	400	350	400	400	350	400	400	350
Differential SSTL-2 Class II (3)	16 mA	350	350	300	350	350	300	350	350	300
	20 mA	400	350	350	350	350	297	400	350	350
	24 mA	400	400	350	-	-	-	400	400	350

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 5 of 5)

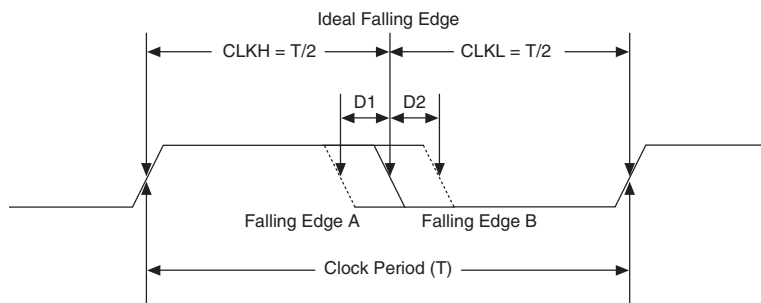
I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTTL	OCT 50 Ω	133	152	152	133	152	152	147	152	152
2.5-V LVTTTL	OCT 50 Ω	207	274	274	207	274	274	235	274	274
1.8-V LVTTTL	OCT 50 Ω	151	165	165	151	165	165	153	165	165
3.3-V LVCMOS	OCT 50 Ω	300	316	316	300	316	316	263	316	316
1.5-V LVCMOS	OCT 50 Ω	157	171	171	157	171	171	174	171	171
SSTL-2 Class I	OCT 50 Ω	121	134	134	121	134	134	77	134	134
SSTL-2 Class II	OCT 25 Ω	56	101	101	56	101	101	58	101	101
SSTL-18 Class I	OCT 50 Ω	100	123	123	100	123	123	106	123	123
SSTL-18 Class II	OCT 25 Ω	61	110	110	-	-	-	59	110	110
1.2-V HSTL (2)	OCT 50 Ω	95	-	-	-	-	-	-	-	95

Notes to Table 5–79:

- (1) For LVDS and HyperTransport technology output on row I/O pins, the toggle rate derating factors apply to loads larger than 5 pF. In the derating calculation, subtract 5 pF from the intended load value in pF for the correct result. For a load less than or equal to 5 pF, refer to Table 5–78 for output toggle rates.
- (2) 1.2-V HSTL is only supported on column I/O pins in I/O banks 4,7, and 8.
- (3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.
- (4) LVPECL is only supported on column clock outputs.

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 5–7. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (Figure 5–7). The maximum DCD for a clock is the larger value of D1 and D2.

Figure 5–7. Duty Cycle Distortion

DCD expressed in absolute derivation, for example, D1 or D2 in [Figure 5–7](#), is clock-period independent. DCD can also be expressed as a percentage, and the percentage number is clock-period dependent. DCD as a percentage is defined as

$$(T/2 - D1) / T \text{ (the low percentage boundary)}$$

$$(T/2 + D2) / T \text{ (the high percentage boundary)}$$

DCD Measurement Techniques

DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions ([Figure 5–8](#)). Therefore, any DCD present on the input clock signal or caused by the clock input buffer or different input I/O standard does not transfer to the output signal.

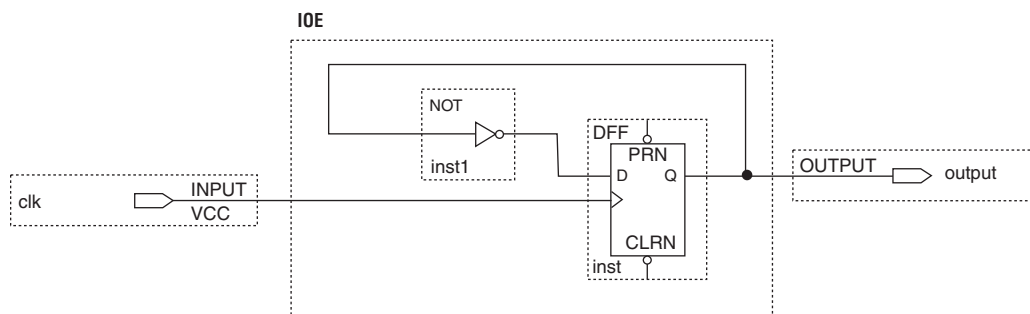
Figure 5–8. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs

Table 5–100. DQS Phase Offset Delay Per Stage <i>Notes (1), (2), (3)</i>			
Speed Grade	Min	Max	Unit
-3	9	14	ps
-4	9	14	ps
-5	9	15	ps

Notes to Table 5–100:

- (1) The delay settings are linear.
- (2) The valid settings for phase offset are -64 to +63 for frequency mode 0 and -32 to +31 for frequency modes 1, 2, and 3.
- (3) The typical value equals the average of the minimum and maximum values.

Table 5–101. DDIO Outputs Half-Period Jitter <i>Notes (1), (2)</i>			
Name	Description	Max	Unit
$t_{\text{OUTHALFJITTER}}$	Half-period jitter (PLL driving DDIO outputs)	200	ps

Notes to Table 5–101:

- (1) The worst-case half period is equal to the ideal half period subtracted by the DCD and half-period jitter values.
- (2) The half-period jitter was characterized using a PLL driving DDIO outputs.

JTAG Timing Specifications

Figure 5–10 shows the timing requirements for the JTAG signals.

Figure 5–10. Stratix II JTAG Waveforms

