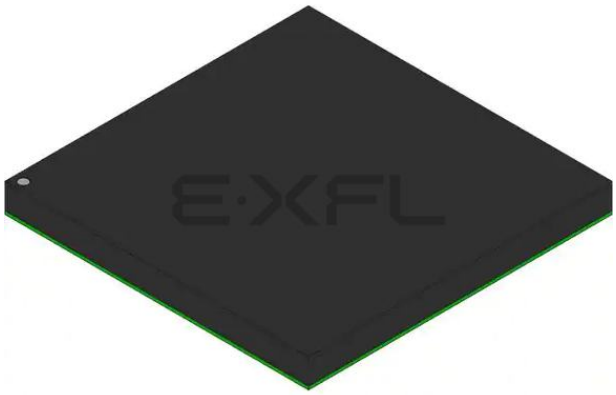

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520488
Number of I/O	758
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2s90f1020c5

Chapter 3. Configuration & Testing

Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC & Switching Characteristics

Chapter Revision Dates

The chapters in this book, *Stratix II Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Introduction
Revised: *May 2007*
Part number: *SII51001-4.2*

Chapter 2. Stratix II Architecture
Revised: *May 2007*
Part number: *SII51002-4.3*

Chapter 3. Configuration & Testing
Revised: *May 2007*
Part number: *SII51003-4.2*

Chapter 4. Hot Socketing & Power-On Reset
Revised: *May 2007*
Part number: *SII51004-3.2*

Chapter 5. DC & Switching Characteristics
Revised: *April 2011*
Part number: *SII51005-4.5*

Chapter 6. Reference & Ordering Information
Revised: *April 2011*
Part number: *SII51006-2.2*

Stratix II devices are available in up to three speed grades, -3, -4, and -5, with -3 being the fastest. Table 1–5 shows Stratix II device speed-grade offerings.

Table 1–5. Stratix II Device Speed Grades

Device	Temperature Grade	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S30	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S60	Commercial	-3, -4, -5		-3, -4, -5		-3, -4, -5	
	Industrial	-4		-4		-4	
EP2S90	Commercial		-4, -5		-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S130	Commercial				-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S180	Commercial					-3, -4, -5	-3, -4, -5
	Industrial					-4	-4

2. Stratix II Architecture

SII51002-4.3

Functional Description

Stratix® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures (M512 RAM, M4K RAM, and M-RAM blocks), and digital signal processing (DSP) blocks.

Each LAB consists of eight adaptive logic modules (ALMs). An ALM is the Stratix II device family's basic building block of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 500 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 550 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 420 MHz. Several M-RAM blocks are located individually in the device's logic array.

DSP blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. The DSP blocks support Q1.15 format rounding and saturation in the multiplier and accumulator stages. These blocks also contain shift registers for digital signal processing applications, including finite impulse response (FIR) and infinite impulse response (IIR) filters. DSP blocks are grouped into columns across the device and operate at up to 450 MHz.

IOE clocks have row and column block regions that are clocked by eight I/O clock signals chosen from the 24 quadrant clock resources. Figures 2–35 and 2–36 show the quadrant relationship to the I/O clock regions.

Figure 2–35. EP2S15 & EP2S30 Device I/O Clock Groups

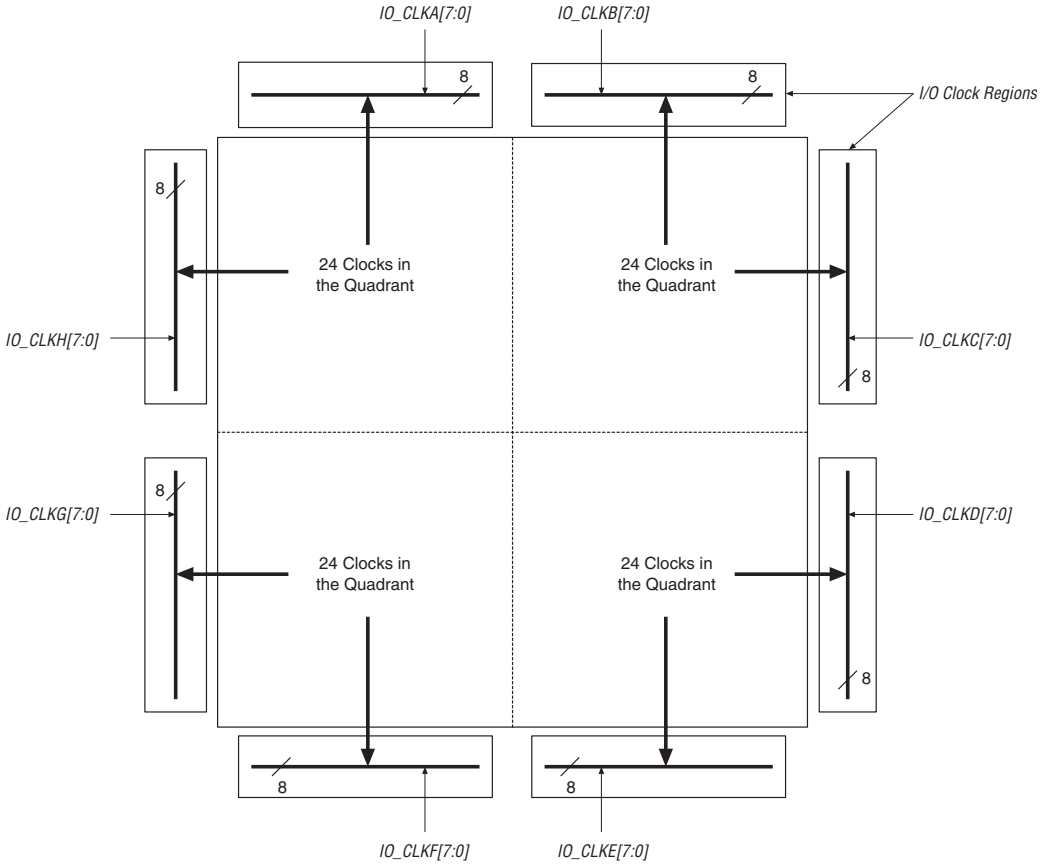
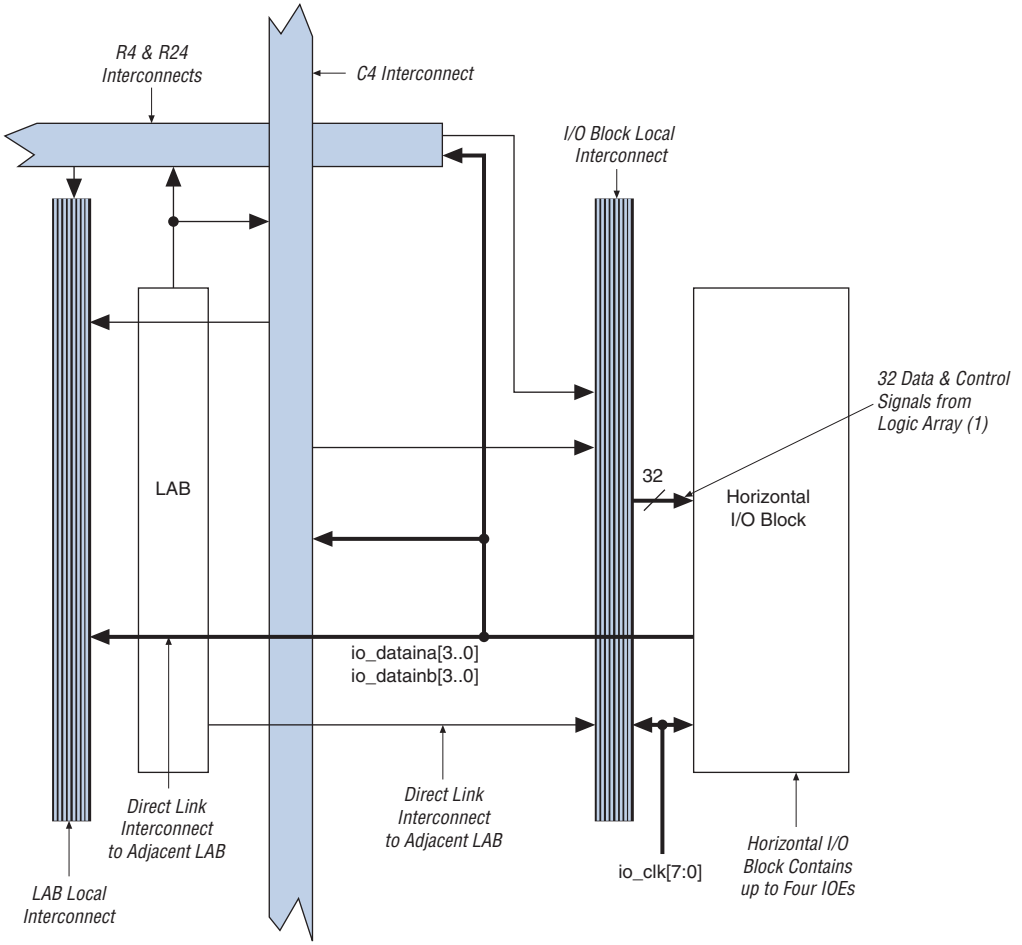


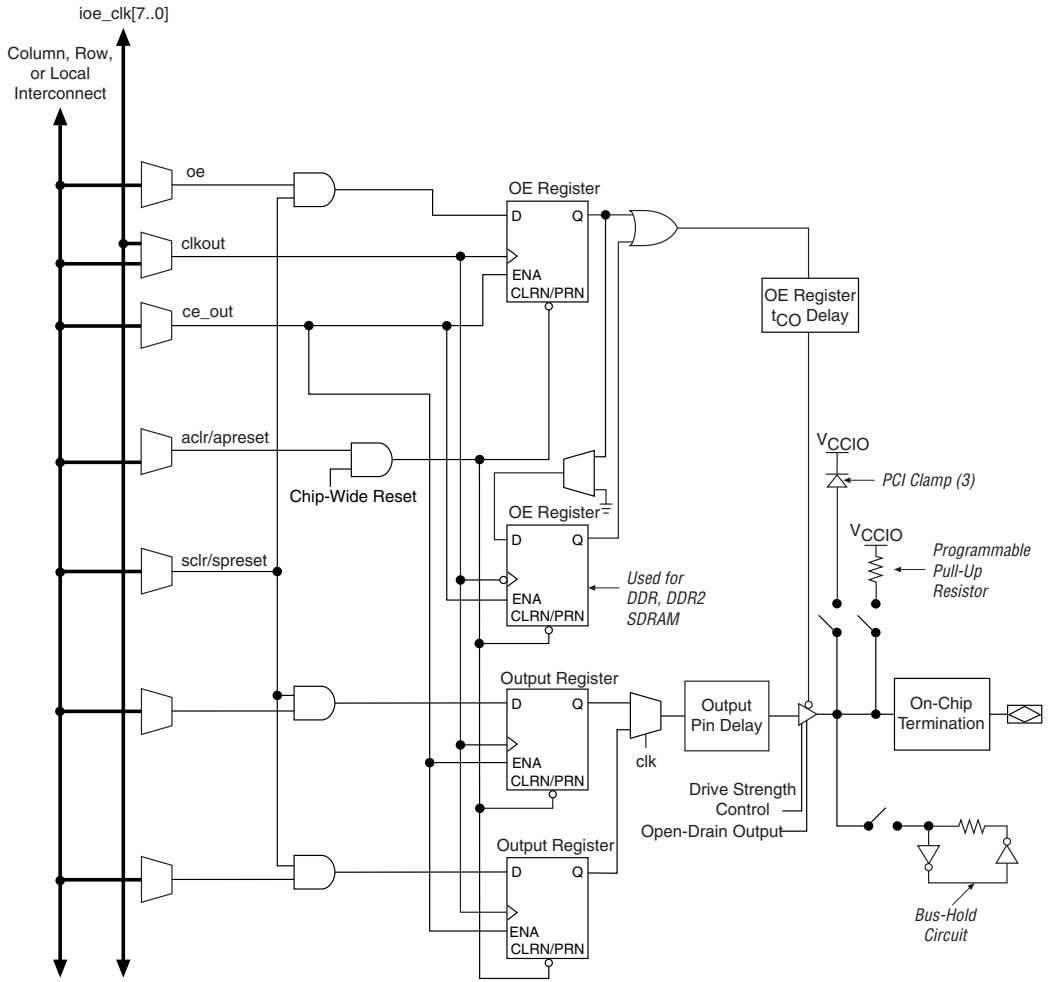
Figure 2–47. Row I/O Block Connection to the Interconnect *Note (1)*



Note to Figure 2–47:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

Figure 2–54. Stratix II IOE in DDR Output I/O Configuration *Notes (1), (2)*



Notes to Figure 2–54:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The tri-state buffer is active low. The DDIO megafunction represents the tri-state buffer as active-high with an inverter at the OE register data port. Similarly, the `aclr` and `apreset` signals are also active-high at the input ports of the DDIO megafunction.

(3) The optional PCI clamp is only available on column I/O pins.

For more information on tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

On-Chip Parallel Termination with Calibration

Stratix II devices support on-chip parallel termination with calibration for column I/O pins only. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip parallel termination calibration circuit compares the total impedance of each I/O buffer to the external 50-Ω resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

On-chip parallel termination with calibration is only supported for input pins.

For more information on on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

For more information on tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

MultiVolt I/O Interface

The Stratix II architecture supports the MultiVolt I/O interface feature that allows Stratix II devices in all packages to interface with systems of different supply voltages.

The Stratix II VCCINT pins must always be connected to a 1.2-V power supply. With a 1.2-V V_{CCINT} level, input pins are 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems).

The Stratix II VCCPD power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The VCCPD pins also power configuration input pins and JTAG input pins.

Operating Modes

The Stratix II architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select POR delay times of 12 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

The nIO PULLUP pin is a dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose configuration I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[2..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-ups, while a logic low turns them on.

Stratix II devices also offer a new power supply, V_{CCPD}, which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the configuration input pins when VCCSEL is connected to ground. See Table 3–4 for more information on the pins affected by VCCSEL.

The VCCSEL pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO}, the V_{IL} and V_{IH} levels driven to the configuration inputs do not have to be a concern.

4. Hot Socketing & Power-On Reset

SII51004-3.2

Stratix® II devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Stratix II board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature also removes some of the difficulty when you use Stratix II devices on printed circuit boards (PCBs) that also contain a mixture of 5.0-, 3.3-, 2.5-, 1.8-, 1.5- and 1.2-V devices. With the Stratix II hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix II hot socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Stratix II devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Stratix II Hot-Socketing Specifications

Stratix II devices offer hot socketing capability with all three features listed above without any external components or special design requirements. The hot socketing feature in Stratix II devices allows:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO}, V_{CCPD}, or V_{CCINT} power supplies. External input signals to I/O pins of the device do not internally power the V_{CCIO} or V_{CCINT} power supplies of the device via internal paths within the device.

Devices Can Be Driven Before Power-Up

You can drive signals into the I/O pins, dedicated input pins and dedicated clock pins of Stratix II devices before or during power-up or power-down without damaging the device. Stratix II devices support any power-up or power-down sequence (V_{CCIO}, V_{CCINT}, and V_{CCPD}) in order to simplify system level design.

I/O Pins Remain Tri-Stated During Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot socketing situation, Stratix II device's output buffers are turned off during system power-up or power-down. Stratix II device also does not drive out until the device is configured and has attained proper operating conditions.

Signal Pins Do Not Drive the V_{CCIO}, V_{CCINT} or V_{CCPD} Power Supplies

Devices that do not support hot-socketing can short power supplies together when powered-up through the device signal pins. This irregular power-up can damage both the driving and driven devices and can disrupt card power-up.

Stratix II devices do not have a current path from I/O pins, dedicated input pins, or dedicated clock pins to the V_{CCIO}, V_{CCINT}, or V_{CCPD} pins before or during power-up. A Stratix II device may be inserted into (or removed from) a powered-up system board without damaging or interfering with system-board operation. When hot-socketing, Stratix II devices may have a minimal effect on the signal integrity of the backplane.

You can power up or power down the V_{CCIO}, V_{CCINT}, and V_{CCPD} pins in any sequence. The power supply ramp rates can range from 100 µs to 100 ms. All V_{CC} supplies must power down within 100 ms of each other to prevent I/O pins from driving out. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF. Stratix II devices meet the following hot socketing specification.

- The hot socketing DC specification is: $| I_{IOPIN} | < 300$ µA.
- The hot socketing AC specification is: $| I_{IOPIN} | < 8$ mA for 10 ns or less.

Table 5–2. Maximum Duty Cycles in Voltage Transitions				
Symbol	**Parameter**	**Condition**	**Maximum Duty Cycles**	**Unit**
V_I	Maximum duty cycles in voltage transitions	V_I = 4.0 V	100	%
		V_I = 4.1 V	90	%
		V_I = 4.2 V	50	%
		V_I = 4.3 V	30	%
		V_I = 4.4 V	17	%
		V_I = 4.5 V	10	%

Recommended Operating Conditions

Table 5–3 contains the Stratix II device family recommended operating conditions.

Table 5–3. Stratix II Device Recommended Operating Conditions (Part 1 of 2) Note (1)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
V_{CCINT}	Supply voltage for internal logic	100 µs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCIO}	Supply voltage for input and output buffers, 3.3-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*, *(6)*	3.135 (3.00)	3.465 (3.60)	V
	Supply voltage for input and output buffers, 2.5-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	2.375	2.625	V
	Supply voltage for input and output buffers, 1.8-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	1.425	1.575	V
	Supply voltage for input and output buffers, 1.2-V operation	100 µs ≤ risetime ≤ 100 ms *(3)*	1.14	1.26	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers.	100 µs ≤ risetime ≤ 100 ms *(4)*	3.135	3.465	V
V_{CCA}	Analog power supply for PLLs	100 µs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_{CCD}	Digital power supply for PLLs	100 µs ≤ risetime ≤ 100 ms *(3)*	1.15	1.25	V
V_I	Input voltage (see Table 5–2)	*(2)*, *(5)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V

Table 5–23. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 5–23:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–24. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 5–24:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–30. Series On-Chip Termination Specification for Top & Bottom I/O Banks (Part 2 of 2)
Notes (1), 2

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_T 2.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
25-Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_T 1.8	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±10	±15	%
50–Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
50-Ω R_T 1.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±10	±15	%
50–Ω R_S 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_T 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±10	±15	%

Notes for Table 5–30:
(1) The resistance tolerances for calibrated SOCT and POCT are for the moment of calibration. If the temperature or voltage changes over time, the tolerance may also change.
(2) On-chip parallel termination with calibration is only supported for input pins.

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 3 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
1.8 V	2 mA	t_{OP}	1042	1093	2904	3048	3338	3472	ps
		t_{DIP}	1062	1115	2970	3118	3414	3562	ps
	4 mA	t_{OP}	1047	1098	2248	2359	2584	2698	ps
		t_{DIP}	1067	1120	2314	2429	2660	2788	ps
	6 mA	t_{OP}	974	1022	2024	2124	2326	2434	ps
		t_{DIP}	994	1044	2090	2194	2402	2524	ps
	8 mA	t_{OP}	976	1024	1947	2043	2238	2343	ps
		t_{DIP}	996	1046	2013	2113	2314	2433	ps
	10 mA	t_{OP}	933	978	1882	1975	2163	2266	ps
		t_{DIP}	953	1000	1948	2045	2239	2356	ps
	12 mA (1)	t_{OP}	934	979	1833	1923	2107	2209	ps
		t_{DIP}	954	1001	1899	1993	2183	2299	ps
1.5 V	2 mA	t_{OP}	1023	1073	2505	2629	2879	3002	ps
		t_{DIP}	1043	1095	2571	2699	2955	3092	ps
	4 mA	t_{OP}	963	1009	2023	2123	2325	2433	ps
		t_{DIP}	983	1031	2089	2193	2401	2523	ps
	6 mA	t_{OP}	966	1012	1923	2018	2210	2315	ps
		t_{DIP}	986	1034	1989	2088	2286	2405	ps
	8 mA (1)	t_{OP}	926	971	1878	1970	2158	2262	ps
		t_{DIP}	946	993	1944	2040	2234	2352	ps
SSTL-2 Class I	8 mA	t_{OP}	913	957	1715	1799	1971	2041	ps
		t_{DIP}	933	979	1781	1869	2047	2131	ps
	12 mA (1)	t_{OP}	896	940	1672	1754	1921	1991	ps
		t_{DIP}	916	962	1738	1824	1997	2081	ps
SSTL-2 Class II	16 mA	t_{OP}	876	918	1609	1688	1849	1918	ps
		t_{DIP}	896	940	1675	1758	1925	2008	ps
	20 mA	t_{OP}	877	919	1598	1676	1836	1905	ps
		t_{DIP}	897	941	1664	1746	1912	1995	ps
	24 mA (1)	t_{OP}	872	915	1596	1674	1834	1903	ps
		t_{DIP}	892	937	1662	1744	1910	1993	ps

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 2 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class I	4 mA	200	150	150	200	150	150	200	150	150
	6 mA	350	250	200	350	250	200	350	250	200
	8 mA	450	300	300	450	300	300	450	300	300
	10 mA	500	400	400	500	400	400	500	400	400
	12 mA	700	550	400	-	-	-	650	550	400
SSTL-18 Class II	8 mA	200	200	150	-	-	-	200	200	150
	16 mA	400	350	350	-	-	-	400	350	350
	18 mA	450	400	400	-	-	-	450	400	400
	20 mA	550	500	450	-	-	-	550	500	450
1.8-V HSTL Class I	4 mA	300	300	300	300	300	300	300	300	300
	6 mA	500	450	450	500	450	450	500	450	450
	8 mA	650	600	600	650	600	600	650	600	600
	10 mA	700	650	600	700	650	600	700	650	600
	12 mA	700	700	650	700	700	650	700	700	650
1.8-V HSTL Class II	16 mA	500	500	450	-	-	-	500	500	450
	18 mA	550	500	500	-	-	-	550	500	500
	20 mA	650	550	550	-	-	-	550	550	550
1.5-V HSTL Class I	4 mA	350	300	300	350	300	300	350	300	300
	6 mA	500	500	450	500	500	450	500	500	450
	8 mA	700	650	600	700	650	600	700	650	600
	10 mA	700	700	650	-	-	-	700	700	650
	12 mA	700	700	700	-	-	-	700	700	700
1.5-V HSTL Class II	16 mA	600	600	550	-	-	-	600	600	550
	18 mA	650	600	600	-	-	-	650	600	600
	20 mA	700	650	600	-	-	-	700	650	600
Differential SSTL-2 Class I *(3)*	8 mA	400	300	300	400	300	300	400	300	300
	12 mA	400	400	350	400	400	350	400	400	350
Differential SSTL-2 Class II *(3)*	16 mA	350	350	300	350	350	300	350	350	300
	20 mA	400	350	350	350	350	297	400	350	350
	24 mA	400	400	350	-	-	-	400	400	350

Table 5–79. Maximum Output Clock Toggle Rate Derating Factors (Part 3 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
1.8-V HSTL Class I	4 mA	245	282	282	245	282	282	229	282	282
	6 mA	164	188	188	164	188	188	153	188	188
	8 mA	123	140	140	123	140	140	114	140	140
	10 mA	110	124	124	110	124	124	108	124	124
	12 mA	97	110	110	97	110	110	104	110	110
1.8-V HSTL Class II	16 mA	101	104	104	-	-	-	99	104	104
	18 mA	98	102	102	-	-	-	93	102	102
	20 mA	93	99	99	-	-	-	88	99	99
1.5-V HSTL Class I	4 mA	168	196	196	168	196	196	188	196	196
	6 mA	112	131	131	112	131	131	125	131	131
	8 mA	84	99	99	84	99	99	95	99	99
	10 mA	87	98	98	-	-	-	90	98	98
	12 mA	86	98	98	-	-	-	87	98	98
1.5-V HSTL Class II	16 mA	95	101	101	-	-	-	96	101	101
	18 mA	95	100	100	-	-	-	101	100	100
	20 mA	94	101	101	-	-	-	104	101	101
Differential SSTL-2 Class II *(3)*	8 mA	364	680	680	-	-	-	350	680	680
	12 mA	163	207	207	-	-	-	188	207	207
	16 mA	118	147	147	-	-	-	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116

Therefore, the DCD percentage for the 267 MHz SSTL-2 Class II non-DDIO row output clock on a –3 device ranges from 47.5% to 52.5%.

Table 5–81. Maximum DCD for Non-DDIO Output on Column I/O Pins *Note (1)*

Column I/O Output Standard I/O Standard	Maximum DCD for Non-DDIO Output		Unit
	-3 Devices	-4 & -5 Devices	
3.3-V LVTTL	190	220	ps
3.3-V LVCMOS	140	175	ps
2.5 V	125	155	ps
1.8 V	80	110	ps
1.5-V LVCMOS	185	215	ps
SSTL-2 Class I	105	135	ps
SSTL-2 Class II	100	130	ps
SSTL-18 Class I	90	115	ps
SSTL-18 Class II	70	100	ps
1.8-V HSTL Class I	80	110	ps
1.8-V HSTL Class II	80	110	ps
1.5-V HSTL Class I	85	115	ps
1.5-V HSTL Class II	50	80	ps
1.2-V HSTL *(2)*	170	-	ps
LVPECL	55	80	ps

Notes to Table 5–81:
(1) The DCD specification is based on a no logic array noise condition.
(2) 1.2-V HSTL is only supported in -3 devices.

Table 5–102 shows the JTAG timing parameters and values for Stratix II devices.

Table 5–102. Stratix II JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	30		ns
t_{JCH}	TCK clock high time	13		ns
t_{JCL}	TCK clock low time	13		ns
t_{JPSU}	JTAG port setup time	3		ns
t_{JPH}	JTAG port hold time	5		ns
t_{JPCO}	JTAG port clock to output		11 *(1)*	ns
t_{JPZX}	JTAG port high impedance to valid output		14 *(1)*	ns
t_{JPXZ}	JTAG port valid output to high impedance		14 *(1)*	ns

Note to Table 5–102:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.3 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

Document Revision History

Table 5–103 shows the revision history for this chapter.

Table 5–103. Document Revision History (Part 1 of 3)

Date and Document Version	Changes Made	Summary of Changes
April 2011, v4.5	Updated Table 5–3.	Added operating junction temperature for military use.
July 2009, v4.4	Updated Table 5–92.	Updated the spread spectrum modulation frequency (f_{SS}) from (100 kHz–500 kHz) to (30 kHz–150 kHz).
May 2007, v4.3	• Updated R_{CONF} in Table 5–4. • Updated f_{IN} (min) in Table 5–92. • Updated f_{IN} and f_{INPFD} in Table 5–93.	—
	Moved the Document Revision History section to the end of the chapter.	—