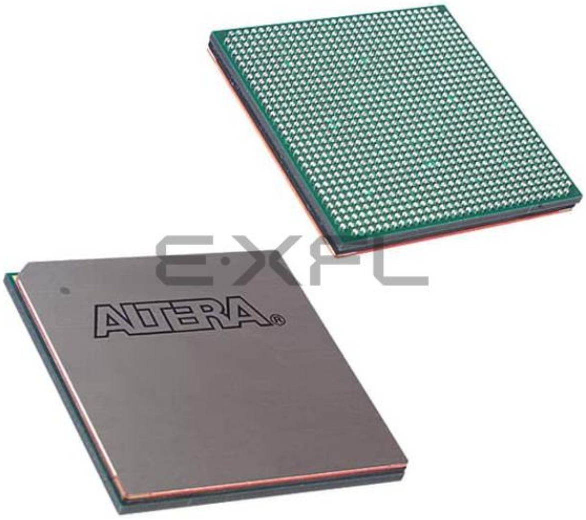

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

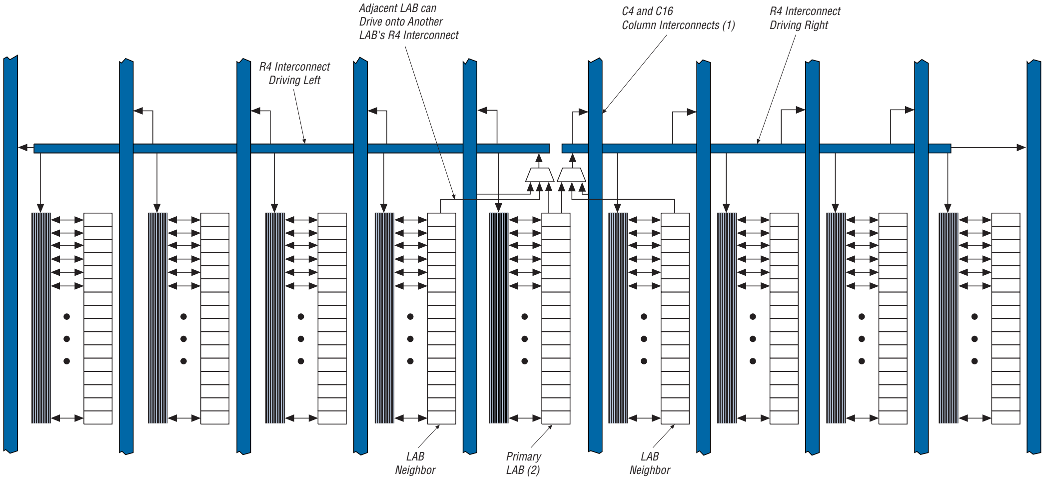
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520488
Number of I/O	758
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s90f1020i4

The direct link interconnect allows an LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself. This provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–16 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

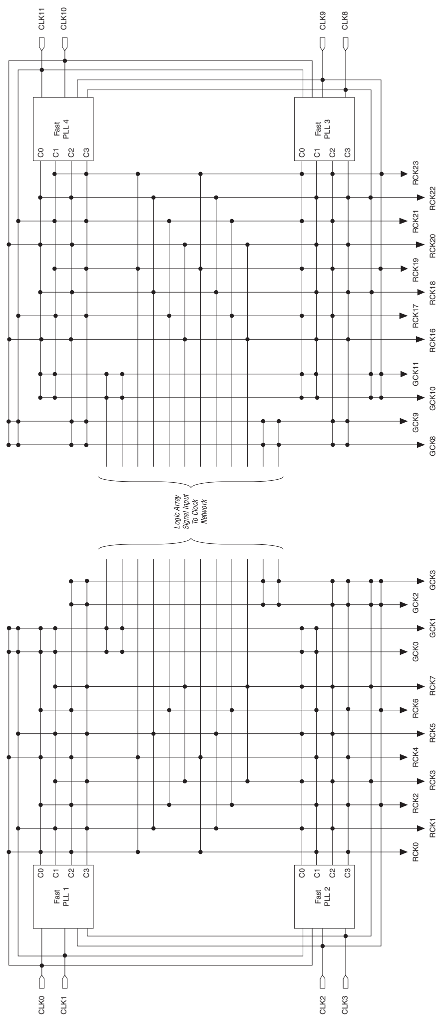
Figure 2–16. R4 Interconnect Connections *Notes (1), (2), (3)*



Notes to Figure 2–16:

(1) C4 and C16 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every LAB in the LAB row.
(3) The LABs in Figure 2–16 show the 16 possible logical outputs per LAB.

Figure 2–41. Global & Regional Clock Connections from Center Clock Pins & Fast PLL Outputs *Note (1)*



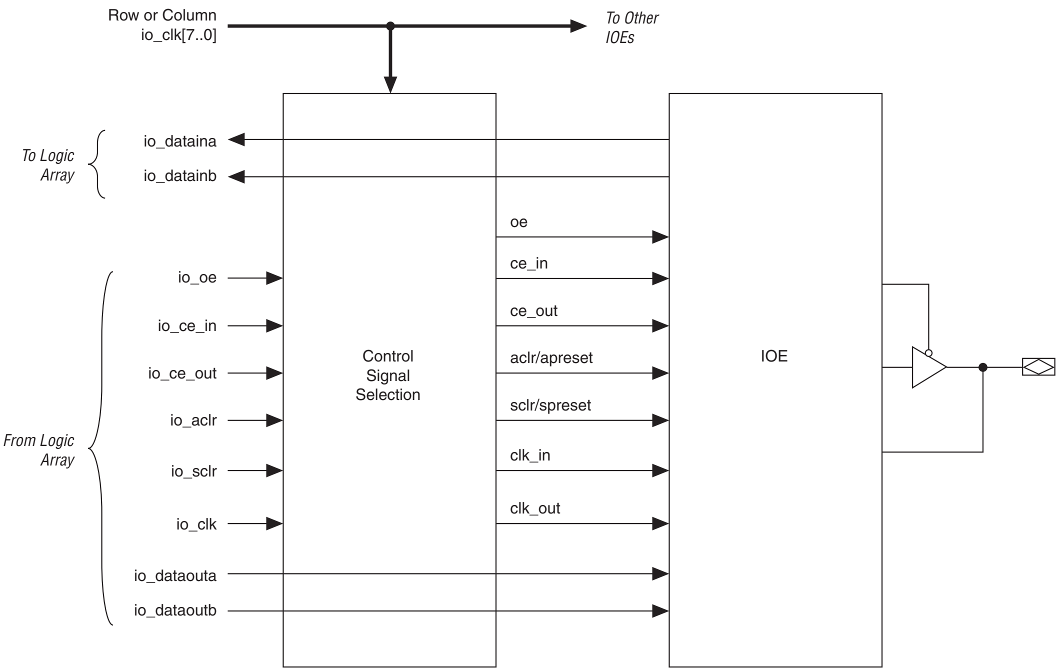
Notes to Figure 2–41:

(1) EP2S15 and EP2S30 devices only have four fast PLLs (1, 2, 3, and 4), but the connectivity from these four PLLs to the global and regional clock networks remains the same as shown.

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

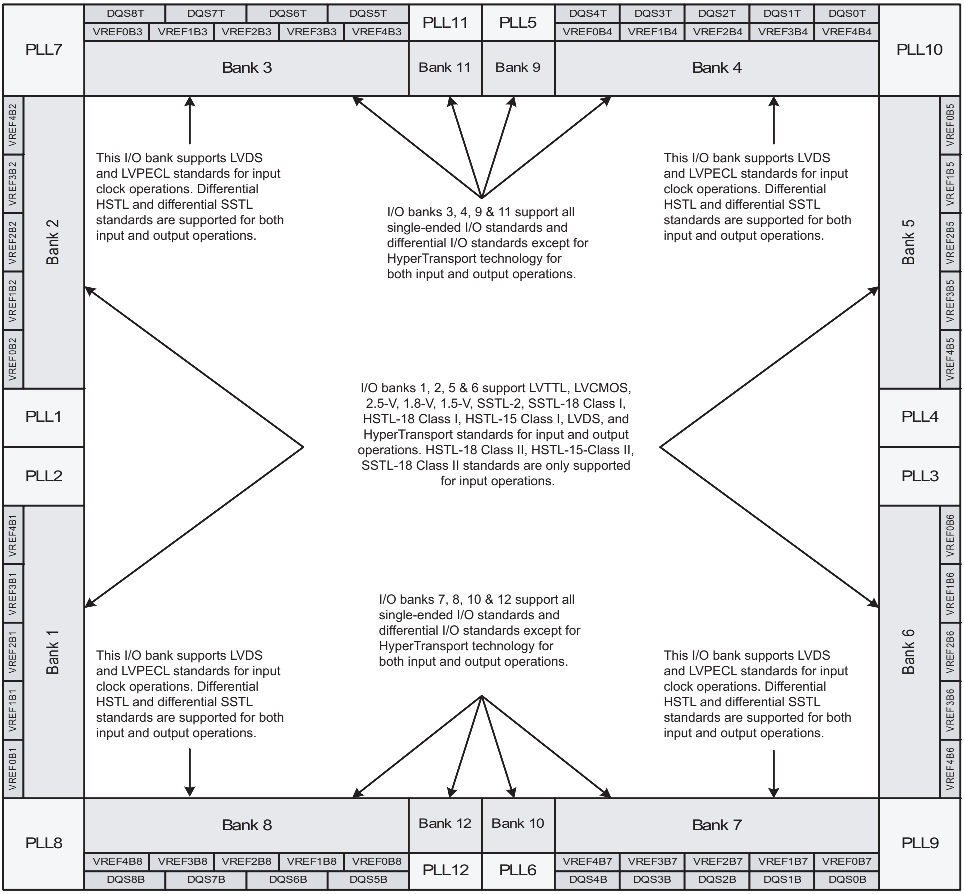
There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks (see the "PLLs & Clock Networks" section). Figure 2–49 illustrates the signal paths through the I/O block.

Figure 2–49. Signal Path through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–50 illustrates the control signal selection.

Figure 2–57. Stratix II I/O Banks *Notes (1), (2), (3), (4)*



Notes to Figure 2–57:

(1) Figure 2–57 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks. These PLL banks utilize the adjacent V_{REF} group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at VREFB7 is the reference voltage level for the SSTL input.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high speed differential I/O standards. See the *High Speed Differential I/O Interfaces in Stratix II & Stratix II GX Devices* chapter of the *Stratix II Device Handbook, Volume 2* or the *Stratix II GX Device Handbook, Volume 2* for more information on differential I/O standards.

Differential On-Chip Termination

Stratix II devices support internal differential termination with a nominal resistance value of 100 Ω for LVDS or HyperTransport technology input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates as shown in the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

For more information on tolerance specifications for differential on-chip termination, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook.*

On-Chip Series Termination Without Calibration

Stratix II devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Stratix II devices support on-chip series termination for single-ended I/O standards with typical R_S values of 25 and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–17 shows the list of output standards that support on-chip series termination without calibration.

On-Chip Series Termination with Calibration

Stratix II devices support on-chip series termination with calibration in column I/O pins in top and bottom banks. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip series termination calibration circuit compares the total impedance of each I/O buffer to the external 25- or 50-Ω resistors connected to the `RUP` and `RDN` pins, and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

For more information on series on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

For more information on tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*.

On-Chip Parallel Termination with Calibration

Stratix II devices support on-chip parallel termination with calibration for column I/O pins only. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip parallel termination calibration circuit compares the total impedance of each I/O buffer to the external 50-Ω resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

On-chip parallel termination with calibration is only supported for input pins.

For more information on on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

For more information on tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook.*

MultiVolt I/O Interface

The Stratix II architecture supports the MultiVolt I/O interface feature that allows Stratix II devices in all packages to interface with systems of different supply voltages.

The Stratix II `VCCINT` pins must always be connected to a 1.2-V power supply. With a 1.2-V V_{CCINT} level, input pins are 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The `VCCIO` pins can be connected to either a 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when `VCCIO` pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems).

The Stratix II `VCCPD` power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The `VCCPD` pins also power configuration input pins and JTAG input pins.

device, PLL 1 can drive a maximum of 10 transmitter channels in I/O bank 1 or a maximum of 19 transmitter channels in I/O banks 1 and 2. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

Table 2–21. EP2S15 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21

Table 2–22. EP2S30 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10
		(3)	19	19	19	19
	Receiver	42 *(2)*	11	10	10	11
		(3)	21	21	21	21
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16
		(3)	29	29	29	29
	Receiver	62 *(2)*	17	14	14	17
		(3)	31	31	31	31

Table 2–25. EP2S130 Differential Channels *Note (1)*										
Package	**Transmitter/ Receiver**	**Total Channels**	**Center Fast PLLs**				**Corner Fast PLLs** *(4)*			
			PLL 1	**PLL 2**	**PLL 3**	**PLL 4**	**PLL 7**	**PLL 8**	**PLL 9**	**PLL 10**
780-pin FineLine BGA	Transmitter	64 *(2)*	16	16	16	16	-	-	-	
		(3)	32	32	32	32	-	-	-	-
	Receiver	68 *(2)*	17	17	17	17	-	-	-	-
		(3)	34	34	34	34	-	-	-	
1,020-pin FineLine BGA	Transmitter	88 *(2)*	22	22	22	22	22	22	22	22
		(3)	44	44	44	44	-	-	-	-
	Receiver	92 *(2)*	23	23	23	23	23	23	23	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-
	Receiver	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-

Table 2–26. EP2S180 Differential Channels *Note (1)*										
Package	**Transmitter/ Receiver**	**Total Channels**	**Center Fast PLLs**				**Corner Fast PLLs** *(4)*			
			PLL 1	**PLL 2**	**PLL 3**	**PLL 4**	**PLL 7**	**PLL 8**	**PLL 9**	**PLL 10**
1,020-pin FineLine BGA	Transmitter	88 *(2)*	22	22	22	22	22	22	22	22
		(3)	44	44	44	44	-	-	-	-
	Receiver	92 *(2)*	23	23	23	23	23	23	23	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-
	Receiver	156 *(2)*	37	41	41	37	37	41	41	37
		(3)	78	78	78	78	-	-	-	-

Notes to Tables 2–21 to 2–26:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

(2) This is the maximum number of channels the PLLs can directly drive.

(3) This is the maximum number of channels if the device uses cross bank channels from the adjacent center PLL.

(4) The channels accessible by the center fast PLL overlap with the channels accessible by the corner fast PLL. Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1, 2, 3, and 4 with the number of channels accessible by PLLs 7, 8, 9, and 10.

you need to support configuration input voltages of 1.8 V/1.5 V, you should set the VCCSEL to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.

For more information on multi-volt support, including information on using TDO and nCEO in multi-volt systems, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Configuration Schemes

You can load the configuration data for a Stratix II device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II device. A configuration device can automatically configure a Stratix II device at system power-up.

You can configure multiple Stratix II devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Stratix II FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect your designs
- Remote system upgrades for remotely updating your Stratix II designs

Table 3–5 summarizes which configuration features can be used in each configuration scheme.

Table 3–5. Stratix II Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ *(1)*	✓ *(1)*	✓
	Enhanced configuration device		✓ *(2)*	✓
AS	Serial configuration device	✓	✓	✓ *(3)*
PS	MAX II device or microprocessor and flash device	✓	✓	✓
	Enhanced configuration device	✓	✓	✓
	Download cable *(4)*	✓	✓	

Table 3–5. Stratix II Configuration Features (Part 2 of 2)

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
PPA	MAX II device or microprocessor and flash device			✓
JTAG	Download cable *(4)*			
	MAX II device or microprocessor and flash device			

Notes for Table 3–5:

(1) In these modes, the host system must send a DCLK that is 4× the data rate.
(2) The enhanced configuration device decompression feature is available, while the Stratix II decompression feature is not available.
(3) Only remote update mode is supported when using the AS configuration scheme. Local update mode is not supported.
(4) The supported download cables include the Altera USB Blaster universal serial bus (USB) port download cable, MasterBlaster serial/USB communications cable, ByteBlaster II parallel port download cable, and the ByteBlasterMV parallel port download cable.

See the *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information about configuration schemes in Stratix II and Stratix II GX devices.

Device Security Using Configuration Bitstream Encryption

Stratix II FPGAs are the industry's first FPGAs with the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm. When using the design security feature, a 128-bit security key is stored in the Stratix II FPGA. To successfully configure a Stratix II FPGA that has the design security feature enabled, it must be configured with a configuration file that was encrypted using the same 128-bit security key. The security key can be stored in non-volatile memory inside the Stratix II device. This non-volatile memory does not require any external devices, such as a battery back-up, for storage.

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Unit
I_{CCI00}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25° C	EP2S15		4.0	*(3)*	mA
			EP2S30		4.0	*(3)*	mA
			EP2S60		4.0	*(3)*	mA
			EP2S90		4.0	*(3)*	mA
			EP2S130		4.0	*(3)*	mA
			EP2S180		4.0	*(3)*	mA
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	Vi = 0; V_{CCIO} = 3.3 V		10	25	50	kΩ
		Vi = 0; V_{CCIO} = 2.5 V		15	35	70	kΩ
		Vi = 0; V_{CCIO} = 1.8 V		30	50	100	kΩ
		Vi = 0; V_{CCIO} = 1.5 V		40	75	150	kΩ
		Vi = 0; V_{CCIO} = 1.2 V		50	90	170	kΩ
	Recommended value of I/O pin external pull-down resistor before and during configuration				1	2	kΩ

Table 5–4. Stratix II Device DC Operating Conditions (Part 2 of 2) *Note (1)*

Notes to Table 5–4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) Maximum values depend on the actual T_J and design utilization. See the Excel-based PowerPlay Early Power Estimator (available at **www.altera.com**) or the Quartus II PowerPlay Power Analyzer feature for maximum values. See the section "Power Consumption" on page 5–20 for more information.

(4) Pin pull-up resistance values are lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 5–5 through 5–32 show the Stratix II device family I/O standard specifications.

Table 5–5. LVTTL Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4		V

Table 5–10. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.500	2.625	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125		1.375	V
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

Table 5–11. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)		3.135	3.300	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840		1,570	mV
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

Note to Table 5–11:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by `VCC_PLL_OUT`. For differential clock output/feedback operation, `VCC_PLL_OUT` should be connected to 3.3 V.

Table 5–21. SSTL-2 Class I & II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.500	2.625	V
V_{SWING} (DC)	DC differential input voltage		0.36			V
V_X (AC)	AC differential input cross point voltage		$(V_{CCIO}/2) - 0.2$		$(V_{CCIO}/2) + 0.2$	V
V_{SWING} (AC)	AC differential input voltage		0.7			V
V_{ISO}	Input clock signal offset voltage			$0.5 \times V_{CCIO}$		V
ΔV_{ISO}	Input clock signal offset voltage variation			±200		mV
V_{OX} (AC)	AC differential output cross point voltage		$(V_{CCIO}/2) - 0.2$		$(V_{CCIO}/2) + 0.2$	V

Table 5–22. 1.2-V HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.14	1.20	1.26	V
V_{REF}	Reference voltage		$0.48 \times V_{CCIO}$	$0.50 \times V_{CCIO}$	$0.52 \times V_{CCIO}$	V
V_{IH} (DC)	High-level DC input voltage		$V_{REF} + 0.08$		$V_{CCIO} + 0.15$	V
V_{IL} (DC)	Low-level DC input voltage		–0.15		$V_{REF} - 0.08$	V
V_{IH} (AC)	High-level AC input voltage		$V_{REF} + 0.15$		$V_{CCIO} + 0.24$	V
V_{IL} (AC)	Low-level AC input voltage		–0.24		$V_{REF} - 0.15$	V
V_{OH}	High-level output voltage	$I_{OH} = 8$ mA	$V_{REF} + 0.15$		$V_{CCIO} + 0.15$	V
V_{OL}	Low-level output voltage	$I_{OH} = -8$ mA	–0.15		$V_{REF} - 0.15$	V

Table 5–23. 1.5-V HSTL Class I Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 5–23:

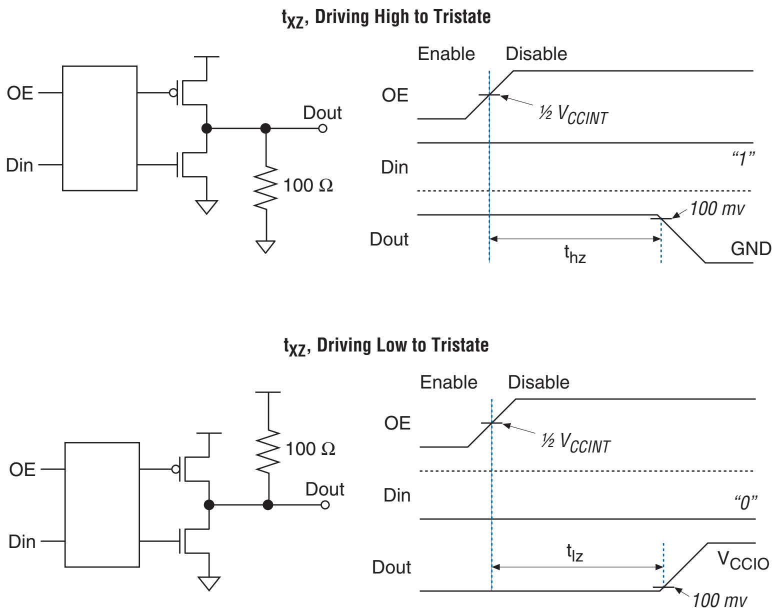
(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Table 5–24. 1.5-V HSTL Class II Specifications						
Symbol	**Parameter**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Unit**
V_{CCIO}	Output supply voltage		1.425	1.500	1.575	V
V_{REF}	Input reference voltage		0.713	0.750	0.788	V
V_{TT}	Termination voltage		0.713	0.750	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 5–24:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

Figure 5–5. Measurement Setup for t_{xz} *Note (1)*



Note to Figure 5–5:

(1) V_{CCINT} is 1.12 V for this measurement.

Table 5–73. Stratix II I/O Input Delay for Column Pins (Part 2 of 3)								
I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.5-V HSTL Class II	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps
1.8-V HSTL Class I	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.8-V HSTL Class II	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
PCI	t_{PI}	679	712	1214	1273	1395	1625	ps
	t_{PCOUT}	413	433	778	816	894	1042	ps
PCI-X	t_{PI}	679	712	1214	1273	1395	1625	ps
	t_{PCOUT}	413	433	778	816	894	1042	ps
Differential SSTL-2 Class I *(1)*	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
Differential SSTL-2 Class II *(1)*	t_{PI}	507	530	818	857	939	1094	ps
	t_{PCOUT}	241	251	382	400	438	511	ps
Differential SSTL-18 Class I *(1)*	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
Differential SSTL-18 Class II *(1)*	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.8-V Differential HSTL Class I *(1)*	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.8-V Differential HSTL Class II *(1)*	t_{PI}	543	569	898	941	1031	1201	ps
	t_{PCOUT}	277	290	462	484	530	618	ps
1.5-V Differential HSTL Class I *(1)*	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps
1.5-V Differential HSTL Class II *(1)*	t_{PI}	560	587	993	1041	1141	1329	ps
	t_{PCOUT}	294	308	557	584	640	746	ps

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 2 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class I	4 mA	200	150	150	200	150	150	200	150	150
	6 mA	350	250	200	350	250	200	350	250	200
	8 mA	450	300	300	450	300	300	450	300	300
	10 mA	500	400	400	500	400	400	500	400	400
	12 mA	700	550	400	-	-	-	650	550	400
SSTL-18 Class II	8 mA	200	200	150	-	-	-	200	200	150
	16 mA	400	350	350	-	-	-	400	350	350
	18 mA	450	400	400	-	-	-	450	400	400
	20 mA	550	500	450	-	-	-	550	500	450
1.8-V HSTL Class I	4 mA	300	300	300	300	300	300	300	300	300
	6 mA	500	450	450	500	450	450	500	450	450
	8 mA	650	600	600	650	600	600	650	600	600
	10 mA	700	650	600	700	650	600	700	650	600
	12 mA	700	700	650	700	700	650	700	700	650
1.8-V HSTL Class II	16 mA	500	500	450	-	-	-	500	500	450
	18 mA	550	500	500	-	-	-	550	500	500
	20 mA	650	550	550	-	-	-	550	550	550
1.5-V HSTL Class I	4 mA	350	300	300	350	300	300	350	300	300
	6 mA	500	500	450	500	500	450	500	500	450
	8 mA	700	650	600	700	650	600	700	650	600
	10 mA	700	700	650	-	-	-	700	700	650
	12 mA	700	700	700	-	-	-	700	700	700
1.5-V HSTL Class II	16 mA	600	600	550	-	-	-	600	600	550
	18 mA	650	600	600	-	-	-	650	600	600
	20 mA	700	650	600	-	-	-	700	650	600
Differential SSTL-2 Class I *(3)*	8 mA	400	300	300	400	300	300	400	300	300
	12 mA	400	400	350	400	400	350	400	400	350
Differential SSTL-2 Class II *(3)*	16 mA	350	350	300	350	350	300	350	350	300
	20 mA	400	350	350	350	350	297	400	350	350
	24 mA	400	400	350	-	-	-	400	400	350

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 3 of 5) Note (1)

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
Differential SSTL-18 Class I (3)	4 mA	200	150	150	200	150	150	200	150	150
	6 mA	350	250	200	350	250	200	350	250	200
	8 mA	450	300	300	450	300	300	450	300	300
	10 mA	500	400	400	500	400	400	500	400	400
	12 mA	700	550	400	350	350	297	650	550	400
Differential SSTL-18 Class II (3)	8 mA	200	200	150	-	-	-	200	200	150
	16 mA	400	350	350	-	-	-	400	350	350
	18 mA	450	400	400	-	-	-	450	400	400
	20 mA	550	500	450	-	-	-	550	500	450
1.8-V Differential HSTL Class I (3)	4 mA	300	300	300	-	-	-	300	300	300
	6 mA	500	450	450	-	-	-	500	450	450
	8 mA	650	600	600	-	-	-	650	600	600
	10 mA	700	650	600	-	-	-	700	650	600
	12 mA	700	700	650	-	-	-	700	700	650
1.8-V Differential HSTL Class II (3)	16 mA	500	500	450	-	-	-	500	500	450
	18 mA	550	500	500	-	-	-	550	500	500
	20 mA	650	550	550	-	-	-	550	550	550
1.5-V Differential HSTL Class I (3)	4 mA	350	300	300	-	-	-	350	300	300
	6 mA	500	500	450	-	-	-	500	500	450
	8 mA	700	650	600	-	-	-	700	650	600
	10 mA	700	700	650	-	-	-	700	700	650
	12 mA	700	700	700	-	-	-	700	700	700
1.5-V Differential HSTL Class II (3)	16 mA	600	600	550	-	-	-	600	600	550
	18 mA	650	600	600	-	-	-	650	600	600
	20 mA	700	650	600	-	-	-	700	650	600
3.3-V PCI		1,000	790	670	-	-	-	1,000	790	670
3.3-V PCI-X		1,000	790	670	-	-	-	1,000	790	670
LVDS (6)		-	-	-	500	500	500	450	400	300
HyperTransport technology (4), (6)					500	500	500	-	-	-
LVPECL (5)		-	-	-	-	-	-	450	400	300
3.3-V LVTTL	OCT 50 Ω	400	400	350	400	400	350	400	400	350
2.5-V LVTTL	OCT 50 Ω	350	350	300	350	350	300	350	350	300

Table 5–93. Fast PLL Specifications

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (for -3 and -4 speed grade devices)	16.08		717	MHz
	Input clock frequency (for -5 speed grade devices)	16.08		640	MHz
f_{INPFD}	Input frequency to the PFD	16.08		500	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤ 2 MHz		0.5		ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 2 MHz		1.0		ns (p-p)
f_{VCO}	Upper VCO frequency range for –3 and –4 speed grades	300		1,040	MHz
	Upper VCO frequency range for –5 speed grades	300		840	MHz
	Lower VCO frequency range for –3 and –4 speed grades	150		520	MHz
	Lower VCO frequency range for –5 speed grades	150		420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875		550	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
f_{OUT_IO}	PLL clock output frequency to regular I/O pin	4.6875		*(1)*	MHz
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs		$75/f_{SCANCLK}$		ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5.00	28.00	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration		0.03	1.00	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift			±15	ps
t_{ARESET}	Minimum pulse width on `areset` signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the `areset` signal when using PLL reconfiguration. Reset the PLL after `scandone` goes high.	500			ns

Note to Table 5–93:

(1) Limited by I/O f_{MAX}. See Table 5–77 on page 5–67 for the maximum.