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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520488
Number of I/O	902
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s90f1508i4

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Chapter 4. Hot Socketing & Power-On Reset

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2. Stratix II Architecture

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Functional Description

Stratix® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures (M512 RAM, M4K RAM, and M-RAM blocks), and digital signal processing (DSP) blocks.

Each LAB consists of eight adaptive logic modules (ALMs). An ALM is the Stratix II device family's basic building block of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 500 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 550 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 420 MHz. Several M-RAM blocks are located individually in the device's logic array.

DSP blocks can implement up to either eight full-precision 9 × 9-bit multipliers, four full-precision 18 × 18-bit multipliers, or one full-precision 36 × 36-bit multiplier with add or subtract features. The DSP blocks support Q1.15 format rounding and saturation in the multiplier and accumulator stages. These blocks also contain shift registers for digital signal processing applications, including finite impulse response (FIR) and infinite impulse response (IIR) filters. DSP blocks are grouped into columns across the device and operate at up to 450 MHz.

The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 2–1 lists the resources available in Stratix II devices.

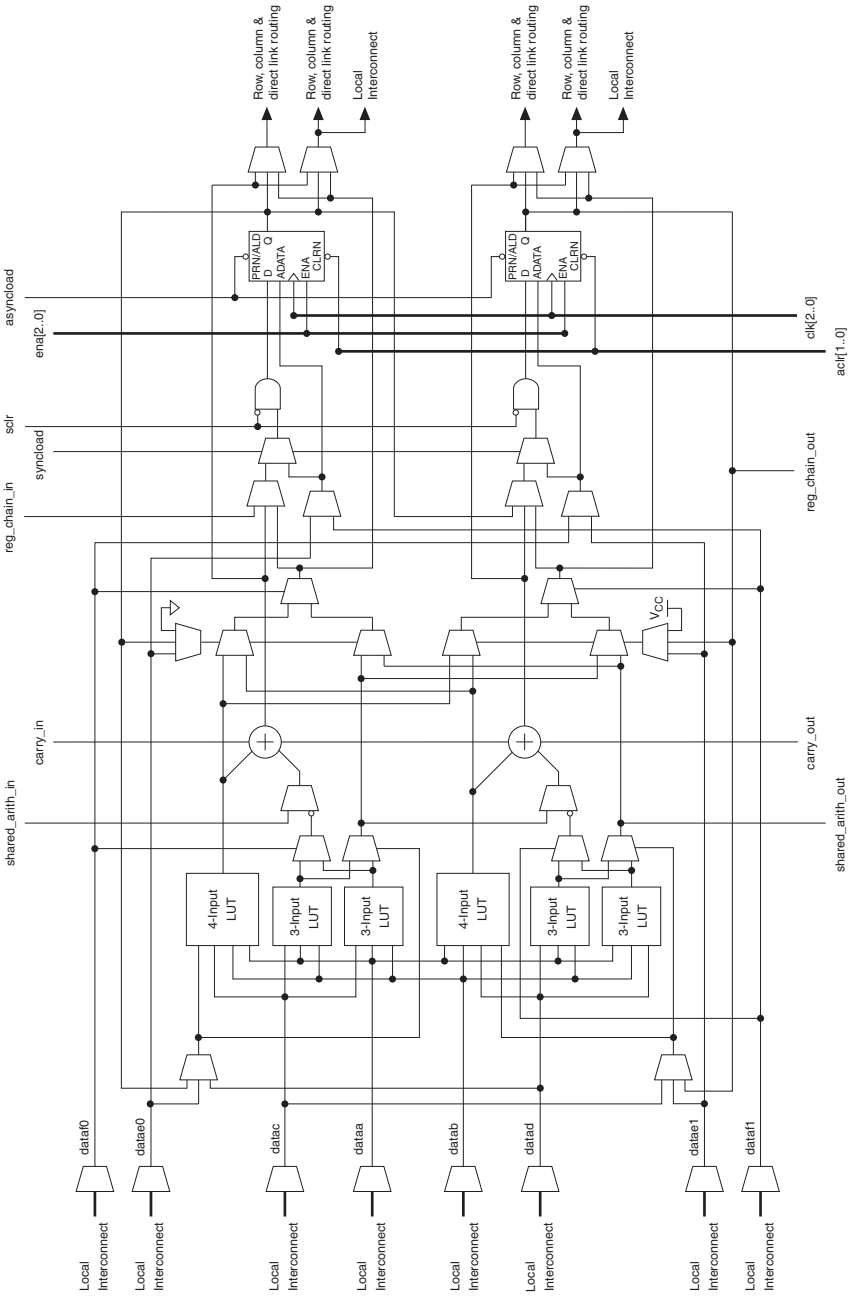
Table 2–1. Stratix II Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP2S15	4 / 104	3 / 78	0	2 / 12	30	26
EP2S30	6 / 202	4 / 144	1	2 / 16	49	36
EP2S60	7 / 329	5 / 255	2	3 / 36	62	51
EP2S90	8 / 488	6 / 408	4	3 / 48	71	68
EP2S130	9 / 699	7 / 609	6	3 / 63	81	87
EP2S180	11 / 930	8 / 768	9	4 / 96	100	96

Logic Array Blocks

Each LAB consists of eight ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in an LAB. The Quartus® II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Figure 2–2 shows the Stratix II LAB structure.

Figure 2–6. Stratix II ALM Details



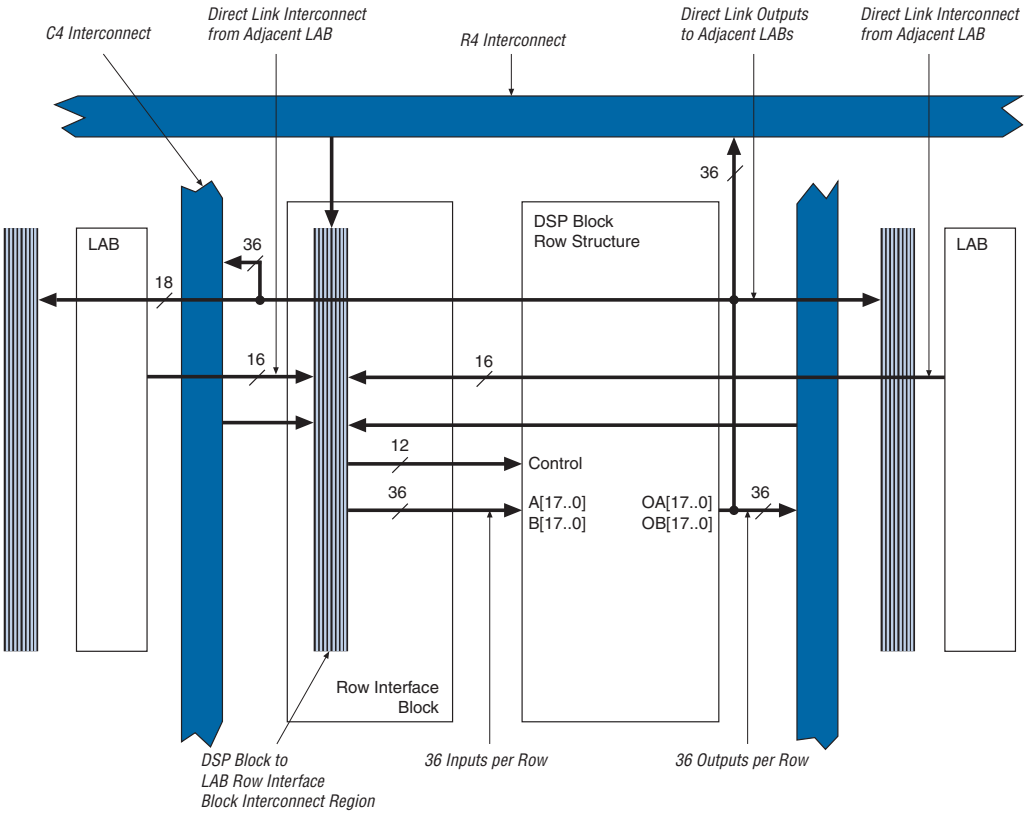
synchronous load, and clock enable control for the register. These LAB-wide signals are available in all ALM modes. See the "LAB Control Signals" section for more information on the LAB-wide control signals.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix II ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–7 shows the supported LUT combinations in normal mode.

Figure 2–30. DSP Block Interface to Interconnect



A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed/unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface.

Table 2–16. Stratix II Supported I/O Standards (Part 2 of 2)

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
SSTL-2 Class I and II	Voltage-referenced	1.25	2.5	1.25

Notes to Table 2–16:

(1) This I/O standard is only available on input and output column clock pins.

(2) This I/O standard is only available on input clock pins and DQS pins in I/O banks 3, 4, 7, and 8, and output clock pins in I/O banks 9,10, 11, and 12.

(3) V_{CCIO} is 3.3 V when using this I/O standard in input and output column clock pins (in I/O banks 9, 10, 11, and 12). The clock input pins supporting LVDS on banks 3, 4, 7, and 8 use V_{CCINT} for LVDS input operations and have no dependency on the V_{CCIO} level of the bank.

(4) 1.2-V HSTL is only supported in I/O banks 4,7, and 8.

For more information on I/O standards supported by Stratix II I/O banks, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

Stratix II devices contain eight I/O banks and four enhanced PLL external clock output banks, as shown in Figure 2–57. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS and HyperTransport inputs and outputs. These banks support all Stratix II I/O standards except PCI or PCI-X I/O pins, and SSTL-18 Class II and HSTL outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, enhanced PLL external clock output banks allow clock output capabilities such as differential support for SSTL and HSTL.

Table 2–23. EP2S60 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
484-pin FineLine BGA	Transmitter	38 *(2)*	10	9	9	10	10	9	9	10
		(3)	19	19	19	19	-	-	-	-
	Receiver	42 *(2)*	11	10	10	11	11	10	10	11
		(3)	21	21	21	21	-	-	-	-
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16	16	13	13	16
		(3)	29	29	29	29	-	-	-	-
	Receiver	62 *(2)*	17	14	14	17	17	14	14	17
		(3)	31	31	31	31	-	-	-	-
1,020-pin FineLine BGA	Transmitter	84 *(2)*	21	21	21	21	21	21	21	21
		(3)	42	42	42	42	-	-	-	-
	Receiver	84 *(2)*	21	21	21	21	21	21	21	21
		(3)	42	42	42	42	-	-	-	-

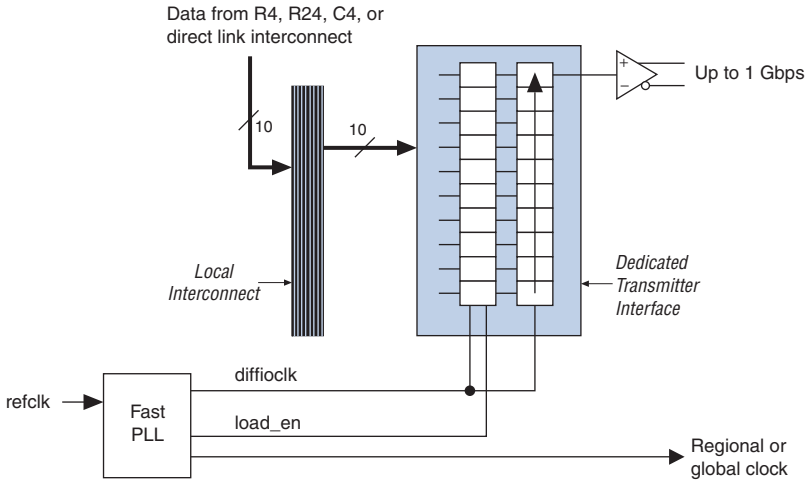
Table 2–24. EP2S90 Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs				Corner Fast PLLs *(4)*			
			PLL 1	PLL 2	PLL 3	PLL 4	PLL 7	PLL 8	PLL 9	PLL 10
484-pin Hybrid FineLine BGA	Transmitter	38 *(2)*	10	9	9	10	-	-	-	-
		(3)	19	19	19	19	-	-	-	-
	Receiver	42 *(2)*	11	10	10	11	-	-	-	-
		(3)	21	21	21	21	-	-	-	-
780-pin FineLine BGA	Transmitter	64 *(2)*	16	16	16	16	-	-	-	
		(3)	32	32	32	32	-	-	-	-
	Receiver	68 *(2)*	17	17	17	17	-	-	-	-
		(3)	34	34	34	34	-	-	-	
1,020-pin FineLine BGA	Transmitter	90 *(2)*	23	22	22	23	23	22	22	23
		(3)	45	45	45	45	-	-	-	-
	Receiver	94 *(2)*	23	24	24	23	23	24	24	23
		(3)	46	46	46	46	-	-	-	-
1,508-pin FineLine BGA	Transmitter	118 *(2)*	30	29	29	30	30	29	29	30
		(3)	59	59	59	59	-	-	-	-
	Receiver	118 *(2)*	30	29	29	30	30	29	29	30
		(3)	59	59	59	59	-	-	-	-

Dedicated Circuitry with DPA Support

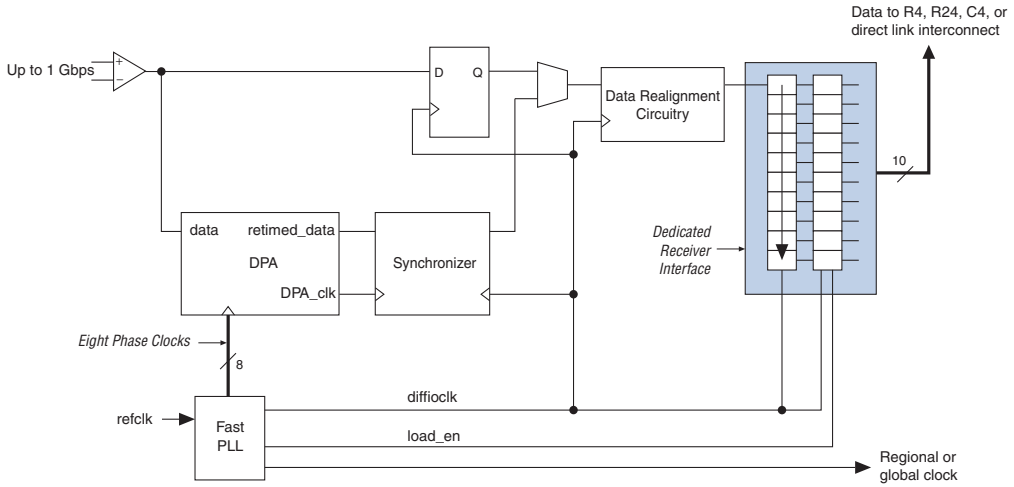
Stratix II devices support source-synchronous interfacing with LVDS or HyperTransport signaling at up to 1 Gbps. Stratix II devices can transmit or receive serial channels along with a low-speed or high-speed clock. The receiving device PLL multiplies the clock by an integer factor W = 1 through 32. For example, a HyperTransport technology application where the data rate is 1,000 Mbps and the clock rate is 500 MHz would require that W be set to 2. The SERDES factor *J* determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor *J* can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these *J* factor values. For a *J* factor of 1, the Stratix II device bypasses the SERDES block. For a *J* factor of 2, the Stratix II device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. Figure 2–58 shows the block diagram of the Stratix II transmitter channel.

Figure 2–58. Stratix II Transmitter Channel



Each Stratix II receiver channel features a DPA block for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel. In addition, you can dynamically switch between using the DPA block or bypassing the block via a control signal from the logic array. Figure 2–59 shows the block diagram of the Stratix II receiver channel.

Figure 2–59. Stratix II Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.

For more information on the fast PLL, see the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

the Device & Pin Options dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Stratix II devices, eliminating the need for external logic. For Stratix II devices, CRC is computed by the device during configuration and checked against an automatically computed CRC during normal operation. The CRC_ERROR pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built in the Stratix II devices to perform error detection automatically. This error detection circuitry in Stratix II devices constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a re-configuration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

In the Quartus II software version 4.1 and later, you can turn on the automated error detection CRC feature in the Device & Pin Options dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

Document Revision History

Table 3–7 shows the revision history for this chapter.

Table 3–7. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.2	Moved Document Revision History section to the end of the chapter.	—
	Updated the "Temperature Sensing Diode (TSD)" section.	—

Table 5–10. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.500	2.625	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125		1.375	V
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

Table 5–11. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)		3.135	3.300	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840		1,570	mV
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

Note to Table 5–11:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, VCC_PLL_OUT should be connected to 3.3 V.

Table 5–12. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage		3.135	3.300	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		300	600	1,000	mV
V_{ICM}	Input common mode voltage		1.0		2.5	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525		970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1,650		2,250	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Note to Table 5–12:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, VCC_PLL_OUT should be connected to 3.3 V.

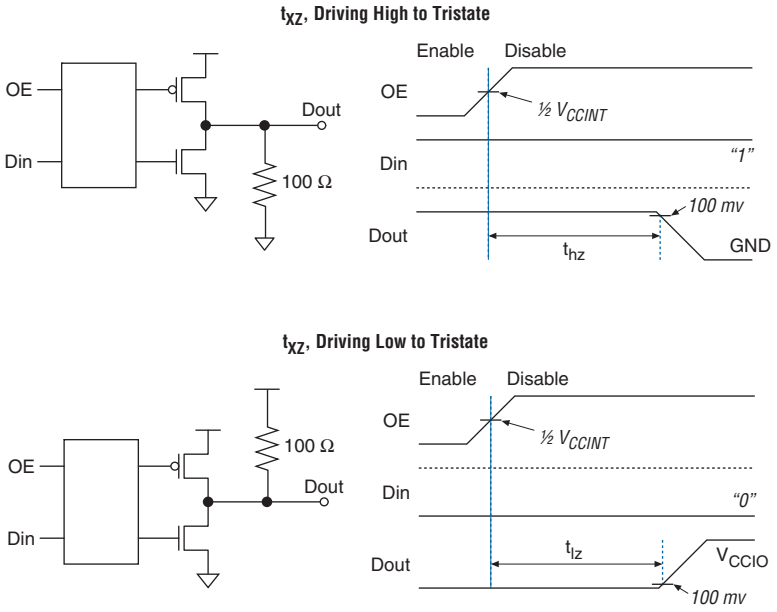
Table 5–13. HyperTransport Technology Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.500	2.625	V
V_{ID}	Input differential voltage swing (single-ended)	R_L = 100 Ω	300	600	900	mV
V_{ICM}	Input common mode voltage	R_L = 100 Ω	385	600	845	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	400	600	820	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			75	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	440	600	780	mV
ΔV_{OCM}	Change in V_{OCM} between high and low	R_L = 100 Ω			50	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Table 5–14. 3.3-V PCI Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V

Figure 5–5. Measurement Setup for t_{xz} *Note (1)*



Note to Figure 5–5:
(1) V_{CCINT} is 1.12 V for this measurement.

Internal Timing Parameters

See Tables 5–37 through 5–42 for internal timing parameters.

Table 5–37. LE_FF Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade *(1)*		-3 Speed Grade *(2)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min *(3)*	Max	Min *(3)*	Max	Min *(4)*	Max	Min *(3)*	Max	
t_{SU}	LE register setup time before clock	90		95		104 104		121		ps
t_{H}	LE register hold time after clock	149		157		172 172		200		ps
t_{CO}	LE register clock-to-output delay	62	94	62	99	59 62	109	62	127	ps
t_{CLR}	Minimum clear pulse width	204		214		234 234		273		ps
t_{PRE}	Minimum preset pulse width	204		214		234 234		273		ps
t_{CLKL}	Minimum clock low time	612		642		703 703		820		ps
t_{CLKH}	Minimum clock high time	612		642		703 703		820		ps
t_{LUT}		162	378	162	397	162 170	435	162	507	ps
t_{ADDER}		354	619	354	650	354 372	712	354	829	ps

Notes to Table 5–37:

(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.

(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

(3) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.

(4) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

Table 5–70. Stratix II IOE Programmable Delay on Row Pins *Note (1)*

Parameter	Paths Affected	Available Settings	Minimum Timing *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade	
			Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)	Min Offset (ps)	Max Offset (ps)
Input delay from pin to internal cells	Pad to I/O dataout to logic array	8	0 0	1,697 1,782	0 0	2,876 3,020	0	3,308	0	3,853
Input delay from pin to input register	Pad to I/O input register	64	0 0	1,956 2,054	0 0	3,270 3,434	0	3,761	0	4,381
Delay from output register to output pin	I/O output register to pad	2	0 0	316 332	0 0	525 525	0	575	0	670
Output enable pin delay	t_{XZ}, t_{ZX}	2	0 0	305 320	0 0	507 507	0	556	0	647

Notes to Table 5–70:

(1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.

(2) The first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

(3) The first number applies to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices. The second number applies to -3 speed grade EP2S130 and EP2S180 devices.

Default Capacitive Loading of Different I/O Standards

See Table 5–71 for default capacitive loading of different I/O standards.

Table 5–71. Default Loading of Different I/O Standards for Stratix II (Part 1 of 2)

I/O Standard	Capacitive Load	Unit
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF
1.8 V	0	pF
1.5 V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL-2 Class I	0	pF

Table 5–74. Stratix II I/O Input Delay for Row Pins (Part 2 of 2)

I/O Standard	Parameter	Minimum Timing		-3 Speed Grade (1)	-3 Speed Grade (2)	-4 Speed Grade	-5 Speed Grade	Unit
		Industrial	Commercial					
1.5-V HSTL Class II	t_{PI}	602	631	1056	1107	1212	1413	ps
	t_{PCOUT}	278	292	529	555	608	708	ps
1.8-V HSTL Class I	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
1.8-V HSTL Class II	t_{PI}	577	605	960	1006	1101	1285	ps
	t_{PCOUT}	253	266	433	454	497	580	ps
LVDS	t_{PI}	515	540	948	994	1088	1269	ps
	t_{PCOUT}	191	201	421	442	484	564	ps
HyperTransport	t_{PI}	515	540	948	994	1088	1269	ps
	t_{PCOUT}	191	201	421	442	484	564	ps

Notes for Table 5–74:
(1) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(2) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.

Table 5–75. Stratix II I/O Output Delay for Column Pins (Part 1 of 8)

I/O Standard	Drive Strength	Parameter	Minimum Timing		-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
			Industrial	Commercial					
LVTTL	4 mA	t_{OP}	1178	1236	2351	2467	2702	2820	ps
		t_{DIP}	1198	1258	2417	2537	2778	2910	ps
	8 mA	t_{OP}	1041	1091	2036	2136	2340	2448	ps
		t_{DIP}	1061	1113	2102	2206	2416	2538	ps
	12 mA	t_{OP}	976	1024	2036	2136	2340	2448	ps
		t_{DIP}	996	1046	2102	2206	2416	2538	ps
	16 mA	t_{OP}	951	998	1893	1986	2176	2279	ps
		t_{DIP}	971	1020	1959	2056	2252	2369	ps
	20 mA	t_{OP}	931	976	1787	1875	2054	2154	ps
		t_{DIP}	951	998	1853	1945	2130	2244	ps
	24 mA (1)	t_{OP}	924	969	1788	1876	2055	2156	ps
		t_{DIP}	944	991	1854	1946	2131	2246	ps

Table 5–93. Fast PLL Specifications

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (for -3 and -4 speed grade devices)	16.08		717	MHz
	Input clock frequency (for -5 speed grade devices)	16.08		640	MHz
f_{INPFD}	Input frequency to the PFD	16.08		500	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤ 2 MHz		0.5		ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 2 MHz		1.0		ns (p-p)
f_{VCO}	Upper VCO frequency range for –3 and –4 speed grades	300		1,040	MHz
	Upper VCO frequency range for –5 speed grades	300		840	MHz
	Lower VCO frequency range for –3 and –4 speed grades	150		520	MHz
	Lower VCO frequency range for –5 speed grades	150		420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875		550	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
f_{OUT_IO}	PLL clock output frequency to regular I/O pin	4.6875		*(1)*	MHz
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs		$75/f_{SCANCLK}$		ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5.00	28.00	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration		0.03	1.00	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift			±15	ps
t_{ARESET}	Minimum pulse width on areset signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500			ns

Note to Table 5–93:
(1) Limited by I/O f_{MAX}. See Table 5–77 on page 5–67 for the maximum.

Table 5–100. DQS Phase Offset Delay Per Stage Notes (1), (2), (3)			
Speed Grade	**Min**	**Max**	**Unit**
-3	9	14	ps
-4	9	14	ps
-5	9	15	ps

Notes to Table 5–100:
(1) The delay settings are linear.
(2) The valid settings for phase offset are -64 to +63 for frequency mode 0 and -32 to +31 for frequency modes 1, 2, and 3.
(3) The typical value equals the average of the minimum and maximum values.

Table 5–101. DDIO Outputs Half-Period Jitter Notes (1), (2)			
Name	**Description**	**Max**	**Unit**
$t_{OUTHALFJITTER}$	Half-period jitter (PLL driving DDIO outputs)	200	ps

Notes to Table 5–101:
(1) The worst-case half period is equal to the ideal half period subtracted by the DCD and half-period jitter values.
(2) The half-period jitter was characterized using a PLL driving DDIO outputs.

JTAG Timing Specifications

Figure 5–10 shows the timing requirements for the JTAG signals.

Figure 5–10. Stratix II JTAG Waveforms