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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520488
Number of I/O	902
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2s90f1508i4n

Chapter 3. Configuration & Testing

Chapter 4. Hot Socketing & Power-On Reset

Chapter 5. DC & Switching Characteristics

Stratix II devices are available in space-saving FineLine BGA® packages (see Tables 1–2 and 1–3).

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 *(3)*	334		492		718	
EP2S90 *(3)*		308		534	758	902
EP2S130 *(3)*				534	742	1,126
EP2S180 *(3)*					742	1,170

Notes to Table 1–2:

(1) All I/O pin counts include eight dedicated clock input pins (`clk1p`, `clk1n`, `clk3p`, `clk3n`, `clk9p`, `clk9n`, `clk11p`, and `clk11n`) that can be used for data inputs.

(2) The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not available as general-purpose I/O pins. The `PLL_ENA` pin can only be used to enable the PLLs within the device.

(3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (`FPLL7CLKp/n`, `FPLL8CLKp/n`, `FPLL9CLKp/n`, and `FPLL10CLKp/n`) that can be used for data inputs.

Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm2)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

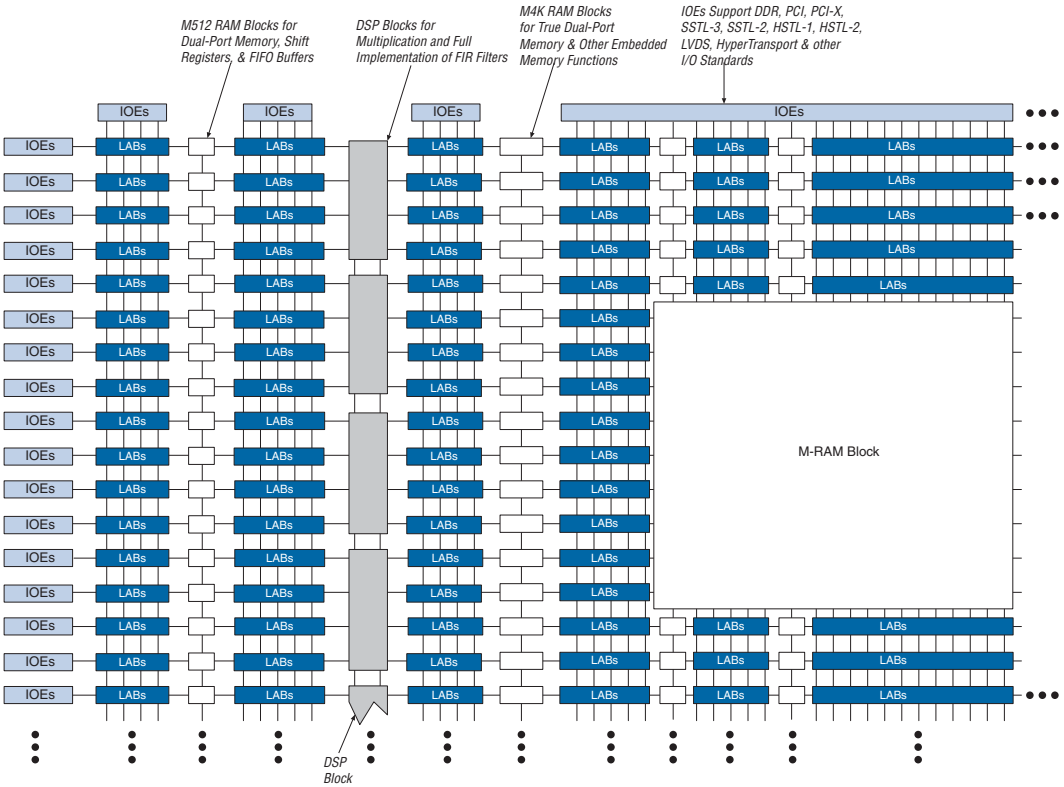
All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

Each Stratix II device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR and DDR2 SDRAM, RLDRAM II, and QDR II SRAM devices. High-speed serial interface channels with dynamic phase alignment (DPA) support data transfer at up to 1 Gbps using LVDS or HyperTransport™ technology I/O standards.

Figure 2–1 shows an overview of the Stratix II device.

Figure 2–1. Stratix II Block Diagram



synchronous load, and clock enable control for the register. These LAB-wide signals are available in all ALM modes. See the "LAB Control Signals" section for more information on the LAB-wide control signals.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix II ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–7 shows the supported LUT combinations in normal mode.

Table 2–2. Stratix II Device Routing Scheme (Part 2 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Column IOE					✓			✓	✓							
Row IOE					✓	✓	✓	✓								

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–3 shows the size and features of the different RAM blocks.

Table 2–3. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	500 MHz	550 MHz	420 MHz
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	
ROM	✓	✓	*(1)*
FIFO buffer	✓	✓	✓
Pack mode		✓	✓
Byte enable	✓	✓	✓
Address clock enable		✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization (**.mif**)	✓	✓	

Digital Signal Processing Block

The most commonly used DSP functions are FIR filters, complex FIR filters, IIR filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix II devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix II device has from two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Stratix II devices have up to 24 DSP blocks per column (see Table 2–5). Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Stratix II DSP block can support one 36 × 36-bit multiplier in a single DSP block. This is true for any combination of signed, unsigned, or mixed sign multiplications.

This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–6 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions. The DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18 × 18-bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9 × 9-bit multipliers in simple multiplier mode.

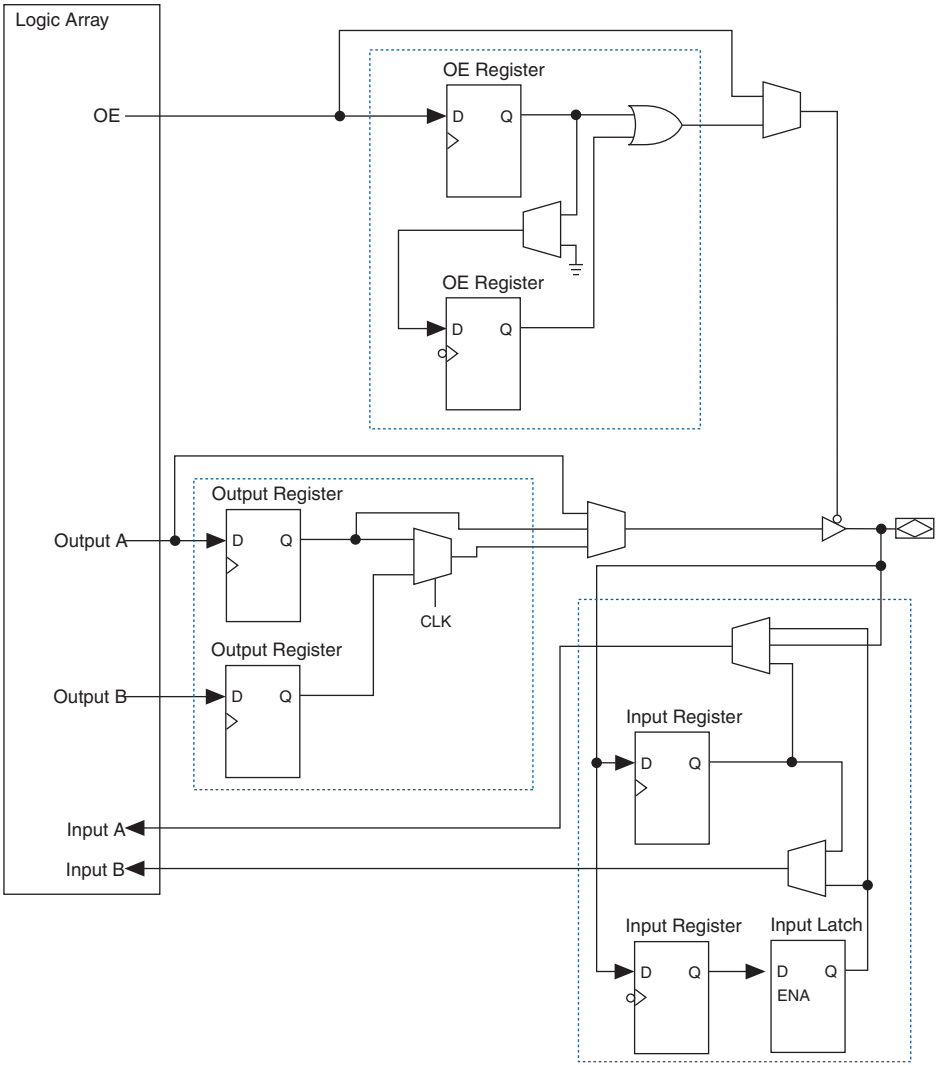
Table 2–6. Multiplier Size & Configurations per DSP Block

DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	-	Two 52-bit multiply-accumulate blocks	-
Two-multipliers adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	-
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	-

DSP Block Interface

Stratix II device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

Figure 2–46. Stratix II IOE Structure



The IOEs are located in I/O blocks around the periphery of the Stratix II device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–47 shows how a row I/O block connects to the logic array. Figure 2–48 shows how a column I/O block connects to the logic array.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2). The PLL banks utilize the adjacent VREF group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at VREFB7 is the reference voltage level for the SSTL input.

I/O pins that reside in PLL banks 9 through 12 are powered by the VCC_PLL<*5, 6, 11, or 12*>_OUT pins, respectively. The EP2S60F484, EP2S60F780, EP2S90H484, EP2S90F780, and EP2S130F780 devices do not support PLLs 11 and 12. Therefore, any I/O pins that reside in bank 11 are powered by the VCCIO3 pin, and any I/O pins that reside in bank 12 are powered by the VCCIO8 pin.

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

On-Chip Termination

Stratix II devices provide differential (for the LVDS or HyperTransport technology I/O standard), series, and parallel on-chip termination to reduce reflections and maintain signal integrity. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Stratix II devices provide four types of termination:

- Differential termination (R_D)
- Series termination (R_S) without calibration
- Series termination (R_S) with calibration
- Parallel termination (R_T) with calibration

Document Revision History

Table 2–27 shows the revision history for this chapter.

Table 2–27. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.3	Updated "Clock Control Block" section.	—
	Updated note in the "Clock Control Block" section.	—
	Deleted Tables 2-11 and 2-12.	—
	Updated notes to: • Figure 2–41 • Figure 2–42 • Figure 2–43 • Figure 2–45	—
	Updated notes to Table 2–18.	—
	Moved Document Revision History to end of the chapter.	—
August 2006, v4.2	Updated Table 2–18 with note.	—
April 2006, v4.1	• Updated Table 2–13. • Removed Note 2 from Table 2–16. • Updated "On-Chip Termination" section and Table 2–19 to include parallel termination with calibration information. • Added new "On-Chip Parallel Termination with Calibration" section. • Updated Figure 2–44.	• Added parallel on-chip termination description and specification. • Changed RCLK names to match the Quartus II software in Table 2–13.
December 2005, v4.0	Updated "Clock Control Block" section.	—
July 2005, v3.1	• Updated HyperTransport technology information in Table 2–18. • Updated HyperTransport technology information in Figure 2–57. • Added information on the asynchronous clear signal.	—
May 2005, v3.0	• Updated "Functional Description" section. • Updated Table 2–3. • Updated "Clock Control Block" section. • Updated Tables 2–17 through 2–19. • Updated Tables 2–20 through 2–22. • Updated Figure 2–57.	—
March 2005, 2.1	• Updated "Functional Description" section. • Updated Table 2–3.	—

The PLL_ENA pin and the configuration input pins (Table 3–4) have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The VCCSEL input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by $V_{CCPD,}$ while the 1.8-V/1.5-V input buffer is powered by V_{CCIO}. Table 3–4 shows the pins affected by VCCSEL.

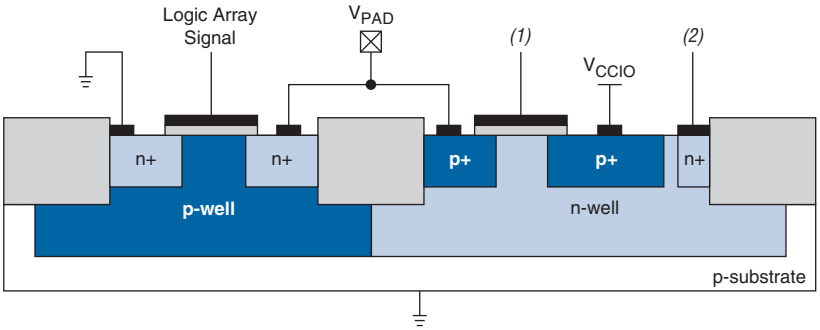
Table 3–4. Pins Affected by the Voltage Level at VCCSEL

Pin	VCCSEL = LOW (connected to GND)	VCCSEL = HIGH (connected to V_{CCPD})
nSTATUS (when used as an input)	3.3/2.5-V input buffer is selected. Input buffer is powered by V_{CCPD}.	1.8/1.5-V input buffer is selected. Input buffer is powered by V_{CCIO} of the I/O bank.
nCONFIG		
CONF_DONE (when used as an input)		
DATA[7..0]		
nCE		
DCLK (when used as an input)		
CS		
nWS		
nRS		
nCS		
CLKUSR		
DEV_OE		
DEV_CLRn		
RUnLU		
PLL_ENA		

VCCSEL is sampled during power-up. Therefore, the VCCSEL setting cannot change on the fly or during a reconfiguration. The VCCSEL input buffer is powered by V_{CCINT} and must be hardwired to V_{CCPD} or ground. A logic high VCCSEL connection selects the 1.8-V/1.5-V input buffer, and a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX® II/microprocessor.

If you need to support configuration input voltages of 3.3 V/2.5 V, you should set the VCCSEL to a logic low; you can set the V_{CCIO} of the I/O bank that contains the configuration inputs to any supported voltage. If

Figure 4–2. Transistor Level Diagram of FPGA Device I/O Buffers



Notes to Figure 4–2:
(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.
(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

Stratix II devices have a POR circuit to keep the whole device system in reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the V_{CCINT}, V_{CCIO}, and V_{CCPD} voltage levels and tri-states all the user I/O pins while V_{CC} is ramping up until normal user levels are reached. The POR circuitry also ensures that all eight I/O bank V_{CCIO} voltages, V_{CCPD} voltage, as well as the logic array V_{CCINT} voltage, reach an acceptable level before configuration is triggered. After the Stratix II device enters user mode, the POR circuit continues to monitor the V_{CCINT} voltage level so that a brown-out condition during user mode can be detected. If there is a V_{CCINT} voltage sag below the Stratix II operational level during user mode, the POR circuit resets the device.

When power is applied to a Stratix II device, a power-on-reset event occurs if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). The maximum V_{CC} rise time for Stratix II device is 100 ms. Stratix II devices provide a dedicated input pin (PORSEL) to select POR delay times of 12 or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms. When the PORSEL pin is connected to V_{CC}, the POR time is 12 ms.

Table 5–40. M512 Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (4)	Max	Min (4)	Max	Min (5)	Max	Min (4)	Max	
$t_{M512DATACO1}$	Clock-to-output delay when using output registers	298	478	298	501	284 298	548	298	640	ps
$t_{M512DATACO2}$	Clock-to-output delay without output registers	2,102	2,345	2,102	2,461	2,003 2,102	2,695	2,102	3,141	ps
$t_{M512CLKL}$	Minimum clock low time	1,315		1,380		1,512 1,512		1,762		ps
$t_{M512CLKH}$	Minimum clock high time	1,315		1,380		1,512 1,512		1,762		ps
$t_{M512CLR}$	Minimum clear pulse width	144		151		165 165		192		ps

Notes to Table 5–40:

(1) F_{MAX} of M512 block obtained using the Quartus II software does not necessarily equal to 1/TM512RC.
(2) These numbers apply to -3 speed grade EP2S15, EP2S30, EP2S60, and EP2S90 devices.
(3) These numbers apply to -3 speed grade EP2S130 and EP2S180 devices.
(4) For the -3 and -5 speed grades, the minimum timing is for the commercial temperature grade. Only -4 speed grade devices offer the industrial temperature grade.
(5) For the -4 speed grade, the first number is the minimum timing parameter for industrial devices. The second number is the minimum timing parameter for commercial devices.

Table 5–41. M4K Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min (4)	Max	Min (4)	Max	Min (5)	Max	Min (4)	Max	
t_{M4KRC}	Synchronous read cycle time	1,462	2,240	1,462	2,351	1,393 1,462	2,575	1,462	3,000	ps
$t_{M4KWERESU}$	Write or read enable setup time before clock	22		23		25 25		29		ps
$t_{M4KWEREH}$	Write or read enable hold time after clock	203		213		233 233		272		ps
$t_{M4KBESU}$	Byte enable setup time before clock	22		23		25 25		29		ps
t_{M4KBEH}	Byte enable hold time after clock	203		213		233 233		272		ps

EP2S15 Clock Timing Parameters

Tables 5–44 though 5–47 show the maximum clock timing parameters for EP2S15 devices.

Table 5–44. EP2S15 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.445	1.512	2.487	2.848	3.309	ns
t_{COUT}	1.288	1.347	2.245	2.570	2.985	ns
t_{PLLCIN}	0.104	0.102	0.336	0.373	0.424	ns
$t_{PLLCOUT}$	-0.053	-0.063	0.094	0.095	0.1	ns

Table 5–45. EP2S15 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.419	1.487	2.456	2.813	3.273	ns
t_{COUT}	1.262	1.322	2.214	2.535	2.949	ns
t_{PLLCIN}	0.094	0.092	0.326	0.363	0.414	ns
$t_{PLLCOUT}$	-0.063	-0.073	0.084	0.085	0.09	ns

Table 5–46. EP2S15 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.232	1.288	2.144	2.454	2.848	ns
t_{COUT}	1.237	1.293	2.140	2.450	2.843	ns
t_{PLLCIN}	-0.109	-0.122	-0.007	-0.021	-0.037	ns
$t_{PLLCOUT}$	-0.104	-0.117	-0.011	-0.025	-0.042	ns

Table 5–50. EP2S30 Row Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.304	1.184	1.966	2.251	2.616	ns
t_{COUT}	1.309	1.189	1.962	2.247	2.611	ns
t_{PLLCIN}	-0.135	–0.158	–0.208	–0.254	–0.302	ns
$t_{PLLCOUT}$	-0.13	–0.153	–0.212	–0.258	–0.307	ns

Table 5–51. EP2S30 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.289	1.352	2.238	2.567	2.990	ns
t_{COUT}	1.294	1.357	2.234	2.563	2.985	ns
t_{PLLCIN}	-0.14	-0.154	-0.169	-0.205	-0.254	ns
$t_{PLLCOUT}$	-0.135	-0.149	-0.173	-0.209	-0.259	ns

EP2S60 Clock Timing Parameters

Tables 5–52 through 5–55 show the maximum clock timing parameters for EP2S60 devices.

Table 5–52. EP2S60 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.681	1.762	2.945	3.381	3.931	ns
t_{COUT}	1.524	1.597	2.703	3.103	3.607	ns
t_{PLLCIN}	0.066	0.064	0.279	0.311	0.348	ns
$t_{PLLCOUT}$	-0.091	-0.101	0.037	0.033	0.024	ns

Table 5–59. EP2S90 Row Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.585	1.658	2.757	3.154	3.665	ns
t_{COUT}	1.590	1.663	2.753	3.150	3.660	ns
t_{PLLCIN}	-0.341	-0.341	-0.193	-0.235	-0.278	ns
$t_{PLLCOUT}$	-0.336	-0.336	-0.197	-0.239	-0.283	ns

EP2S130 Clock Timing Parameters

Tables 5–60 through 5–63 show the maximum clock timing parameters for EP2S130 devices.

Table 5–60. EP2S130 Column Pins Regional Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.889	1.981	3.405	3.722	4.326	ns
t_{COUT}	1.732	1.816	3.151	3.444	4.002	ns
t_{PLLCIN}	0.105	0.106	0.226	0.242	0.277	ns
$t_{PLLCOUT}$	-0.052	-0.059	-0.028	-0.036	-0.047	ns

Table 5–61. EP2S130 Column Pins Global Clock Timing Parameters

Parameter	Minimum Timing		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
	Industrial	Commercial				
t_{CIN}	1.907	1.998	3.420	3.740	4.348	ns
t_{COUT}	1.750	1.833	3.166	3.462	4.024	ns
t_{PLLCIN}	0.134	0.136	0.276	0.296	0.338	ns
$t_{PLLCOUT}$	-0.023	-0.029	0.022	0.018	0.014	ns

Table 5–78. Maximum Output Toggle Rate on Stratix II Devices (Part 4 of 5) *Note (1)*

I/O Standard	Drive Strength	Column I/O Pins (MHz)			Row I/O Pins (MHz)			Clock Outputs (MHz)		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.8-V LVTTL	OCT 50 Ω	700	550	450	700	550	450	700	550	450
3.3-V LVCMOS	OCT 50 Ω	350	350	300	350	350	300	350	350	300
1.5-V LVCMOS	OCT 50 Ω	550	450	400	550	450	400	550	450	400
SSTL-2 Class I	OCT 50 Ω	600	500	500	600	500	500	600	500	500
SSTL-2 Class II	OCT 25 Ω	600	550	500	600	550	500	600	550	500
SSTL-18 Class I	OCT 50 Ω	560	400	350	590	400	350	450	400	350
SSTL-18 Class II	OCT 25 Ω	550	500	450	-	-	-	550	500	450
1.2-V HSTL *(2)*	OCT 50 Ω	280	-	-	-	-	-	280	-	-
1.5-V HSTL Class I	OCT 50 Ω	600	550	500	600	550	500	600	550	500
1.8-V HSTL Class I	OCT 50 Ω	650	600	600	650	600	600	650	600	600
1.8-V HSTL Class II	OCT 25 Ω	500	500	450	-	-	-	500	500	450
Differential SSTL-2 Class I	OCT 50 Ω	600	500	500	600	500	500	600	500	500
Differential SSTL-2 Class II	OCT 25 Ω	600	550	500	600	550	500	600	550	500
Differential SSTL-18 Class I	OCT 50 Ω	560	400	350	590	400	350	560	400	350
Differential SSTL-18 Class II	OCT 25 Ω	550	500	450	-	-	-	550	500	450
1.8-V Differential HSTL Class I	OCT 50 Ω	650	600	600	650	600	600	650	600	600
1.8-V Differential HSTL Class II	OCT 25 Ω	500	500	450	-	-	-	500	500	450
1.5-V Differential HSTL Class I	OCT 50 Ω	600	550	500	600	550	500	600	550	500

High-Speed I/O Specifications

Table 5–88 provides high-speed timing specifications definitions.

Table 5–88. High-Speed Timing Specifications & Definitions

High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 5–89 shows the high-speed I/O timing specifications for -3 speed grade Stratix II devices.

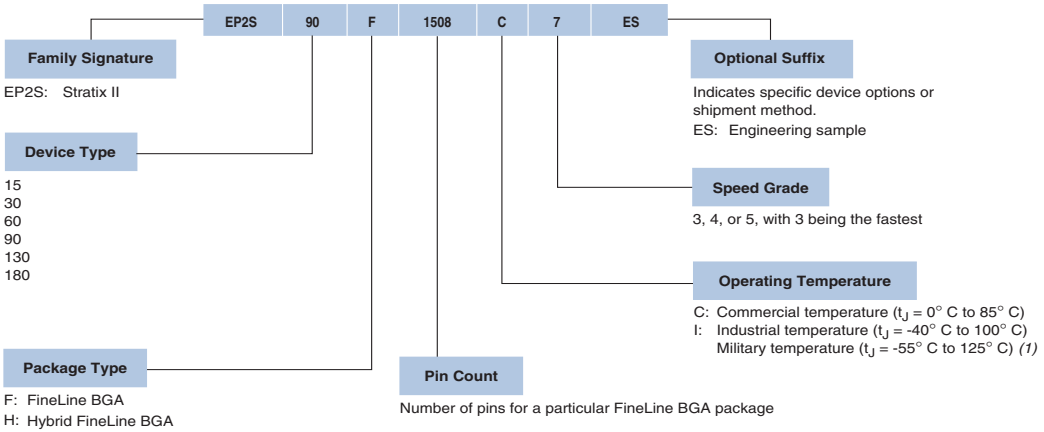
Table 5–89. High-Speed I/O Specifications for -3 Speed Grade (Part 1 of 2) *Notes (1), (2)*

Symbol	Conditions	-3 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (clock frequency) $f_{HSCLK} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*	16		520	MHz
	W = 1 (SERDES bypass, LVDS only)	16		500	MHz
	W = 1 (SERDES used, LVDS only)	150		717	MHz

Table 5–103. Document Revision History (Part 3 of 3)

Date and Document Version	Changes Made	Summary of Changes
January 2005, v2.0	• Updated the "Power Consumption" section. • Added the "High-Speed I/O Specifications" and "On-Chip Termination Specifications" sections. • Removed the ESD Protection Specifications section. • Updated Tables 5–3 through 5–13, 5–16 through 5–18, 5–21, 5–35, 5–39, and 5–40. • Updated tables in "Timing Model" section. • Added Tables 5–30 and 5–31.	—
October 2004, v1.2	• Updated Table 5–3. • Updated introduction text in the "PLL Timing Specifications" section.	—
July 2004, v1.1	• Re-organized chapter. • Added typical values and C_{OUTFB} to Table 5–32. • Added undershoot specification to Note (4) for Tables 5–1 through 5–9. • Added Note (1) to Tables 5–5 and 5–6. • Added V_{ID} and V_{ICM} to Table 5–10. • Added "I/O Timing Measurement Methodology" section. • Added Table 5–72. • Updated Tables 5–1 through 5–2 and Tables 5–24 through 5–29.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Figure 6–1. Stratix II Device Packaging Ordering Information



Note to Figure 6–1:
(1) Applicable to I4 devices. For more information, refer to the *Stratix II Military Temperature Range Support* technical brief.

Document Revision History

Table 6–1 shows the revision history for this chapter.

Table 6–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
April 2011, v2.2	Updated Figure 6–1.	Added operating junction temperature for military use.
May 2007, v2.1	Moved the Document Revision History section to the end of the chapter.	—
January 2005, v2.0	Contact information was removed.	—
October 2004, v1.1	Updated Figure 6–1.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—