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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx8240vtpu200e

1.2 Pinout Listing

Table 1-1 provides the pinout listing for the PC8240, 352 TBGA package.

Table 1-1. PC8240 Pinout Listing

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
$\overline{C/BE}$[0 – 3]	A25 F23 K23 P25	I/O	OVdd	DRV_PCI	(6)(15)
$\overline{DEVSEL}$	H26	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{FRAME}$	J24	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{IRDY}$	K25	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{LOCK}$	J26	Input	OVdd	–	(8)
AD[0 – 31]	C22 D22 B22 B23 D19 B24 A24 B26 A26 C26 D25 D26 E23 E25 E26 F24 L26 L25 M25 M26 N23 N25 N26 R26 R25 T26 T25 U23 U24 U26 U25 V25	I/O	OVdd	DRV_PCI	(6)(15)
PAR	G25	I/O	OVdd	DRV_PCI	(15)
$\overline{GNT}$[0 – 3]	V26 W23 W24 W25	Output	OVdd	DRV_PCI	(6)(15)
$\overline{GNT4}$/DA5	W26	Output	OVdd	DRV_PCI	(7)(15)
$\overline{REQ}$[0 – 3]	AB26 AA25 AA26 Y25	Input	OVdd	–	(6)(12)
$\overline{REQ4}$/DA4	Y26	Input	OVdd	–	(12)
$\overline{PERR}$	G26	I/O	OVdd	DRV_PCI	(8)(15)(18)
$\overline{SERR}$	F26	I/O	OVdd	DRV_PCI	(8)(15)(16)
$\overline{STOP}$	H25	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{TRDY}$	K26	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{INTA}$	AC26	Output	OVdd	DRV_PCI	(15)(16)
IDSEL	P26	Input	OVdd	–	–
Memory Interface Signals					
MDL[0 – 31]	AD17 AE17 AE15 AF15 AC14 AE13 AF13 AF12 AF11 AF10 AF9 AD8 AF8 AF7 AF6 AE5 B1 A1 A3 A4 A5 A6 A7 D7 A8 B8 A10 D10 A12 B11 B12 A14	I/O	GVdd	DRV_MEM_DATA	(5)(6)(13)
MDH[0 – 31]	AC17 AF16 AE16 AE14 AF14 AC13 AE12 AE11 AE10 AE9 AE8 AC7 AE7 AE6 AF5 AC5 E4 A2 B3 D4 B4 B5 D6 C6 B7 C9 A9 B10 A11 A13 B13 A15	I/O	GVdd	DRV_MEM_DATA	(6)(13)
$\overline{CAS}$/DQM[0 – 7]	AB1 AB2 K3 K2 AC1 AC2 K1 J1	Output	GVdd	DRV_MEM_ADDR	(6)
$\overline{RAS/CS}$[0 – 7]	Y4 AA3 AA4 AC4 M2 L2 M1 L1	Output	GVdd	DRV_MEM_ADDR	(6)
$\overline{FOE}$	H1	I/O	GVdd	DRV_MEM_ADDR	(3)(4)
$\overline{RCS0}$	N4	I/O	GVdd	DRV_MEM_ADDR	(3)(4)
$\overline{RCS1}$	N2	Output	GVdd	DRV_MEM_ADDR	–
SDMA[11 – 0]	N1 R1 R2 T1 T2 U4 U2 U1 V1 V3 W1 W2	Output	GVdd	DRV_MEM_ADDR	(6)(14)
SDMA12/SDBA1	P1	Output	GVdd	DRV_MEM_ADDR	(14)

Table 1-1. PC8240 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
$\overline{\text{MIV}}$	A16	Output	OVdd	DRV_STD	–
PMAA[0 – 2]	AD18 AF18 AE19	Output	OVdd	DRV_STD	(3)(4)(6)(15)
Test/Configuration Signals					
PLL_CFG[0 – 4]/ DA[10 – 6]	A22 B19 A21 B18 B17	Input	OVdd	–	(4)(6)
$\overline{\text{TEST}}$[0 – 1]	AD22 B20	Input	OVdd	–	(1)(6)(9)
$\overline{\text{TEST2}}$	Y2	Input	–	–	(11)
TEST3	AF20	Input	OVdd	–	(10)
TEST4	AC18	I/O	OVdd	DRV_STD	(10)
TCK	AF22	Input	OVdd	–	(9)(12)
TDI	AF23	Input	OVdd	–	(9)(12)
TDO	AC21	Output	OVdd	DRV_PCI	–
TMS	AE22	Input	OVdd	–	(9)(12)
TRST	AE23	Input	OVdd	–	(9)(12)
Power and Ground Signals					
GND	AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3	Ground 52 terminals	–	–	–
LVdd	AC20 AC23 D20 D23 G23 P23 Y23	Reference voltage 3.3V, 5.0V	LVdd	–	–
GVdd	AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3	Power for Memory Drivers 2.5V, 3.3V	GVdd	–	–
OVdd	AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24	PCI/Stnd 3.3V	OVdd	–	–
Vdd	AA24 AC16 AC19 AD12 AD6 AD9 C15 C18 C21 D11 D8 F3 H23 J3 L23 M3 R24 T4 V24 W4	Power for Core 2.5V	Vdd	–	–
LAVdd	D17	Power for DLL 2.5V	LAVdd	–	–
AVdd	C17	Power for PLL (CPU Core Logic) 2.5V	AVdd	–	–
AVdd2	AF24	Power for PLL (Peripheral Logic) 2.5V	AVdd2	–	–

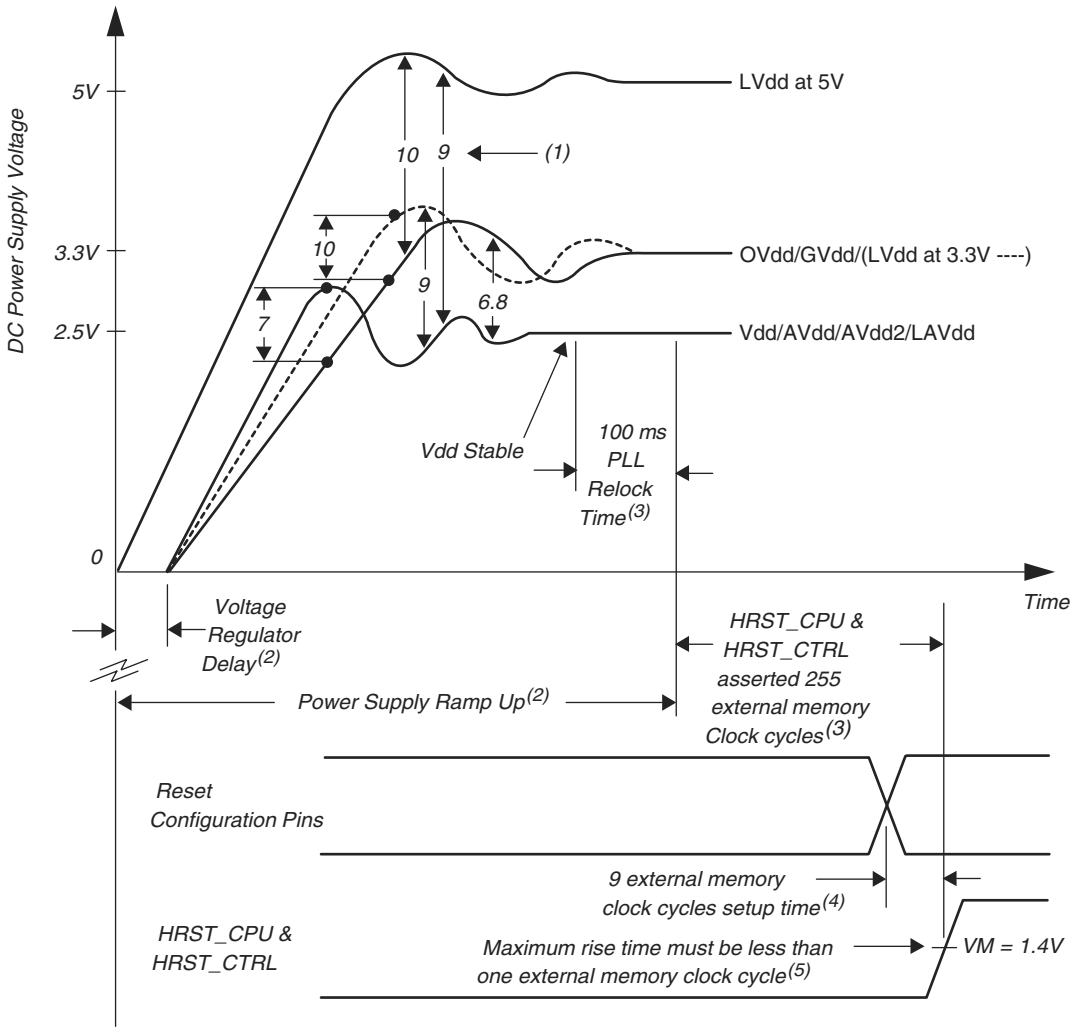
3.3 Recommended Operating Conditions

Table 3-2. Recommended Operating Conditions

Symbol	Characteristic[1]		Recommended Value	Unit	Notes
Vdd	Supply Voltage		2.5 ± 5 %	V	(5)
OVdd	I/O Buffer supply for PCI and Standard		3.3 ± 0.3	V	(5)
GVdd	Supply Voltages for Memory Bus Drivers		3.3 ± 5 %	V	(7)
			2.5 ± 5 %	V	(7)
AVdd	PLL Supply Voltage – CPU Core Logic		2.5 ± 5 %	V	(5)
AVdd2	PLL Supply Voltage – Peripheral Logic		2.5 ± 5 %	V	(6)
LAVdd	DLL Supply Voltage		2.5 ± 5 %	V	(6)
LVdd	PCI Reference		5 ± 5 %	V	(8)(9)
			3.3 ± 0.3	V	(8)(9)
V_{IN}	Input Voltage	PCI Inputs	0 to 3.6 or 5.75	V	(2)(3)
		All Other Inputs	0 to 3.6	V	(4)
T_C	Operating Temperature		–40 to 125	°C	

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. PCI pins are designed to withstand LVdd + 0.5V DC when LVdd is connected to a 5.0V DC power supply.
3. PCI pins are designed to withstand LVdd + 0.5V DC when LVdd is connected to a 3.3V DC power supply.
4. Caution: Input voltage (V_{IN}) must not be greater than the supply voltage (Vdd/AVdd/AVdd2/LAVdd) by more than 2.5V at all times including during power-on reset.
5. Caution: OVdd must not exceed Vdd/AVdd/AVdd2/LAVdd by more than 1.8V at any time including during power-on reset.
6. Caution: Vdd/AVdd/AVdd2/LAVdd must not exceed OVdd by more than 0.6V at any time including during power-on reset.
7. Caution: GVdd must not exceed Vdd/AVdd/AVdd2/LAVdd by more than 1.8V at any time including during power-on reset.
8. Caution: LVdd must not exceed Vdd/AVdd/AVdd2/LAVdd by more than 5.4V at any time including during power-on reset.
9. Caution: LVdd must not exceed OVdd by more than 3.6V at any time including during power-on reset.

Figure 3-1. Supply Voltage Sequencing and Separation Cautions

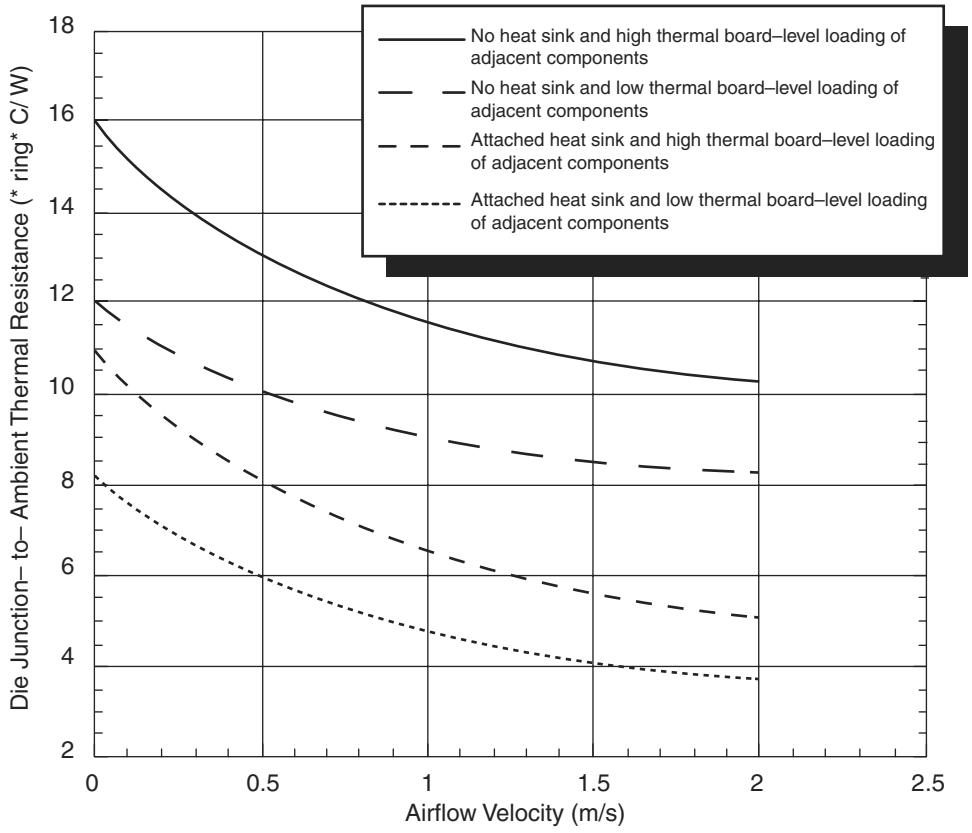


Notes:
1. Numbers associated with waveform separations correspond to caution numbers listed in Table 3-2, “Recommended Operating Conditions,” on page 9.
2. Refer to “Power Supply Voltage Sequencing” on page 37 for additional information.
3. Refer to Table 4-4 on page 20 for additional information on PLL Relock and reset signal assertion timing requirements.
4. Refer to Table 4-5 on page 22 for additional information on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST\_CPU/HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the non-reset state.

Figure 3-4 depicts the die junction-to-ambient thermal resistance for four typical cases:

1. A heat sink is not attached to the TBGA package and there exists high board-level thermal loading of adjacent components.
2. A heat sink is not attached to the TBGA package and there exists low board-level thermal loading of adjacent components.
3. A heat sink (e.g. ChipCoolers #HTS255-P) is attached to the TBGA package and there exists high board-level thermal loading of adjacent components.
4. A heat sink (e.g. ChipCoolers #HTS255-P) is attached to the TBGA package and there exists low board-level thermal loading of adjacent components.

Figure 3-4. Die Junction-to-Ambient Resistance



The board designer can choose between several types of heat sinks to place on the PC8240. There are several commercially-available heat sinks for the PC8240 provided by the following vendors:

Chip Coolers Inc. 333 Strawberry Field Rd. Warwick, RI 02887-6979	800-227-0254 (USA/Canada) 401-739-7600 Internet: www.chipcoolers.com
International Electronic Research Corporation (IERC) 135 W. Magnolia Blvd. Burbank, CA 91502	818-842-7277 Internet: www.ctscorp.com
Thermalloy 2021 W. Valley View Lane Dallas, TX 75234-8993	972-243-4321 Internet: www.thermalloy.com
Wakefield Engineering 100 Cummings Center, Suite 157H Beverly, MA 01915	781-406-3000 Internet: www.wakefield.com
Aavid Engineering 250 Apache Trail Terrell, TX 75160	972-551-7330 Internet: www.aavid.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

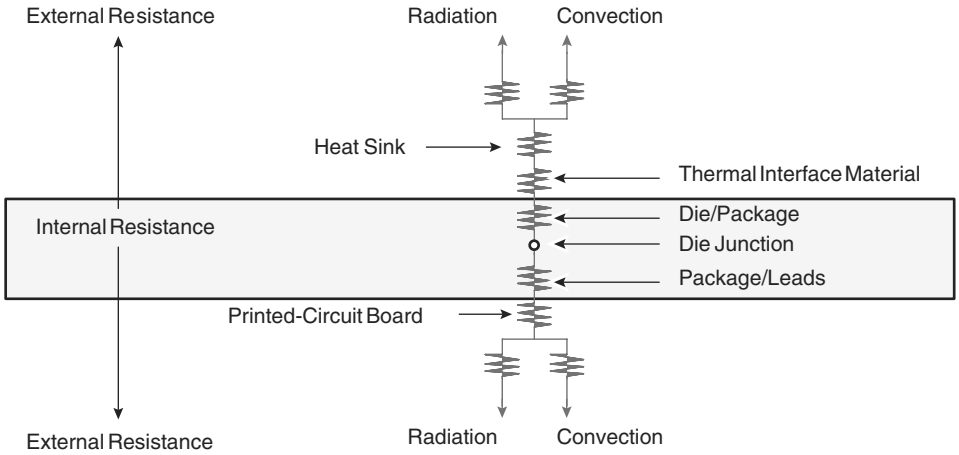
3.4.3 Internal Package Conduction Resistance

For the TBGA, cavity down, packaging technology, shown in Figure 3-3 on page 11, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance,
- The die junction-to-ball thermal resistance.

Figure 3-5 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 3-5. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



(Note the internal versus external package resistance)

For this cavity-down, wire-bond TBGA package, heat generated on the active side of the chip is conducted through the silicon, the die attach and package spreader, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Dow-Corning Corporation Dow-Corning Electronic Materials PO Box 0997 Midland, MI 48686-0997	800-248-2481 Internet: www.dow.com
Chomerics, Inc. 77 Dragon Court Woburn, MA 01888-4014	781-935-4850 Internet: www.chomerics.com
Thermagon Inc. 3256 West 25th Street Cleveland, OH 44109-1668	888-246-9050 Internet: www.thermagon.com
Loctite Corporation 1001 Trout Brook Crossing Rocky Hill, CT 06067-3910	860-571-5100 Internet: www.loctite.com

3.4.4.1 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$T_J = T_A + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$

Where:

T_J is the die-junction temperature.

T_A is the inlet cabinet ambient temperature.

T_R is the air temperature rise within the computer cabinet.

θ_{JC} is the junction-to-case thermal resistance.

θ_{INT} is the adhesive or interface material thermal resistance.

θ_{SA} is the heat sink base-to-ambient thermal resistance.

P_D is the power dissipated by the device.

During operation the die-junction temperatures (T_J) should be maintained less than the value specified in Table. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30 to 40° C. The air temperature rise within a cabinet (T_R) may be in the range of 5 to 10° C. The thermal resistance of the thermal interface material (θ_{INT}) is typically about 1° C/W. Assuming a T_A of 30° C, a T_R of 5° C, a TBGA package θ_{JC} = 1.8, and a power consumption (P_D) of 5.0 watts, the following expression for T_J is obtained:

Die-junction temperature: $T_J = 30° C + 5° C + (1.8° C/W + 1.0° C/W + \theta_{SA}) \times 5.0W$

For preliminary heat sink sizing, the heat sink base-to-ambient thermal resistance is needed from the heat sink manufacturer.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow.

7. The typical minimum I/O power values were results of the PC8240 performing cache resident integer operations at the slowest frequency combination of 33:66:166 (PCI:Mem:CPU) MHz.
8. The typical maximum OVdd value resulted from the PC8240 operating at the fastest frequency combination of 66:100:200 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeroes to PCI memory.
9. The typical maximum GVdd value resulted from the PC8240 operating at the fastest frequency combination of 66:100:200 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeroes on 64-bit boundaries to local memory.

Note: To calculate the power consumption at low temperature (–55°C), use a 1.25 factor.

3.6 Marking

The document where markings are defined is identified in the related reference documents. Each microcircuit is legible and permanently marked with the following information as minimum:

- e2v Logo,
- Manufacturer's part number, Date-code of inspection lot,
- ESD identifier if available,
- Country of manufacturing.

4. Electrical Characteristics

4.1 Static Characteristics

Table 4-1 provides the DC electrical characteristics for the PC8240.

At recommended operating conditions (see Table 3-2 on page 9)

Table 4-1. DC Electrical Specifications

Characteristics[1]	Conditions[4]	Symbol	Value		Unit
			Min	Max	
Input High Voltage	PCI only	V_{IH}	0.5*OVdd	LVdd	V
Input Low Voltage	PCI only	V_{IL}	–	0.3*OVdd	V
Input High Voltage	All other pins (GVdd = 3.3V)	V_{IH}	2.0	3.3	V
Input High Voltage	All other pins (GVdd = 2.5V)	V_{IH}	1.8	2.5	V
Input Low Voltage	All inputs except OSC_IN	V_{IL}	GND	0.8	V
PCI_SYNC_IN Input High Voltage		CV_{IH}	0.5*OVdd	–	V
PCI_SYNC_IN Input Low Voltage		CV_{IL}	GND	0.3*OVdd	V
Input Leakage Current[5] for pins using DRV_PCI driver	0.5V V_{IN} 2.7V at LVdd = 4.75	I_L	–	70	A
Input Leakage Current[5] for pins using DRV_PCI driver	0.5V V_{IN} 5.5V at LVdd = 5.5	I_L	–	TBD	A
Input Leakage Current[5] all others	LVdd = 3.6V GVdd = 3.465	I_L	–	10	A
Output High Voltage	I_{OH} = N/A (GVdd = 3.3V)[3]	V_{OH}	2.4	–	V
Output Low Voltage	I_{OL} = N/A (GVdd = 3.3V)[3]	V_{OL}	–	0.4	V

2. For all others with OVdd or GVdd = 3.3V, I_{OH} read from the listing in the pull-up mode, I(Min) column, at the 0.9V table entry which corresponds to the V_{OH} = 2.4V where Table Entry Voltage = O/GVdd - PCI V_{OH}.
3. For GVdd = 2.5V, I_{OH} read from the listing in the pull-up mode, I(Min) column, at the TBDV table entry which corresponds to the V_{OH} = TBD V where Table Entry Voltage = GVdd - V_{OH}.
4. For DRV_PCI, I_{OL} read from the listing in the pull-down mode, I(Max) column, at 0.33V = PCI V_{OL} = 0.1*LVdd (LVdd = 3.3V) by interpolating between the 0.3V and 0.4V table entries.
5. For all others with OVdd or GVdd = 3.3V, I_{OL} read from the listing in the pull-down mode, I(Max) column, at the 0.4V table entry.
6. For GVdd = 2.5V, I_{OL} read from the listing in the pull-down mode, I(Max) column, at the TBDV table entry.

4.2 Dynamic Electrical Characteristics

This section provides the AC electrical characteristics for the PC8240. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 4-4, “Clock AC Timing Specifications,” on page 20 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0-4] signals. Parts are sold by maximum processor core frequency; see “Ordering Information” on page 42.

Table 4-3 provides the operating frequency information for the PC8240.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 4-3. Operating frequency

Characteristic[1]	200 MHz		Unit
	Min	Max	
Processor Frequency (CPU)	100	200	MHz
Memory Bus Frequency	25 - 100		MHz
PCI Input Frequency	25 - 66		MHz

Note: 1. Caution: The PCI_SYNC_IN frequency and PLL_CFG[0 – 4] settings must be chosen such that the resulting peripheral logic/memory bus frequency, CPU (core) frequency, and PLL (VCO) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0 – 4] signal description in “PLL Configuration” on page 36 for valid PLL_CFG[0 – 4] settings and PCI_SYNC_IN frequencies.

4.2.1 Clock AC Specifications

Table 4-4 provides the clock AC timing specifications as defined in Section.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 4-4. Clock AC Timing Specifications

Num	Characteristics and Conditions[1]	Min	Max	Unit	Notes
1a	Frequency of Operation (PCI_SYNC_IN)	25	66	MHz	
1b	PCI_SYNC_IN Cycle Time	40	15	ns	
2, 3	PCI_SYNC_IN Rise and Fall Times	–	2.0	ns	(2)
4	PCI_SYNC_IN Duty Cycle Measured at 1.4V	40	60	%	
5a	PCI_SYNC_IN Pulse Width High Measured at 1.4V	6	9	ns	(3)
5b	PCI_SYNC_IN Pulse Width Low Measured at 1.4V	6	9	ns	(3)
7	PCI_SYNC_IN Short Term Jitter (Cycle to Cycle)	–	< 500	ps	
8a	PCI_CLK[0 – 4] Skew (Pin to Pin)	0	500	ps	
8b	SDRAM_CLK[0 – 3] Skew (Pin to Pin)	TBD	TBD	ps	(8)
10	Internal PLL Relock Time	–	100	µs	(3)(4)(6)
15	DLL Lock Range with DLL_EXTEND = 0 disabled (Default)	0 (NT_{clk} - t_{loop} - t_{fix0}) 7		ns	(7)
16	DLL Lock Range with DLL_EXTEND = 1 enabled	0 (NT_{clk} - T_{clk}/2 - t_{loop} - tf_{ix0}) 7		ns	(7)
17	Frequency of Operation (OSC_IN)	25	66	MHz	
18	OSC_IN Cycle Time	40	15	ns	
19	OSC_IN Rise and Fall Times	–	5	ns	(5)
20	OSC_IN Duty Cycle Measured at 1.4V	40	60	%	
21	OSC_IN Frequency Stability	–	100	ppm	
22	OSC_IN V_{IH} (Loaded)	TBD		V	
23	OSC_IN V_{IL} (Loaded)	–	TBD	V	

Notes:
1. These specifications are for the default driver strengths indicated in Table 4-2 on page 18.
2. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4V.
3. Specification value at maximum frequency of operation.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.
6. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRST\_CPU/HRST\_CTRL}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
7. DLL_EXTEND is bit 7 of the PMC2 register <72>. N is a non-zero integer (1, 2, 3, ...). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. t_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. t_{fix0} is a fixed delay inherent in the design when the DLL is at tap point 0 and the DLL is contributing no delay; t_{fix0} equals approximately 3 ns. See Figure 4-2 on page 21 for DLL locking ranges.

4.2.2 Input AC Timing Specifications

Table 4-5 provides the input AC timing specifications. See Figure 4-3 on page 22 and Figure 4-4 on page 23.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 4-5. Input AC Timing Specifications

Num	Characteristics	Min	Max	Unit	Notes
10a	PCI Input Signals Valid to PCI_SYNC_IN (Input Setup)	2.0	–	ns	(2)(3)
10b1	Memory Control and Data Input Signals in Flow Through Mode Valid to SDRAM_SYNC_IN (Input Setup)	4.0	–	ns	(1)(3)
10b2	Memory Control and Data Input Signals in Registered Mode Valid to SDRAM_SYNC_IN (Input Setup)	TBD	–	ns	(1)(3)
10c	Epic, Misc. Debug Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	TBD	–	ns	(1)(3)
10d	Two-wire Interface Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	TBD	–	ns	(1)(3)
10e	Mode select Inputs Valid to HRST_CPU/HRST_CTRL (Input Setup)	$9*t_{CLK}$	–	ns	(1)(3)(5)
11a	PCI_SYNC_IN (SDRAM_SYNC_IN) to Inputs Invalid (Input Hold)	1.0	–	ns	(1)(2)(3)
11b	$\overline{\text{HRST\_CPU/HRST\_CTRL}}$ to Mode select Inputs Invalid (Input Hold)	TBD	–	ns	(1)(3)(5)

Notes:
1. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0V) of the signal in question to the V_M = 1.4V of the rising edge of the memory bus clock, SDRAM_SYNC_IN. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 4-3 on page 22.
2. All PCI signals are measured from OVdd/2 of the rising edge of PCI_SYNC_IN to 0.4*OVdd of the signal in question for 3.3V PCI signaling levels. See Figure 4-4.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0V) of the signal in question to the V_M = 1.4V of the rising edge of the $\overline{\text{HRST\_CPU/HRST\_CTRL}}$ signal. See Figure 4-5.

Figure 4-3. Input – Output Timing Diagram Referenced to SDRAM_SYNC_IN

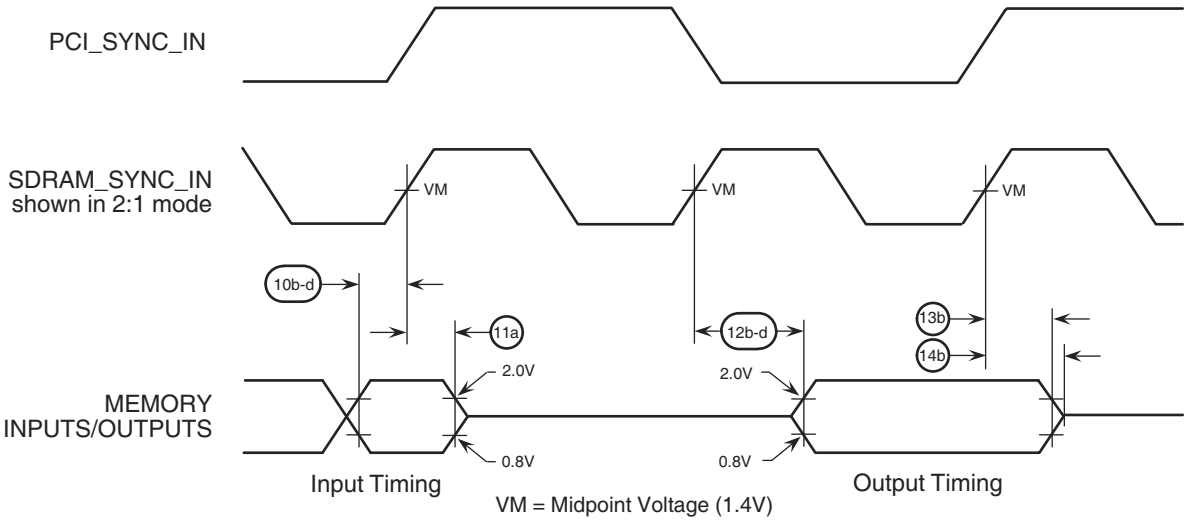


Figure 4-4. Input – Output Timing Diagram Referenced to PCI_SYNC_IN

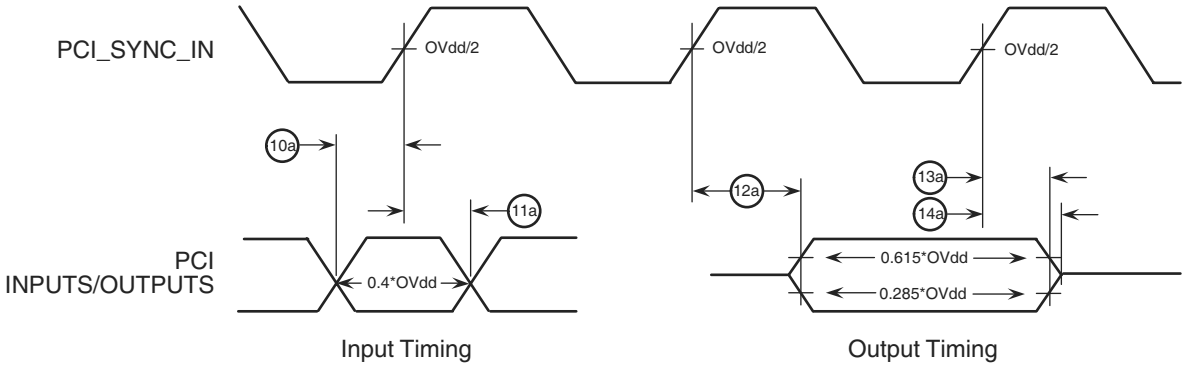
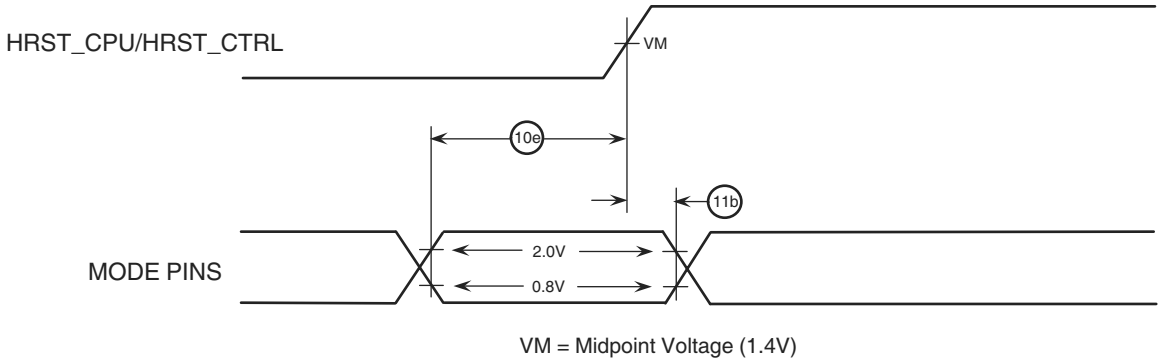


Figure 4-5. Input Timing Diagram for Mode Select Signals



4.2.3 Output AC Timing Specification

Table 4-6 provides the processor bus AC timing specifications for the PC8240. See Figure 4-3 on page 22 and Figure 4-4 on page 23.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Figure 4-9. Two-wire Interface Timing Diagram II

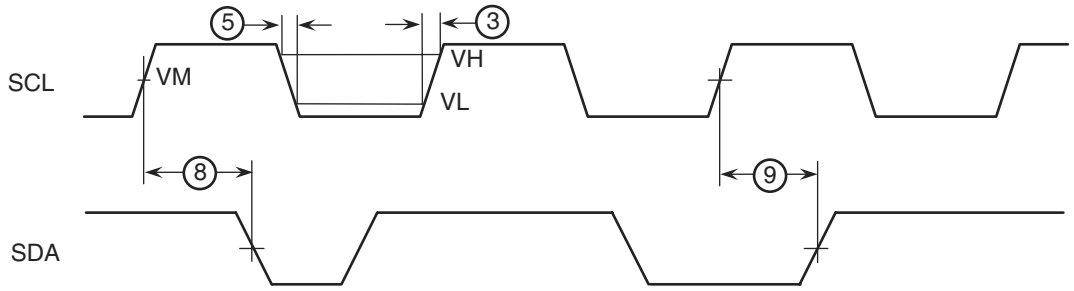
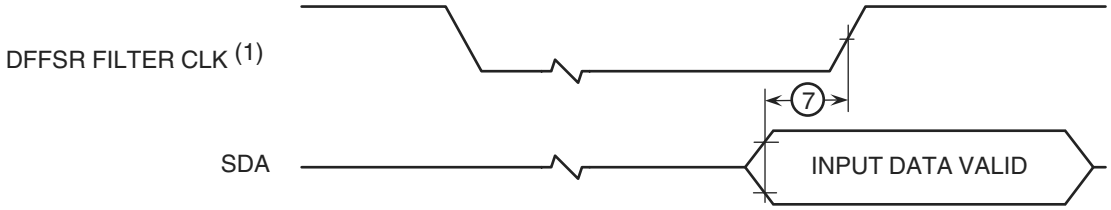
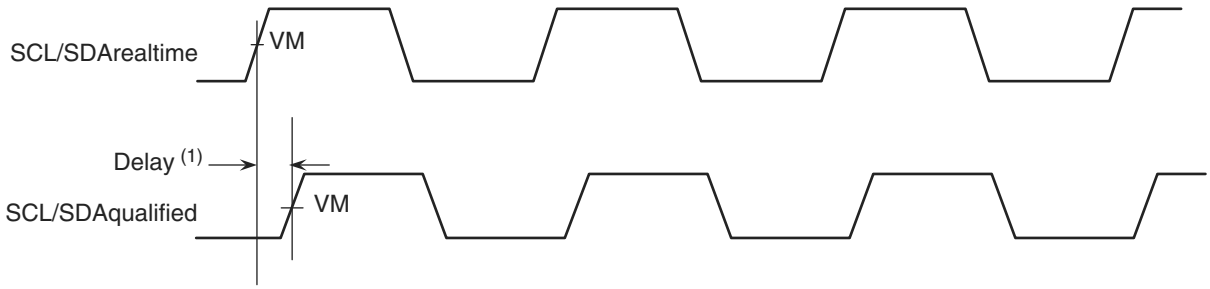


Figure 4-10. Two-wire Interface Timing Diagram III



Note: 1. DFFSR Filter Clock is the SDRAM_CLK clock times DFFSR value.

Figure 4-11. Two-wire Interface Timing Diagram IV (Qualified signal)



Note: 1. The delay is the Local Memory clock times DFFSR times 2 plus 1 Local Memory clock.

4.2.6 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 4-12 provides the JTAG AC timing specifications for the PC8240 while in the JTAG operating mode.

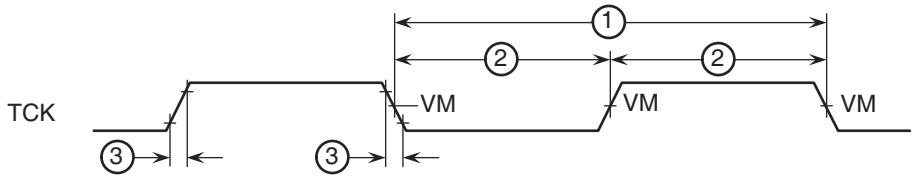
At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 4-12. JTAG AC Timing Specifications (Independent of PCI_SYNC_IN)

Num	Characteristics[4]	Min	Max	Unit	Notes
	TCK Frequency of Operation	0	25	MHz	
1	TCK Cycle Time	40	–	ns	
2	TCK Clock Pulse Width Measured at 1.5V	20	–	ns	
3	TCK Rise and Fall Times	0	3	ns	
4	TRST_ Setup Time to TCK Falling Edge	10	–	ns	(1)
5	TRST_ Assert Time	10	–	ns	
6	Input Data Setup Time	5	–	ns	(2)
7	Input Data Hold Time	15	–	ns	(2)
8	TCK to Output Data Valid	0	30	ns	(3)
9	TCK to Output High Impedance	0	30	ns	(3)
10	TMS, TDI Data Setup Time	5	–	ns	
11	TMS, TDI Data Hold Time	15	–	ns	
12	TCK to TDO Data Valid	0	15	ns	
13	TCK to TDO High Impedance	0	15	ns	

Notes: 1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test (other than TDI and TMS) signal input timing with respect to TCK.
3. Non-test (other than TDO) signal output timing with respect to TCK.
4. Timings are independent of the system clock (PCI_SYNC_IN).

Figure 4-14. JTAG Clock Input Timing Diagram



VM = Midpoint Voltage

Figure 4-15. JTAG TRST Timing Diagram

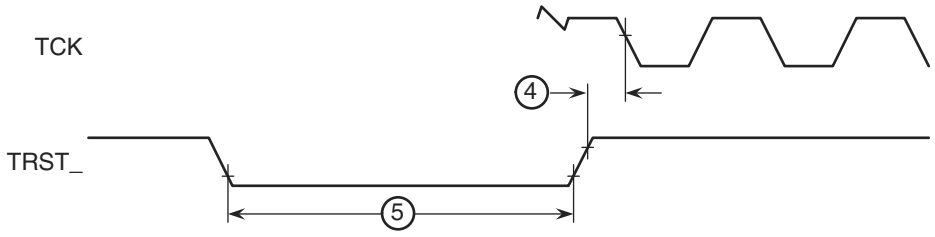


Figure 4-16. JTAG Boundary Scan Timing Diagram

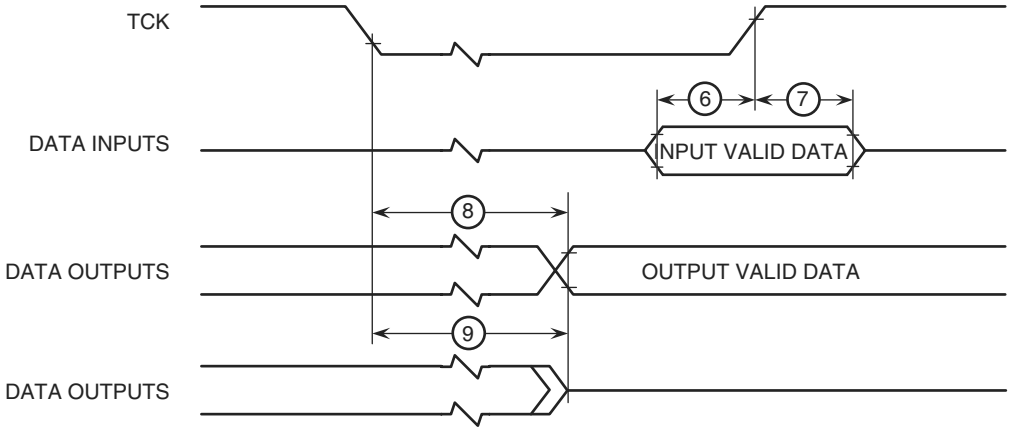
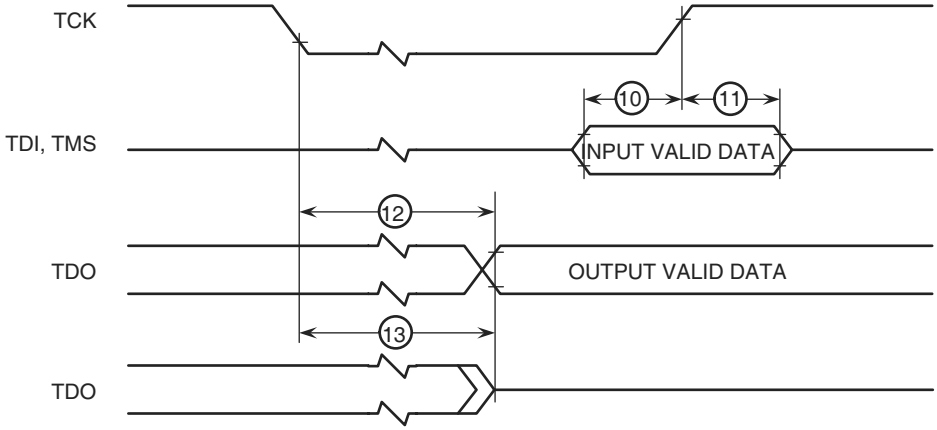


Figure 4-17. Test Access Port Timing Diagram



7.3 PLL Configuration

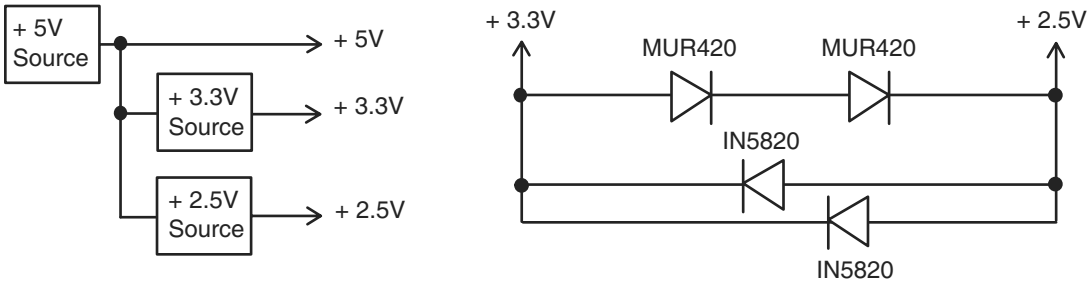
The PC8240's internal PLLs are configured by the PLL_CFG[0–4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the Peripheral Logic/Memory Bus PLL (VCO) frequency of operation for the PCI-to-Memory frequency multiplying and the 603e CPU PLL (VCO) frequency of operation for Memory-to-CPU frequency multiplying. The PLL configuration for the PC8240 is shown in Table 7-2.

Table 7-2. PC8240 Microprocessor PLL Configuration

			200 MHz Part[9]			Ratios [4][5]	
Ref	PLL_ CFG [0 – 4][1][3]	CPU HID1 [0 – 4][2]	PCI Clock Input (PCI_SYNC_IN) Range[1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO) Multiplier	Mem to CPU (CPU VCO) Multiplier
0	00000	00110	25 – **26**	75 – 80	188 – **200**	3[6]	2.5[5]
1	00001	TBD	NOT USABLE			3[6]	3[6]
2	00010	TBD	50 – 56[6]	50 – 56	100 – 112	1[4]	2[8]
3	00011	TBD	Bypass			Bypass	2[8]
4	00100	00101	25 – 28[6]	50 – 56	100 – 113	2[8]	2[8]
5	00101	TBD	Bypass			Bypass	2.5[5]
7	00111	TBD	Bypass			Bypass	3[6]
8	01000	11000	33[7] – 56[6]	33 – 56	100 – 168	1[4]	3[6]
A	01010	TBD	NOT USABLE			2[4]	4.5[9]
C	01100	00110	25 – **40**	50 – 80	125 – **200**	2[4]	2.5[5]
E	01110	11000	25 – **33**	50 – 66	150 – **200**	2[4]	3[6]
10	10000	00100	25 – **33**	75 – 100	150 – **200**	3[6]	2[4]
12	10010	00100	33[8] – **66**	50 – 100	100 – **200**	1.5[3]	2[4]
14	10100	11110	25 – **28**	50 – 56	175 – **200**	2[4]	3.5[7]
16	10110	11010	25	50	200	2[4]	4[8]
18	11000	11000	25 – **26**	62 – 65	186 – **200**	2.5[5]	3[6]
1A	11010	11010	50	50	200	1[2]	4[8]
1C	11100	11000	3 – **44**	50 – 66	150 – **200**	1.5[3]	3[6]
1D	11101	00110	33[8] – **53**	50 – 80	125 – **200**	1.5[3]	2.5[5]
1E	11110	TBD				Off	Off
1F	11111	TBD				Off	Off

Notes:
1. Caution: The PCI_SYNC_IN frequency and PLL_CFG[0 – 4] settings must be chosen such that the resulting peripheral logic/ memory bus frequency, CPU (core) frequency, and PLL (VCO) frequencies do not exceed their respective maximum or minimum operating frequencies shown in Table. Bold font numerical pairs indicate input range limit and limiting parameter.
2. The processor HID1 values only represent the multiplier of the processor's PLL (Memory to Processor Multiplier), thus multiple PC8240 PLL_CFG[0 – 4] values may have the same processor HID1 value. This implies that system software cannot read the HID1 register and associate it with a unique PLL_CFG[0 – 4] value.
3. PLL_CFG[0 – 4] settings not listed (00110, 01001, 01011, 01101, 01111, 10001, 10011, 10101, 10111, 11001, and 11011) are reserved.
4. In PLL Bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for factory use only. The AC timing specifications given in this document do not apply in PLL Bypass mode.

Figure 7-3. Example Voltage Sequencing Circuits



7.4.3 Power Supply Sizing

The power consumption numbers provided in Table do not reflect power from the OV_{DD} and GVdd power supplies which are nonnegligible for the PC8240. In typical application measurements, the OV_{DD} power ranged from 200 to 600 mW and the GVdd power ranged from 300 to 900 mW. The ranges' low end power numbers were results of the PC8240 performing cache resident integer operations at the slowest frequency combination of 33:66:166 (PCI:Mem:CPU) MHz. The OVdd high end range's value resulted from the PC8240 performing continuous flushes of cache lines with alternating ones and zeroes to PCI memory. The GVdd high end range's value resulted from the PC8240 operating at the fastest frequency combination of 66:100:200 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeroes on 64-bit boundaries to local memory.

7.4.4 Decoupling Recommendations

Due to the PC8240's dynamic power management feature, large address and data buses, and high operating frequencies, the PC8240 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC8240 system, and the PC8240 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each Vdd, OVdd, GVdd, and LVdd pin of the PC8240. It is also recommended that these decoupling capacitors receive their power from separate Vdd, OVdd, GVdd, and GND power planes in the PCB, utilizing short traces to minimize inductance. These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603, oriented such that connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd, OVdd, GVdd, and LVdd planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors – 100 – 330 µF (AVX TPS tantalum or Sanyo OSCON).

7.4.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OVdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, GVdd, LVdd and GND pins of the PC8240.

The PCI_SYNC_OUT signal is intended to be routed halfway out to the PCI devices and then returned to the PCI_SYNC_IN input of the PC8240.

The SDRAM_SYNC_OUT signal is intended to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the PC8240. The trace length may be used to skew or adjust the timing window as needed. See Freescale application note AN1794/D for more information on this topic.

7.4.6 Pull-up/Pull-down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: DH[0 – 31], DL[0 – 31], and PAR[0 – 7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (DL[0 – 31], and PAR[4 – 7]) will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

The $\overline{\text{TEST}}$[0 – 1] pins require pull-up resistors of 120Ω or less connected to OVdd.

It is recommended that $\overline{\text{TEST2}}$ have weak pull-up resistor (2 kΩ – 10 kΩ) connected to GVdd.

It is recommended that the following signals be pulled up to OVdd with weak pull-up resistors (2 kΩ – 10 kΩ): SDA, SCL, $\overline{\text{SMI}}$, $\overline{\text{SRESET}}$, TBEN, $\overline{\text{CHKSTOP\_IN}}$, TEST3, and TEST4.

It is recommended that the following PCI control signals be pulled up to LVdd with weak pull-up resistors (2 kΩ – 10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, and $\overline{\text{TRDY}}$. The resistor values may need to be adjusted stronger to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[0 – 3], $\overline{\text{REQ4}}$/DA4, TCK, TDI, TMS, and $\overline{\text{TRST}}$. See Table 1-1, “PC8240 Pinout Listing,” on page 4 for more information.

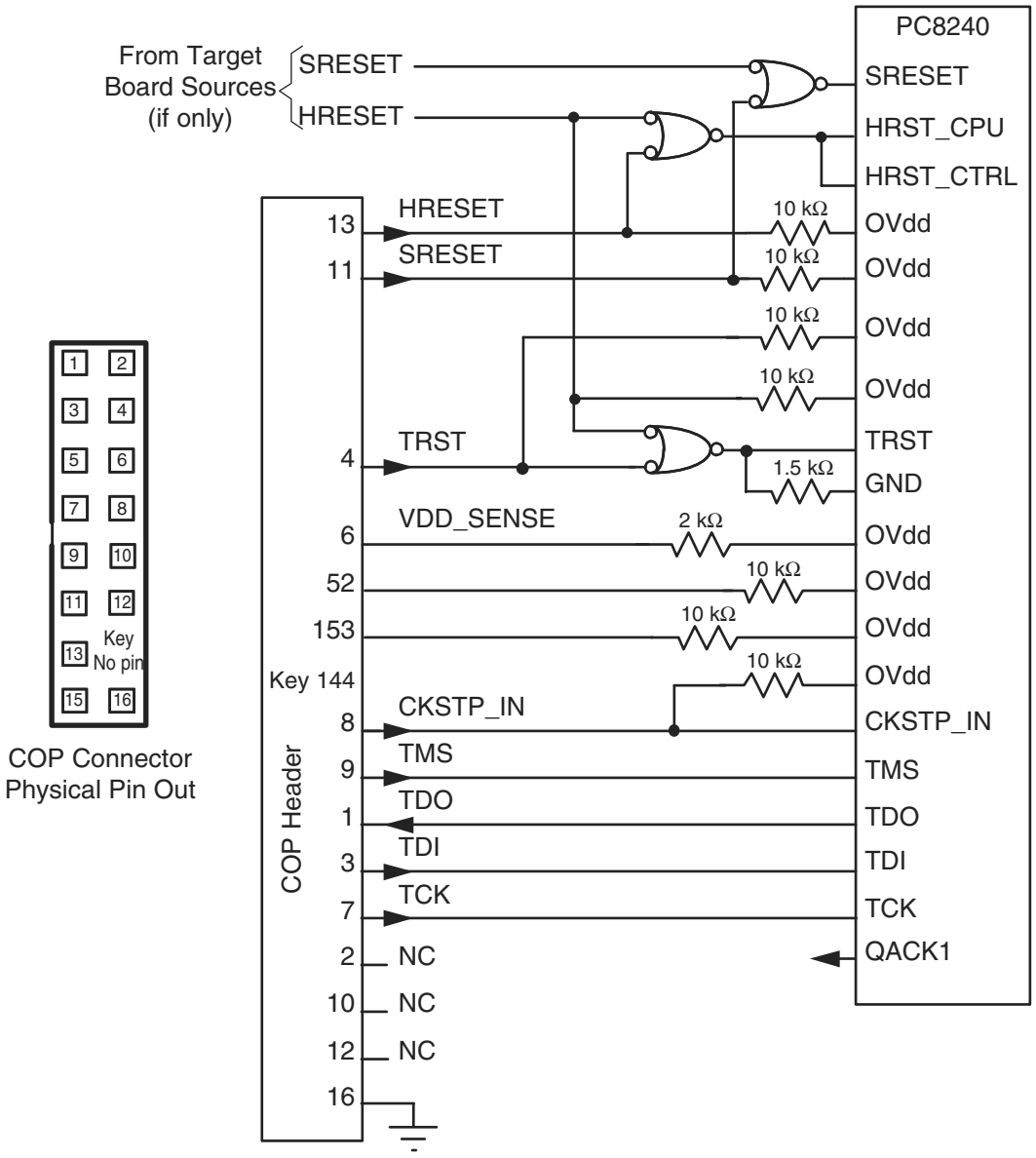
The following pins have internal pull-up resistors enabled only while device is in the reset state: $\overline{\text{GNT4}}$/DA5, DL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, MAA[0 – 2], PMAA[0 – 2]. See Table 1-1, “PC8240 Pinout Listing,” on page 4 for more information.

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, DL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0 – 2], PMAA[0 – 2], and PLL_CFG[0 – 4]/DA[10 – 6]. These pins are sampled during reset to configure the device.

Reset configuration pins should be tied to GND via 1 kΩ pull-down resistors to ensure a logic zero level is read into the configuration bits during reset if the default logic one level is not desired.

Any other unused active low input pins should be tied to a logic one level via weak pull-up resistors (2 kΩ – 10 kΩ) to the appropriate power supply listed in Table 3-2 on page 9. Unused active high input pins should be tied to GND via weak pull-down resistors (2 kΩ – 10 kΩ).

Figure 7-4. COP Connector Diagram



Notes:
1. QACK is an output on the PC8240 and is not required at the COP header for emulation.
2. RUN/STOP normally found on pin 5 of the COP header is not implemented on the PC8240. Connect pin 5 of the COP header to OVdd with a 10K pull-up resistor.
3. CKSTP_OUT normally found on pin 15 of the COP header is not implemented on the PC8240. Connect pin 15 of the COP header to OVdd with a 10K pull-up resistor.
4. Pin 14 is not physically present on the COP header
5. Component not populated.

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