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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

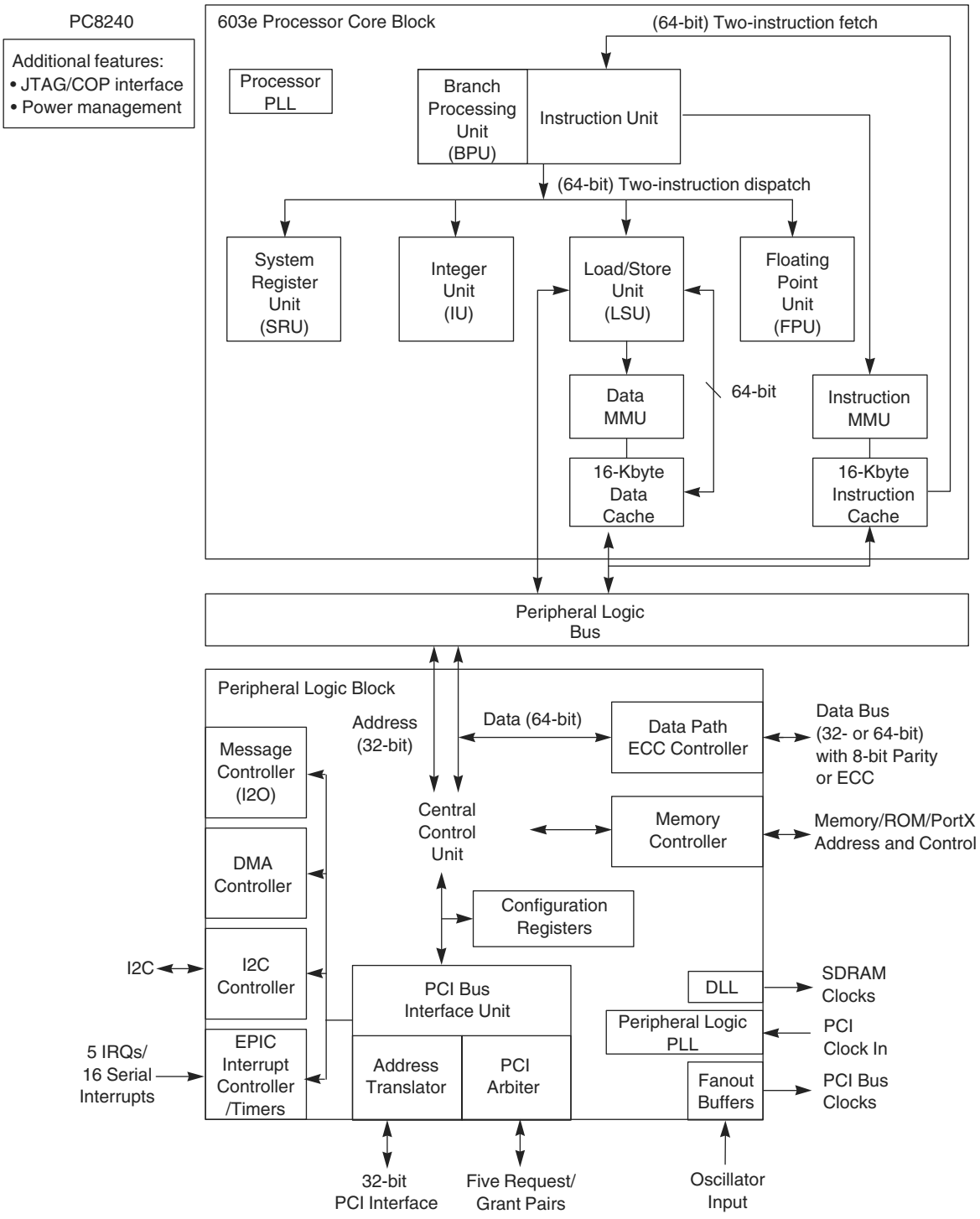
Details	
Product Status	Obsolete
Core Processor	PowerPC 603e
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TJ)
Security Features	-
Package / Case	352-LBGA
Supplier Device Package	352-TBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pcx8240vtpu200ezd3

1. General Description

1.1 Block Diagram

The PC8240 integrated processor is comprised of a peripheral logic block and a 32-bit superscalar Power Architecture 603e core, as shown in Figure 1-1.

Figure 1-1. Block Diagram



1.2 Pinout Listing

Table 1-1 provides the pinout listing for the PC8240, 352 TBGA package.

Table 1-1. PC8240 Pinout Listing

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
$\overline{C/BE}$[0 – 3]	A25 F23 K23 P25	I/O	OVdd	DRV_PCI	(6)(15)
$\overline{DEVSEL}$	H26	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{FRAME}$	J24	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{IRDY}$	K25	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{LOCK}$	J26	Input	OVdd	–	(8)
AD[0 – 31]	C22 D22 B22 B23 D19 B24 A24 B26 A26 C26 D25 D26 E23 E25 E26 F24 L26 L25 M25 M26 N23 N25 N26 R26 R25 T26 T25 U23 U24 U26 U25 V25	I/O	OVdd	DRV_PCI	(6)(15)
PAR	G25	I/O	OVdd	DRV_PCI	(15)
$\overline{GNT}$[0 – 3]	V26 W23 W24 W25	Output	OVdd	DRV_PCI	(6)(15)
$\overline{GNT4}$/DA5	W26	Output	OVdd	DRV_PCI	(7)(15)
$\overline{REQ}$[0 – 3]	AB26 AA25 AA26 Y25	Input	OVdd	–	(6)(12)
$\overline{REQ4}$/DA4	Y26	Input	OVdd	–	(12)
$\overline{PERR}$	G26	I/O	OVdd	DRV_PCI	(8)(15)(18)
$\overline{SERR}$	F26	I/O	OVdd	DRV_PCI	(8)(15)(16)
$\overline{STOP}$	H25	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{TRDY}$	K26	I/O	OVdd	DRV_PCI	(8)(15)
$\overline{INTA}$	AC26	Output	OVdd	DRV_PCI	(15)(16)
IDSEL	P26	Input	OVdd	–	–
Memory Interface Signals					
MDL[0 – 31]	AD17 AE17 AE15 AF15 AC14 AE13 AF13 AF12 AF11 AF10 AF9 AD8 AF8 AF7 AF6 AE5 B1 A1 A3 A4 A5 A6 A7 D7 A8 B8 A10 D10 A12 B11 B12 A14	I/O	GVdd	DRV_MEM_DATA	(5)(6)(13)
MDH[0 – 31]	AC17 AF16 AE16 AE14 AF14 AC13 AE12 AE11 AE10 AE9 AE8 AC7 AE7 AE6 AF5 AC5 E4 A2 B3 D4 B4 B5 D6 C6 B7 C9 A9 B10 A11 A13 B13 A15	I/O	GVdd	DRV_MEM_DATA	(6)(13)
$\overline{CAS}$/DQM[0 – 7]	AB1 AB2 K3 K2 AC1 AC2 K1 J1	Output	GVdd	DRV_MEM_ADDR	(6)
$\overline{RAS/CS}$[0 – 7]	Y4 AA3 AA4 AC4 M2 L2 M1 L1	Output	GVdd	DRV_MEM_ADDR	(6)
$\overline{FOE}$	H1	I/O	GVdd	DRV_MEM_ADDR	(3)(4)
$\overline{RCS0}$	N4	I/O	GVdd	DRV_MEM_ADDR	(3)(4)
$\overline{RCS1}$	N2	Output	GVdd	DRV_MEM_ADDR	–
SDMA[11 – 0]	N1 R1 R2 T1 T2 U4 U2 U1 V1 V3 W1 W2	Output	GVdd	DRV_MEM_ADDR	(6)(14)
SDMA12/SDBA1	P1	Output	GVdd	DRV_MEM_ADDR	(14)

Table 1-1. PC8240 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
SDBA0	P2	Output	GVdd	DRV_MEM_ADDR	–
PAR[0 – 7]	AF3 AE3 G4 E2 AE4 AF4 D2 C2	I/O	GVdd	DRV_MEM_ADDR	(6)(13)(14)
$\overline{\text{SDRAS}}$	AD1	Output	GVdd	DRV_MEM_ADDR	(3)
$\overline{\text{SDCAS}}$	AD2	Output	GVdd	DRV_MEM_ADDR	(3)
CKE	H2	Output	GVdd	DRV_MEM_ADDR	(3)(4)
$\overline{\text{WE}}$	AA1	Output	GVdd	DRV_MEM_ADDR	–
$\overline{\text{AS}}$	Y1	Output	GVdd	DRV_MEM_ADDR	(3)(4)
EPIC Control Signals					
IRQ_0/S_INT	C19	Input	OVdd	–	–
IRQ_1/S_CLK	B21	I/O	OVdd	DRV_PCI	–
IRQ_2/S_RST	AC22	I/O	OVdd	DRV_PCI	–
IRQ_3/$\overline{\text{S\_FRAME}}$	AE24	I/O	OVdd	DRV_PCI	–
IRQ_4/$\overline{\text{L\_INT}}$	A23	I/O	OVdd	DRV_PCI	–
Two-wire Interface Control Signals					
SDA	AE20	I/O	OVdd	DRV_STD	(10)(16)
SCL	AF21	I/O	OVdd	DRV_STD	(10)(16)
Clock Out Signals					
PCI_CLK[0 – 3]	AC25 AB25 AE26 AF25	Output	GVdd	DRV_PCI_CLK	(6)
PCI_CLK4/DA3	AF26	Output	GVdd	DRV_PCI_CLK	–
PCI_SYNC_OUT	AD25	Output	GVdd	DRV_PCI_CLK	–
PCI_SYNC_IN	AB23	Input	GVdd	–	–
SDRAM_CLK[0 – 3]	D1 G1 G2 E1	Output	GVdd	DRV_MEM_ADDR	(6)
SDRAM_SYNC_OUT	C1	Output	GVdd	DRV_MEM_ADDR	–
SDRAM_SYNC_IN	H3	Input	GVdd	–	–
CKO/DA1	B15	Output	OVdd	DRV_STD	–
OSC_IN	AD21	Input	OVdd	–	–
Miscellaneous Signals					
$\overline{\text{HRST\_CTRL}}$	A20	Input	OVdd	–	–
$\overline{\text{HRST\_CPU}}$	A19	Input	OVdd	–	–
$\overline{\text{MCP}}$	A17	Output	OVdd	DRV_STD	(3)(4)(17)
NMI	D16	Input	OVdd	–	–
$\overline{\text{SMI}}$	A18	Input	OVdd	–	(10)
$\overline{\text{SRESET}}$	B16	Input	OVdd	–	(10)
TBEN	B14	Input	OVdd	–	(10)
$\overline{\text{QACK}}$/DA0	F2	Output	OVdd	DRV_STD	(3)(4)
$\overline{\text{CHKSTOP\_IN}}$	D14	Input	OVdd	–	(10)
MAA[0 – 2]	AF2 AF1 AE1	Output	–	DRV_MEM_DATA	(3)(4)(6)

Table 1-1. PC8240 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
Manufacturing Pins					
DA2	C25	I/O	OVdd	DRV_PCI	(2)
DA[11 — 13]	AD26 AF17 AF19	I/O	OVdd	DRV_PCI	(2)(6)
DA[14 — 15]	F1 J2	I/O	GVdd	DRV_MEM_ADDR	(2)(6)

Notes:
1. Place pull-up resistors of 120Ω or less on the $\overline{\text{TEST}}$[0 – 1] pins.
2. Treat these pins as No Connects unless using debug address functionality.
3. This pin has an internal pull-up resistor which is enabled only when the PC8240 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a "1" is read into configuration bits during reset.
4. This pin is a reset configuration pin.
5. DL[0] is a reset configuration pin and has an internal pull-up resistor which is enabled only when the PC8240 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to insure that a "1" is read into configuration bits during reset.
6. Multi-pin signals such as AD[0 – 31] or DL[0 – 31] have their physical package pin numbers listed in order corresponding to the signal names. Ex: AD0 is on pin C22, AD1 is on pin D22,... AD31 is on pin V25.
7. $\overline{\text{GNT4}}$ is a reset configuration pin and has an internal pull-up resistor which is enabled only when the PC8240 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to insure that a "1" is read into configuration bits during reset.
8. Recommend a weak pull-up resistor (2 kΩ – 10 kΩ) be placed on this PCI control pin to LVdd.
9. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 4-1, “DC Electrical Specifications,” on page 17.
10. Recommend a weak pull-up resistor (2 kΩ – 10 kΩ) be placed on this pin to OVdd.
11. Recommend a weak pull-up resistor (2 kΩ – 10 kΩ) be placed on this pin to GVdd.
12. This pin has an internal pull-up resistor; the value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
13. Output Valid specifications for this pin are memory interface mode dependent (Registered or Flow-through), see Table 4-6, “Output AC Timing Specifications,” on page 24.
14. Non-DRAM Access Output Valid specification applies to this pin during non-DRAM accesses, see specification 12b3 in Table 4-6, “Output AC Timing Specifications,” on page 24.
15. This pin is affected by programmable PCI_HOLD_DEL parameter, see “PCI Signal Output Hold Timing” on page 25.
16. This pin is an open drain signal.
17. This pin can be programmed to be driven (default) or can be programmed to be open drain; see PMCR2 register description in the Freescale PC8240 User’s Manual for details.
18. This pin is a Sustained Tri-State pin as defined by the PCI Local Bus Specification.

2. Detailed Specification

This drawing describes the specific requirements for the PC8240 processor, in compliance with e2v standard screening.

3. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics.
2. MIL-PRF-38535: General specifications for microcircuits.

The microcircuits are in accordance with the applicable documents and as specified herein.

3.1 Design and Construction

3.1.1 Terminal Connections

The terminal connections are shown in Table 1-1, “PC8240 Pinout Listing,” on page 4.

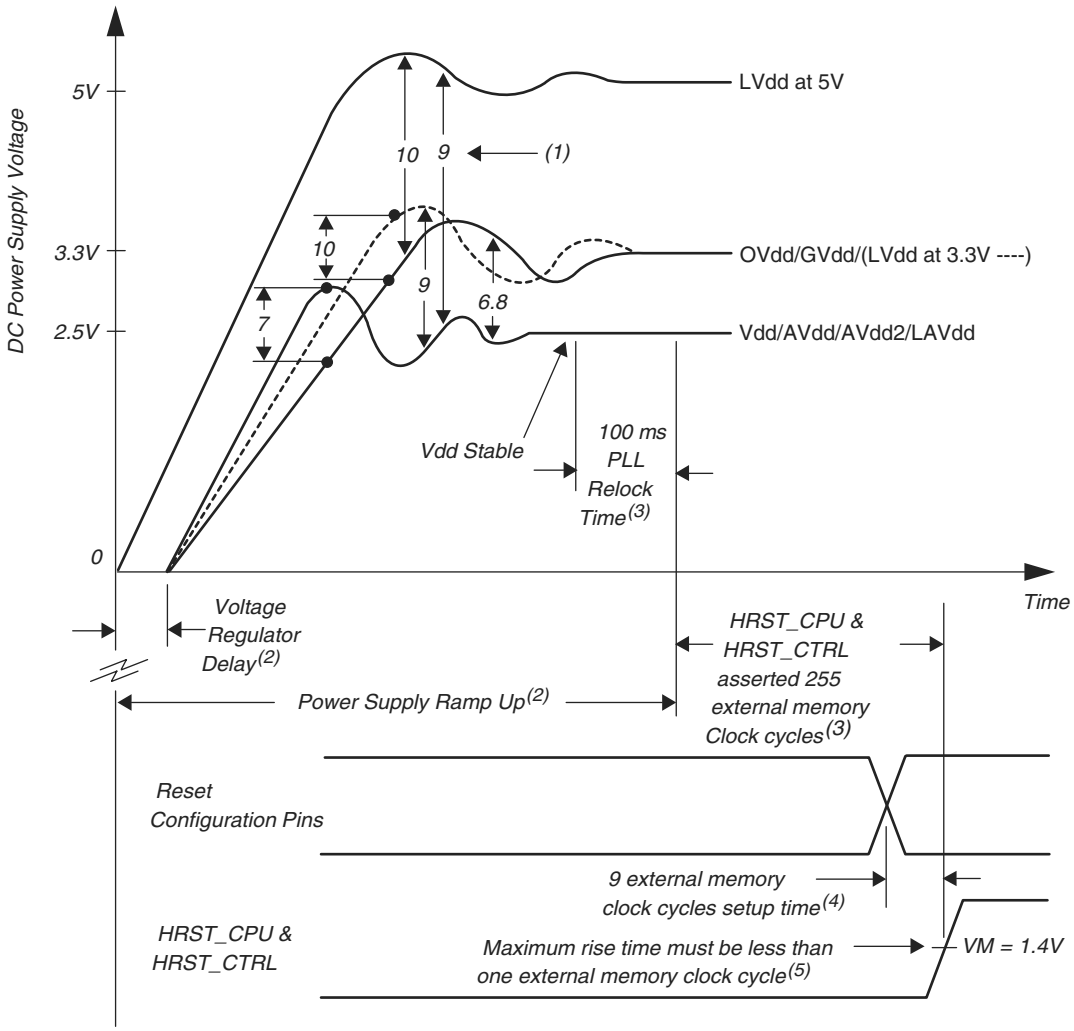
3.2 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings

Symbol	Characteristic(1)	Value	Unit
Vdd	Supply Voltage – CPU Core and Peripheral Logic	–0.3 to 2.75	V
GVdd	Supply Voltage – Memory Bus Drivers	–0.3 to 3.6	V
OVdd	Supply Voltage – PCI and Standard I/O Buffers	–0.3 to 3.6	V
AVdd/AVdd2/LAVdd	Supply Voltage – PLLs and DLL	–0.3 to 2.75	V
V_{IN}	Supply Voltage – PCI Reference	–0.3 to 3.6	V
LVdd	Input Voltage(2)	–0.3 to 5.4	V
T_{STG}	Storage Temperature Range	–55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 3-2. Absolute maximum ratings are stress ratings only and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LVdd = 5V 5% V DC may be correspondingly stressed at voltages exceeding LVdd + 0.5V DC.

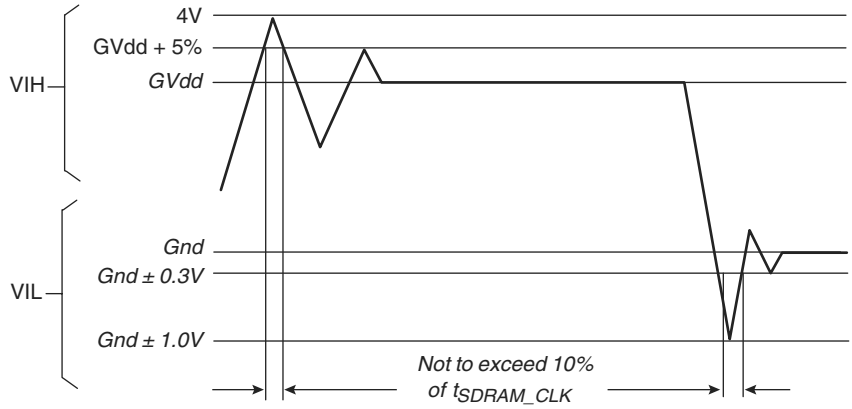
Figure 3-1. Supply Voltage Sequencing and Separation Cautions



Notes:
1. Numbers associated with waveform separations correspond to caution numbers listed in Table 3-2, “Recommended Operating Conditions,” on page 9.
2. Refer to “Power Supply Voltage Sequencing” on page 37 for additional information.
3. Refer to Table 4-4 on page 20 for additional information on PLL Relock and reset signal assertion timing requirements.
4. Refer to Table 4-5 on page 22 for additional information on reset configuration pin setup timing requirements.
5. $\overline{\text{HRST\_CPU/HRST\_CTRL}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the non-reset state.

Figure 3-2 shows the undershoot and overshoot voltage of the memory interface of the PC8240.

Figure 3-2. Overshoot/Undershoot Voltage



3.4 Thermal Information

3.4.1 Thermal Characteristics

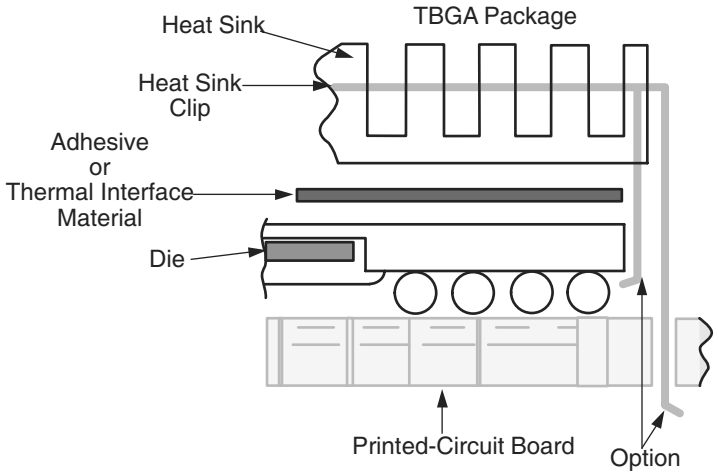
Table 3-3. Package Thermal Characteristics

Symbol	Characteristic	Min	Unit
θ_{JC}	Die Junction-to-Case Thermal Resistance	1.8	°C/W
θ_{JB}	Die Junction-to-Board Thermal Resistance	4.8	°C/W

3.4.2 Thermal Management Information

This section provides thermal management information for the tape ball grid array (TBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design, the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods-adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 3-3.

Figure 3-3. Package Exploded Cross-Sectional View with Several Heat Sink Options

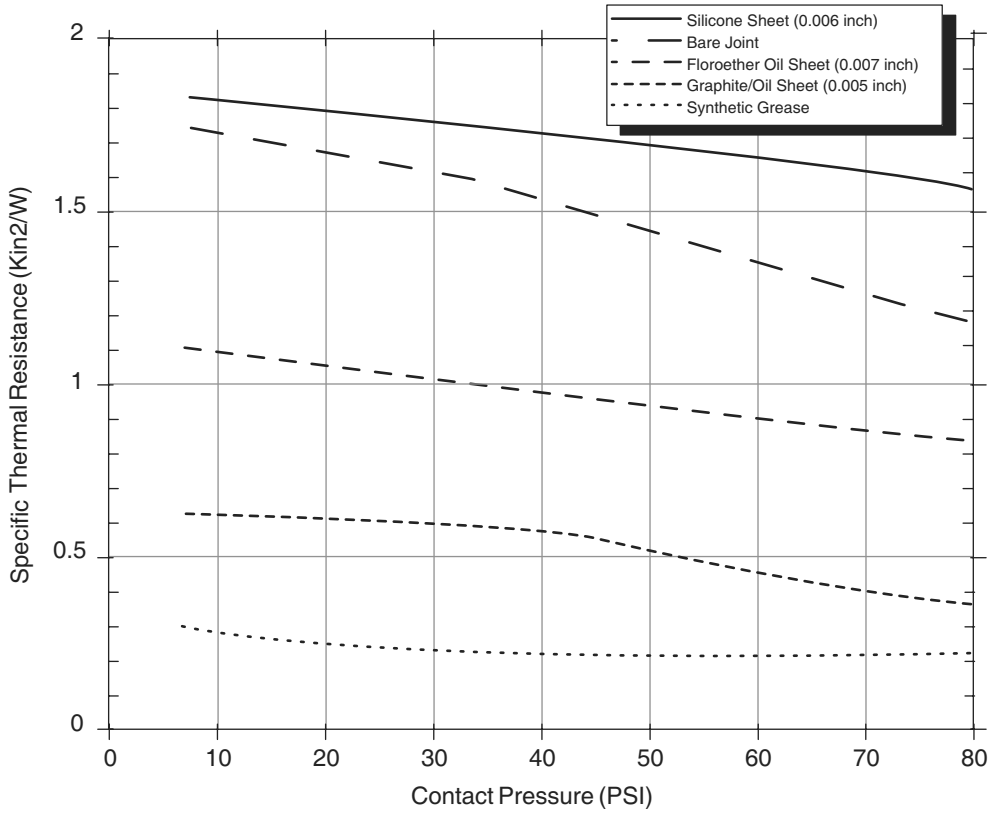


3.4.4 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 3-6 shows the thermal performance of three thinsheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 3-5). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors, thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

Figure 3-6. Thermal Performance of Select Thermal Interface Material



The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature-airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.

3.5 Power Consideration

Table 3-4 provides **preliminary** power consumption data for the PC8240.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 3-4. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)				Unit	Notes
	33/66/166	33/66/200	33/100/200	66/100/200		
Typical	2.5	2.8	3.0	3.0	W	(1)(5)
Max – FP	3.0	3.4	3.6	3.6	W	(1)(2)
Max – INT	2.7	3.0	3.3	3.4	W	(1)(3)
Doze	1.8	2.0	2.2	2.2	W	(1)(4)(6)
Nap	700	700	900	900	mW	(1)(4)(6)
Sleep	500	500	500	800	mW	(1)(4)(6)

I/O Power Supplies				
Mode	**Minimum**	**Maximum**	**Unit**	**Notes**
Typ – OVdd	200	600	mW	(7)(8)
Typ – GVdd	300	900	mW	(7)(9)

Notes:
1. The values include Vdd, AVdd, AVdd2, and LVdd but do not include I/O Supply Power, see "Power Supply Sizing" on page 38 for information on OVdd and GVdd supply power.
2. Maximum – FP power is measured at Vdd = 2.625V with dynamic power management enabled while running an entirely cacheresident, looping, floating point multiplication instruction.
3. Maximum – INT power is measured at Vdd = 2.625V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at Vdd = 2.625V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at Vdd = AVdd = 2.5V, OVdd = 3.3V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeroes on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.

7. The typical minimum I/O power values were results of the PC8240 performing cache resident integer operations at the slowest frequency combination of 33:66:166 (PCI:Mem:CPU) MHz.
8. The typical maximum OVdd value resulted from the PC8240 operating at the fastest frequency combination of 66:100:200 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeroes to PCI memory.
9. The typical maximum GVdd value resulted from the PC8240 operating at the fastest frequency combination of 66:100:200 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeroes on 64-bit boundaries to local memory.

Note: To calculate the power consumption at low temperature (–55°C), use a 1.25 factor.

3.6 Marking

The document where markings are defined is identified in the related reference documents. Each microcircuit is legible and permanently marked with the following information as minimum:

- e2v Logo,
- Manufacturer's part number, Date-code of inspection lot,
- ESD identifier if available,
- Country of manufacturing.

4. Electrical Characteristics

4.1 Static Characteristics

Table 4-1 provides the DC electrical characteristics for the PC8240.

At recommended operating conditions (see Table 3-2 on page 9)

Table 4-1. DC Electrical Specifications

Characteristics[1]	Conditions[4]	Symbol	Value		Unit
			Min	Max	
Input High Voltage	PCI only	V_{IH}	0.5*OVdd	LVdd	V
Input Low Voltage	PCI only	V_{IL}	–	0.3*OVdd	V
Input High Voltage	All other pins (GVdd = 3.3V)	V_{IH}	2.0	3.3	V
Input High Voltage	All other pins (GVdd = 2.5V)	V_{IH}	1.8	2.5	V
Input Low Voltage	All inputs except OSC_IN	V_{IL}	GND	0.8	V
PCI_SYNC_IN Input High Voltage		CV_{IH}	0.5*OVdd	–	V
PCI_SYNC_IN Input Low Voltage		CV_{IL}	GND	0.3*OVdd	V
Input Leakage Current[5] for pins using DRV_PCI driver	0.5V V_{IN} 2.7V at LVdd = 4.75	I_L	–	70	A
Input Leakage Current[5] for pins using DRV_PCI driver	0.5V V_{IN} 5.5V at LVdd = 5.5	I_L	–	TBD	A
Input Leakage Current[5] all others	LVdd = 3.6V GVdd = 3.465	I_L	–	10	A
Output High Voltage	I_{OH} = N/A (GVdd = 3.3V)[3]	V_{OH}	2.4	–	V
Output Low Voltage	I_{OL} = N/A (GVdd = 3.3V)[3]	V_{OL}	–	0.4	V

Table 4-1. DC Electrical Specifications (Continued)

Characteristics[1]	Conditions[4]	Symbol	Value		Unit
			Min	Max	
Output High Voltage	I_{OH} = N/A (GVdd = 2.5V)[3]	V_{OH}	1.85	–	V
Output Low Voltage	I_{OL} = N/A (GVdd = 2.5V)[3]	V_{OL}	–	0.6	V
Capacitance[2]	V_{IN} = 0V, f = 1 MHz	C_{IN}	–	7.0	pF

Notes: 1. See Table 1-1 on page 4 for pins with internal pull-up resistors.
2. Capacitance is periodically sampled rather than 100% tested.
3. See Table 4-2 on page 18 for the typical drive capability of a specific signal pin based upon the type of output driver associated with that pin as listed in.
4. These specifications are for the default driver strengths indicated in Table.
5. Leakage current is measured on input pins and on output pins in the high impedance state. The leakage current is measured for nominal OVdd/LVdd and Vdd or both Ovdd/LVdd and Vdd must vary in the same direction.

Table 4-2 provides information on the characteristics of the output drivers referenced in. The values are from the PC8240 IBIS model (v1.0) and are not tested, for additional detailed information see the complete IBIS model listing at http://www.mot.com/SPS/PowerPC/ teksupport/tools/IBIS/kahlua_1.ibs.txt

Table 4-2. Drive Capability of PC8240 Output Pins

Driver Type	Programmable Output Impedance (Ohms)	Supply Voltage (V)	I_{OH}	I_{OL}	Unit	Notes
DRV_STD	20	OVdd = 3.3	TBD	TBD	mA	(2)(5)
	40 (default)	OVdd = 3.3	TBD	TBD	mA	(2)(5)
DRV_PCI	25	LVdd = 3.3	11.0	20.6	mA	(1)(4)
		LVdd = 5.0	5.6	10.3	mA	(1)(4)
	50 (default)	LVdd = 3.3	5.6	10.3	mA	(1)(4)
		LVdd = 5.0	5.6	10.3	mA	(1)(4)
DRV_MEM_ADDR DRV_PCI_CLK	8 (default)	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	89.0	73.3	mA	(2)(5)
	13.3	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	55.9	46.4	mA	(2)(5)
	20	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	36.7	30.0	mA	(2)(5)
	40	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	TBD	TBD	mA	(2)(5)
DRV_MEM_DATA	20 (default)	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	36.7	30.0	mA	(2)(5)
	40	GVdd = 2.5	TBD	TBD	mA	(3)(6)
		GVdd = 3.3	18.7	15.0	mA	(2)(5)

Notes: 1. For DRV_PCI, I_{OH} read from the listing in the pull-up mode, I(Min) column, at the 0.33V label by interpolating between the 0.3V and 0.4V table entries' current values which correspond to the PCI V_{OH} = 2.97 = 0.9*LVdd (LVdd = 3.3V) where Table Entry Voltage = LVdd - PCI V_{OH}.

4.2.2 Input AC Timing Specifications

Table 4-5 provides the input AC timing specifications. See Figure 4-3 on page 22 and Figure 4-4 on page 23.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 4-5. Input AC Timing Specifications

Num	Characteristics	Min	Max	Unit	Notes
10a	PCI Input Signals Valid to PCI_SYNC_IN (Input Setup)	2.0	–	ns	(2)(3)
10b1	Memory Control and Data Input Signals in Flow Through Mode Valid to SDRAM_SYNC_IN (Input Setup)	4.0	–	ns	(1)(3)
10b2	Memory Control and Data Input Signals in Registered Mode Valid to SDRAM_SYNC_IN (Input Setup)	TBD	–	ns	(1)(3)
10c	Epic, Misc. Debug Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	TBD	–	ns	(1)(3)
10d	Two-wire Interface Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	TBD	–	ns	(1)(3)
10e	Mode select Inputs Valid to HRST_CPU/HRST_CTRL (Input Setup)	$9*t_{CLK}$	–	ns	(1)(3)(5)
11a	PCI_SYNC_IN (SDRAM_SYNC_IN) to Inputs Invalid (Input Hold)	1.0	–	ns	(1)(2)(3)
11b	$\overline{\text{HRST\_CPU/HRST\_CTRL}}$ to Mode select Inputs Invalid (Input Hold)	TBD	–	ns	(1)(3)(5)

Notes:
1. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0V) of the signal in question to the V_M = 1.4V of the rising edge of the memory bus clock, SDRAM_SYNC_IN. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 4-3 on page 22.
2. All PCI signals are measured from OVdd/2 of the rising edge of PCI_SYNC_IN to 0.4*OVdd of the signal in question for 3.3V PCI signaling levels. See Figure 4-4.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0V) of the signal in question to the V_M = 1.4V of the rising edge of the $\overline{\text{HRST\_CPU/HRST\_CTRL}}$ signal. See Figure 4-5.

Figure 4-3. Input – Output Timing Diagram Referenced to SDRAM_SYNC_IN

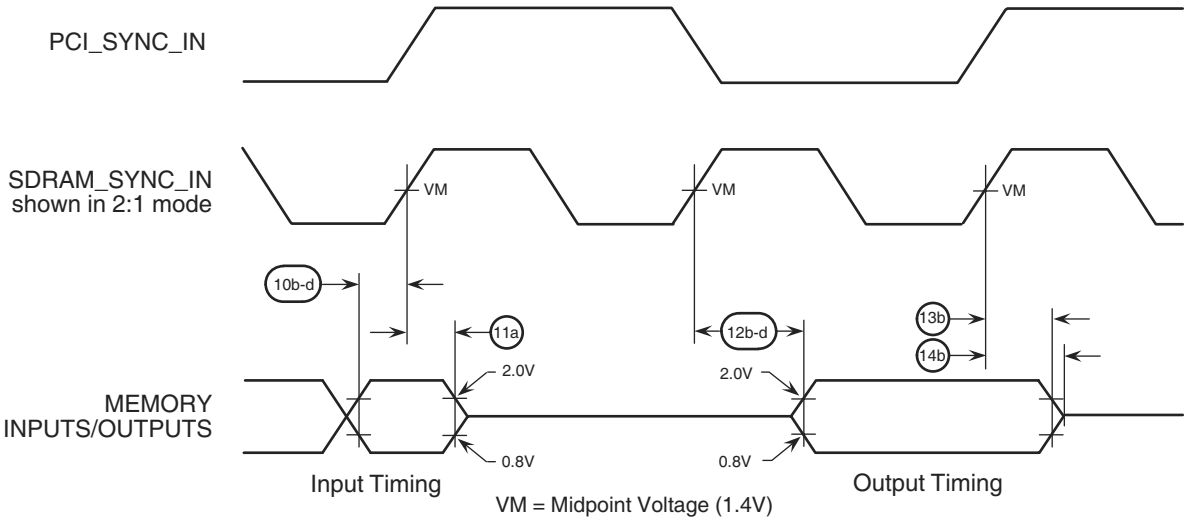


Figure 4-7. PCI_HOLD_DEL Affect on Output Valid and Hold Time

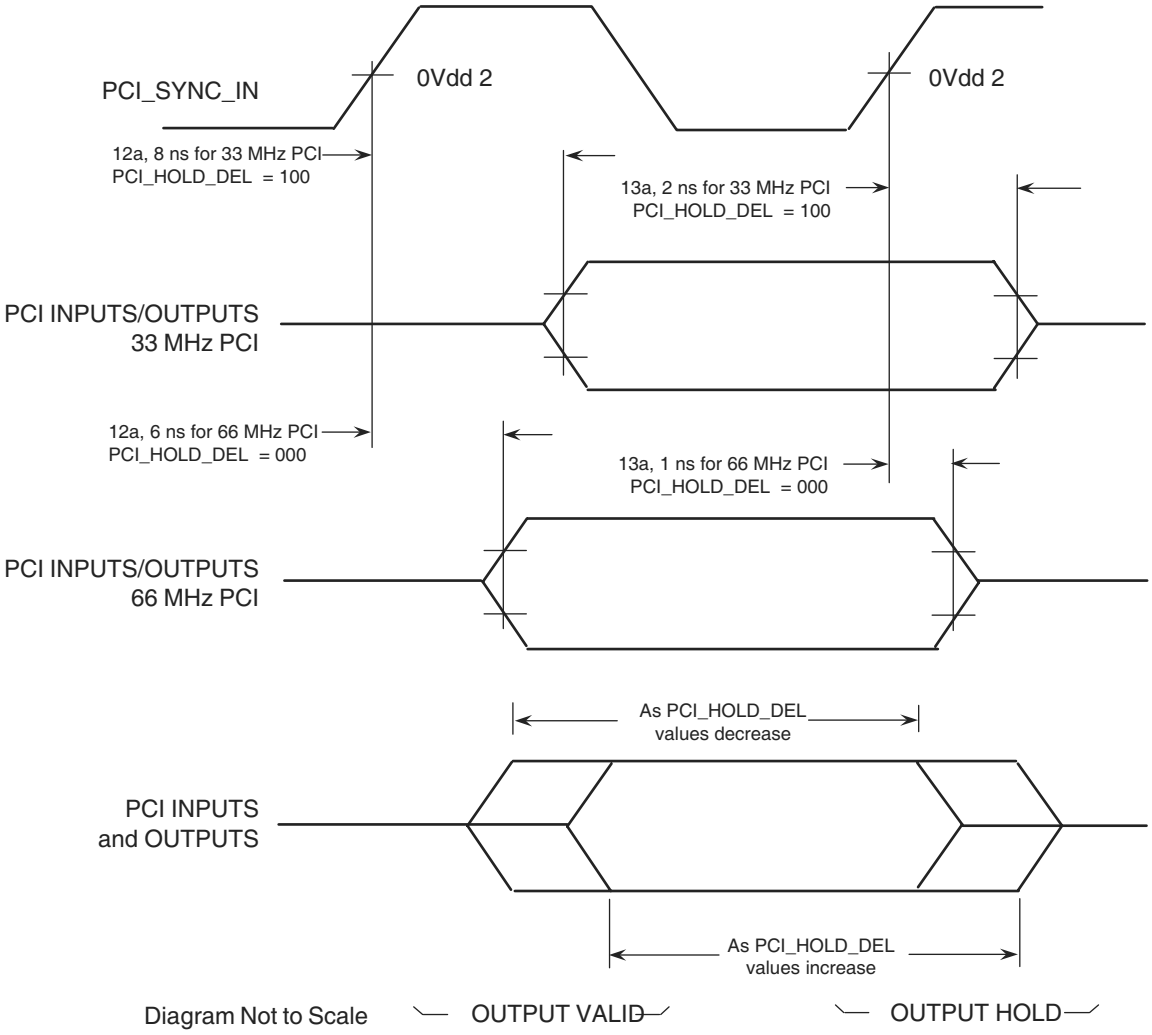


Table 4-10 provides the two-wire interface output AC timing specifications for the PC8240.

At recommended operating conditions (see Table 3-2 on page 9) with GVdd = 3.3V ± 5% and LVdd = 3.3V ± 5%

Table 4-10. Two-wire Interface Output AC Timing Specifications

Num	Characteristics	Min	Max	Unit	Notes
1	Start condition hold time	(FDR[5] == 0) x (D_{FDR}/16)/2N + (FDR[5] == 1) x (D_{FDR}/16)/2M	–	CLKs	(1)(2)(5)
2	Clock low period	D_{FDR}/2	–	CLKs	(1)(2)(5)
3	SCL/SDA rise time (from 0.5V to 2.4V)	–	–	mS	(3)
4	Data hold time	8.0 + (16 x $2^{FDR[4:2]}$) x (5 - 4({FDR[5],FDR[1]} == b'10) - 3({FDR[5],FDR[1]} == b'11) - 2({FDR[5],FDR[1]} == b'00) - 1({FDR[5],FDR[1]} == b'01))	–	CLKs	(1)(2)(5)
5	SCL/SDA fall time (from 2.4V to 0.5V)		< 5	ns	(4)
6	Clock high time	D_{FDR}/2	–	CLKs	(1)(2)(5)
7	Data setup time (PC8240 as a master only)	(D_{FDR}/2) - (Output data hold time)	–	CLKs	(1)(5)
8	Start condition setup time (for repeated start condition only)	D_{FDR} + (Output start condition hold time)	–	CLKs	(1)(2)(5)
9	Stop condition setup time	4.0	–	CLKs	(1)(2)

Notes:
1. Units for these specifications are in SDRAM_CLK units.
2. The actual values depend on the setting of the Digital Filter Frequency Sampling Rate (DFFSR) bits in the Frequency Divider Register I2CFDR. Therefore, the noted timings in the above table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the two-wire interface bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK clock times DFFSR times 2 plus 1 SDRAM_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 4-9 on page 30.
3. Since SCL and SDA are open-drain type outputs, which the PC8240 can only drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
4. Specified at a nominal 50 pF load.
5. D_{FDR} is the decimal divider number indexed by FDR[5:0] value. Refer to the two-wire interface Interface chapter's Serial Bit Clock Frequency Divider Selections table. FDR[x] refers to the Frequency Divider Register I2CFDR bit x. N is equal to a variable number that would make the result of the divide (Data Hold Time value) equal to a number less than 16. M is equal to a variable number that would make the result of the divide (Data Hold Time value) equal to a number less than 9.

Figure 4-8. Two-wire Interface Timing Diagram I

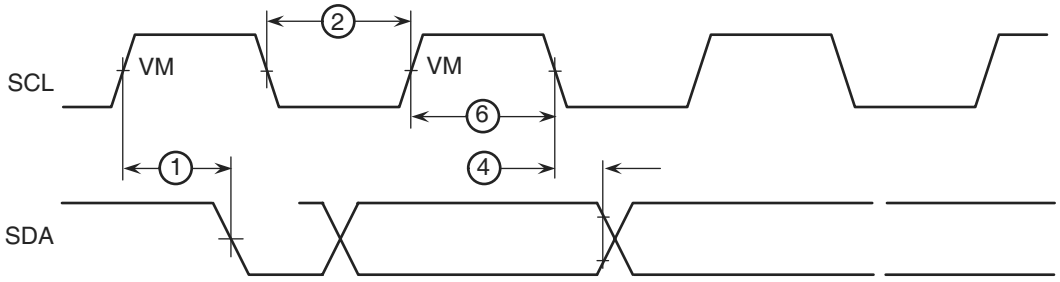


Figure 4-15. JTAG TRST Timing Diagram

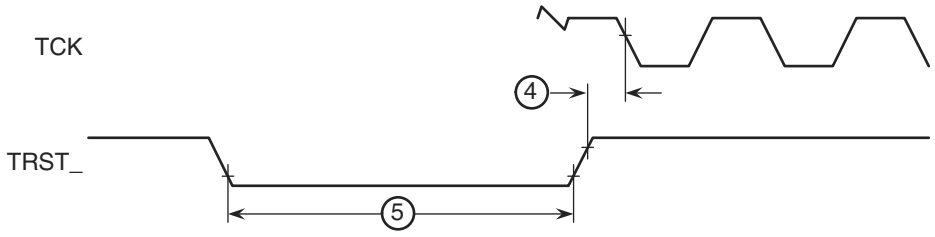


Figure 4-16. JTAG Boundary Scan Timing Diagram

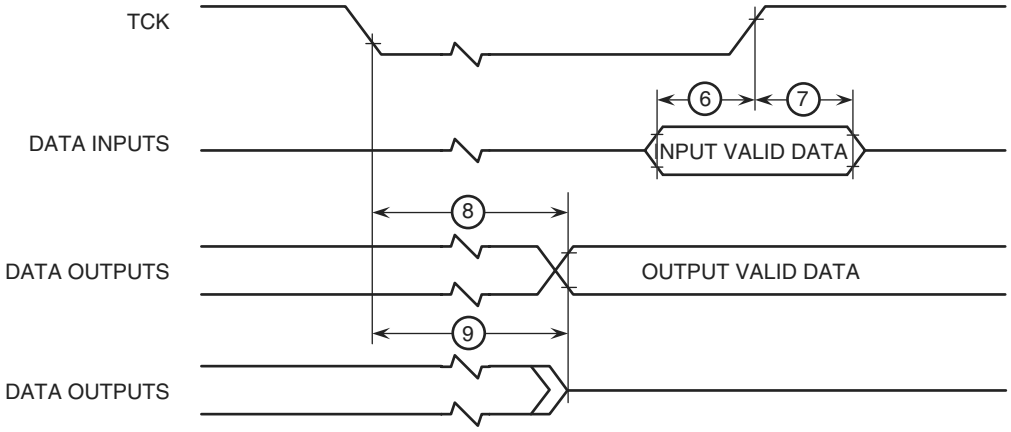
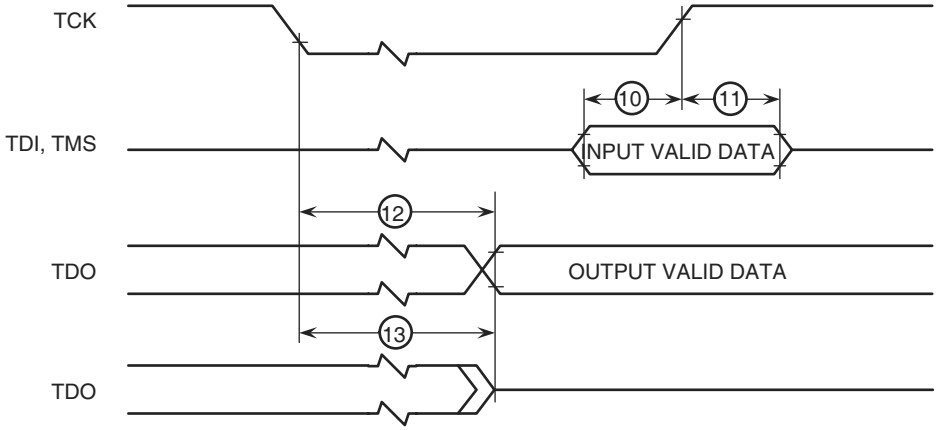


Figure 4-17. Test Access Port Timing Diagram



5. Preparation for Delivery

5.1 Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

5.2 Certificate of Compliance

e2v offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 and guaranteeing the parameters not tested at temperature extremes for the entire temperature range.

6. Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces.
- Ground test equipment, tools and operator.
- Do not handle devices by the leads.
- Store devices in conductive foam or carriers.
- Avoid use of plastic, rubber or silk in MOS areas.
- Maintain relative humidity above 50% if practical.

7. Package Description

7.1 Package Parameters

The PC8240 uses a 35 mm x 35 mm, cavity down, 352 pin Tape Ball Grid Array (TBGA) package. The package parameters are as provided in the following list.

Table 7-1. Package Parameters

Parameter	
Package Outline	35 mm x 35 mm
Interconnects	352
Pitch	1.27 mm
Solder Balls	63/37 Sn/Pb
Solder Balls Diameter	0.75 mm
Maximum Module Height	1.65 mm
Co-planarity Specification	0.15 mm
Maximum Force	6.0 lbs. total, uniformly distributed over package (8 grams/ball)

7.3 PLL Configuration

The PC8240's internal PLLs are configured by the PLL_CFG[0–4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the Peripheral Logic/Memory Bus PLL (VCO) frequency of operation for the PCI-to-Memory frequency multiplying and the 603e CPU PLL (VCO) frequency of operation for Memory-to-CPU frequency multiplying. The PLL configuration for the PC8240 is shown in Table 7-2.

Table 7-2. PC8240 Microprocessor PLL Configuration

			200 MHz Part[9]			Ratios [4][5]	
Ref	PLL_ CFG [0 – 4][1][3]	CPU HID1 [0 – 4][2]	PCI Clock Input (PCI_SYNC_IN) Range[1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO) Multiplier	Mem to CPU (CPU VCO) Multiplier
0	00000	00110	25 – **26**	75 – 80	188 – **200**	3[6]	2.5[5]
1	00001	TBD	NOT USABLE			3[6]	3[6]
2	00010	TBD	50 – 56[6]	50 – 56	100 – 112	1[4]	2[8]
3	00011	TBD	Bypass			Bypass	2[8]
4	00100	00101	25 – 28[6]	50 – 56	100 – 113	2[8]	2[8]
5	00101	TBD	Bypass			Bypass	2.5[5]
7	00111	TBD	Bypass			Bypass	3[6]
8	01000	11000	33[7] – 56[6]	33 – 56	100 – 168	1[4]	3[6]
A	01010	TBD	NOT USABLE			2[4]	4.5[9]
C	01100	00110	25 – **40**	50 – 80	125 – **200**	2[4]	2.5[5]
E	01110	11000	25 – **33**	50 – 66	150 – **200**	2[4]	3[6]
10	10000	00100	25 – **33**	75 – 100	150 – **200**	3[6]	2[4]
12	10010	00100	33[8] – **66**	50 – 100	100 – **200**	1.5[3]	2[4]
14	10100	11110	25 – **28**	50 – 56	175 – **200**	2[4]	3.5[7]
16	10110	11010	25	50	200	2[4]	4[8]
18	11000	11000	25 – **26**	62 – 65	186 – **200**	2.5[5]	3[6]
1A	11010	11010	50	50	200	1[2]	4[8]
1C	11100	11000	3 – **44**	50 – 66	150 – **200**	1.5[3]	3[6]
1D	11101	00110	33[8] – **53**	50 – 80	125 – **200**	1.5[3]	2.5[5]
1E	11110	TBD				Off	Off
1F	11111	TBD				Off	Off

Notes:
1. Caution: The PCI_SYNC_IN frequency and PLL_CFG[0 – 4] settings must be chosen such that the resulting peripheral logic/ memory bus frequency, CPU (core) frequency, and PLL (VCO) frequencies do not exceed their respective maximum or minimum operating frequencies shown in Table. Bold font numerical pairs indicate input range limit and limiting parameter.
2. The processor HID1 values only represent the multiplier of the processor's PLL (Memory to Processor Multiplier), thus multiple PC8240 PLL_CFG[0 – 4] values may have the same processor HID1 value. This implies that system software cannot read the HID1 register and associate it with a unique PLL_CFG[0 – 4] value.
3. PLL_CFG[0 – 4] settings not listed (00110, 01001, 01011, 01101, 01111, 10001, 10011, 10101, 10111, 11001, and 11011) are reserved.
4. In PLL Bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for factory use only. The AC timing specifications given in this document do not apply in PLL Bypass mode.

7.4.7 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. (BSDL descriptions of the PC8240 are available on the internet at www.mot.com/SPS/PowerPC/teksupport/tools/BSDL/) The TRST signal is optional in the IEEE 1149.1 specification but is provided on all Power Architecture implementations. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the TRST signal is asserted during power-on reset. Since the JTAG interface is also used for accessing the common on-chip processor (COP) function of Power Architecture processors, simply tying TRST to HRST_CPU/HRST_CTRL is not practical. Note that the two hard reset signals on the PC8240 (HRST_CPU and HRST_CTRL) must be asserted and negated together to guarantee normal operation.

The common on-chip processor (COP) function of Power Architecture processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRST_CPU/HRST_CTRL or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 7-4 allows the COP to independently assert HRST_CPU/HRST_CTRL or TRST while ensuring that the target can drive HRST_CPU/HRST_CTRL as well. The shown COP header, adds many benefits including breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface. Availability of these features can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025” square-post 0.100” centered header assembly (often called a “Berg” header). The connector typically has pin 14 removed as a connector key, as shown in Figure 7-4.

There is no standardized way to number the COP header shown in Figure 7-4 on page 41; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin one (as with an IC). Regardless of the numbering, the signal placement recommended in is common to all known emulators.

8. Definitions

8.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

9. Ordering Information

xx	8240	y	xx	x	n	x	(ZD3)
Product Code (1)	Part Identifier	Temperature Range: T_C (1)	Package (1)	Screening Level (1)	Max Internal Processor Speed (1)	Revision Level	Extended temperature
PC(X) (2)	8240	V: -40˚C, +110˚C	TP: TBGA	U: Upscreening	200: 200 MHz	E	TC = -40˚C to 125˚C

Notes: 1. For availability of the different versions, contact your local e2v sales office.

2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

10. Document Revision History

Table 10-1 provides a revision history for this hardware specification.

Table 10-1. Document Revision History

Revision Number	Date	Substantive Change(s)
C	07/2007	Name change from Atmel to e2v Ordering information update

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