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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	38 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f510-e-sn



PIC12F510/16F506

8/14-Pin, 8-Bit Flash Microcontroller

Devices Included In This Data Sheet:

- PIC16F506
- PIC12F510

High-Performance RISC CPU:

- Only 33 Single-Word Instructions to Learn
- All Single-Cycle Instructions except for Program Branches, which are Two-Cycle
- 12-Bit Wide Instructions
- Two-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- 8-Bit Wide Data Path
- 10 Special Function Hardware Registers (PIC12F510)
- 13 Special Function Hardware Registers (PIC16F506)
- Operating Speed:
 - DC – 8 MHz Crystal Oscillator (PIC12F510)
 - DC – 500 ns instruction cycle (PIC12F510)
 - DC – 20 MHz Crystal Oscillator (PIC16F506)
 - DC – 200 ns instruction cycle (PIC16F506)

Special Microcontroller Features:

- 4 or 8 MHz Selectable Precision Internal Oscillator:
 - Factory calibrated to $\pm 1\%$
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debugging (ICD) Support
- Power-on Reset (POR)
- Device Reset Timer (DRT):
 - Short DRT (1.125 ms, typical) for INTOSC, EXTRC and EC
 - DRT (18 ms, typical) for HS, XT and LP
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed $\overline{\text{MCLR}}$ Input Pin
- Selectable Internal Weak Pull-Ups on I/O Pins
- Power-Saving Sleep mode
- Wake-up from Sleep on Pin Change
- Wake-up from Sleep on Comparator Change

- Selectable Oscillator Options:
 - INTOSC: 4/8 MHz precision Internal oscillator
 - EXTRC: External low-cost RC oscillator
 - XT: Standard crystal/resonator
 - LP: Power-saving, low-frequency crystal
 - HS: High-speed crystal/resonator (PIC16F506 only)
 - EC: High-speed external clock input (PIC16F506 only)
- Analog-to-Digital (A/D) Converter:
 - 8-bit resolution
 - 4-input channels (1 channel is dedicated to conversion of the internal 0.6V absolute voltage reference)
- High Current Sink/Source for Direct LED Drive
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

Low-Power Features/CMOS Technology:

- Operating Current:
 - < 175 μA @ 2V, 4 MHz, typical
- Standby Current:
 - 100 nA @ 2V, typical
- Low-Power, High-Speed Flash Technology:
 - 100,000 cycle Flash endurance
 - > 40-year retention
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
- Wide Temperature Range:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +125°C

Peripheral Features (PIC12F510):

- 6 I/O Pins:
 - 5 I/O pins with individual direction control
 - 1 input only pin
- 1 Analog Comparator with Absolute Reference

Peripheral Features (PIC16F506):

- 12 I/O Pins:
 - 11 I/O pins with individual direction control
 - 1 input only pin
- 2 Analog Comparators with Absolute Reference and Programmable Reference

1.0 GENERAL DESCRIPTION

The PIC12F510/16F506 devices from Microchip Technology are low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word/single-cycle instructions. All instructions are single-cycle except for program branches, which take two cycles. The PIC12F510/16F506 devices deliver performance in an order of magnitude higher than their competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy-to-remember instruction set reduces development time significantly.

The PIC12F510/16F506 products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. There are four oscillator configurations to choose from (six on the PIC16F506), including INTOSC Internal Oscillator mode and the Power-Saving LP (Low-power) Oscillator mode. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC12F510/16F506 devices allow the customer to take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC12F510/16F506 products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC12F510/16F506 devices fit in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers perfect for applications with space limitations. Low-cost, low-power, high-performance, ease-of-use and I/O flexibility make the PIC12F510/16F506 devices very versatile, even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

TABLE 1-1: PIC12F510/16F506 DEVICES

		PIC16F506	PIC12F510
Clock	Maximum Frequency of Operation (MHz)	20	8
Memory	Flash Program Memory (words)	1024	1024
	Data Memory (bytes)	67	38
Peripherals	Timer Module(s)	TMR0	TMR0
	Wake-up from Sleep on Pin Change	Yes	Yes
Features	I/O Pins	11	5
	Input Only Pin	1	1
	Internal Pull-ups	Yes	Yes
	In-Circuit Serial Programming	Yes	Yes
	Number of Instructions	33	33
	Packages	14-pin PDIP, SOIC, TSSOP	8-pin PDIP, SOIC, MSOP, DFN

The PIC12F510/16F506 devices have Power-on Reset, selectable Watchdog Timer, selectable code-protect, high I/O current capability and precision internal oscillator.

The PIC12F510/16F506 devices use serial programming with data pin RB0/GP0 and clock pin RB1/GP1.

4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

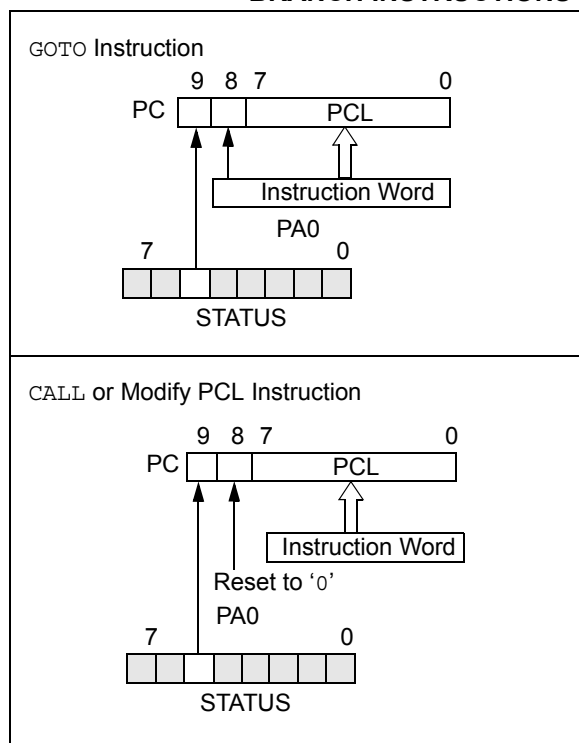
For a `GOTO` instruction, bits 8:0 of the PC are provided by the `GOTO` instruction word. The Program Counter (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-4).

For a `CALL` instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-4).

Instructions where the PCL is the destination or modify PCL instructions include `MOVWF PC`, `ADDWF PC` and `BSF PC, 5`.

Note: Because PC<8> is cleared in the `CALL` instruction or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-4: LOADING OF PC BRANCH INSTRUCTIONS



4.6.1 EFFECTS OF RESET

The PC is set upon a Reset, which means that the PC addresses the last location in the last page (i.e., the oscillator calibration instruction). After executing `MOVLW XX`, the PC will roll over to location 00h and begin executing user code.

The STATUS register page preselect bits are cleared upon a Reset, which means that page 0 is preselected.

Therefore, upon a Reset, a `GOTO` instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

The PIC12F510/16F506 devices have a two-deep, 12-bit wide hardware PUSH/POP stack.

A `CALL` instruction will PUSH the current value of Stack 1 into Stack 2 and then PUSH the current PC value, incremented by one, into Stack Level 1. If more than two sequential `CALL`s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will POP the contents of Stack Level 1 into the PC and then copy Stack Level 2 contents into Stack Level 1. If more than two sequential `RETLW`s are executed, the stack will be filled with the address previously stored in Stack Level 2.

Note 1: The W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

- 2: There are no Status bits to indicate stack overflows or stack underflow conditions.
- 3: There are no instruction mnemonics called `PUSH` or `POP`. These are actions that occur from the execution of the `CALL` and `RETLW` instructions.

4.8 Indirect Data Addressing: INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

4.8.1 INDIRECT ADDRESSING EXAMPLE

- Register file 07 contains the value 10h
- Register file 08 contains the value 0Ah
- Load the value 07 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 08)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```

        MOVLW    0x10    ;initialize pointer
        MOVWF    FSR     ;to RAM
NEXT    CLRF     INDF    ;clear INDF register
        INCF     FSR,F   ;inc pointer
        BTFSC    FSR,4   ;all done?
        GOTO     NEXT    ;NO, clear next
CONTINUE
        :           ;YES, continue
        :
    
```

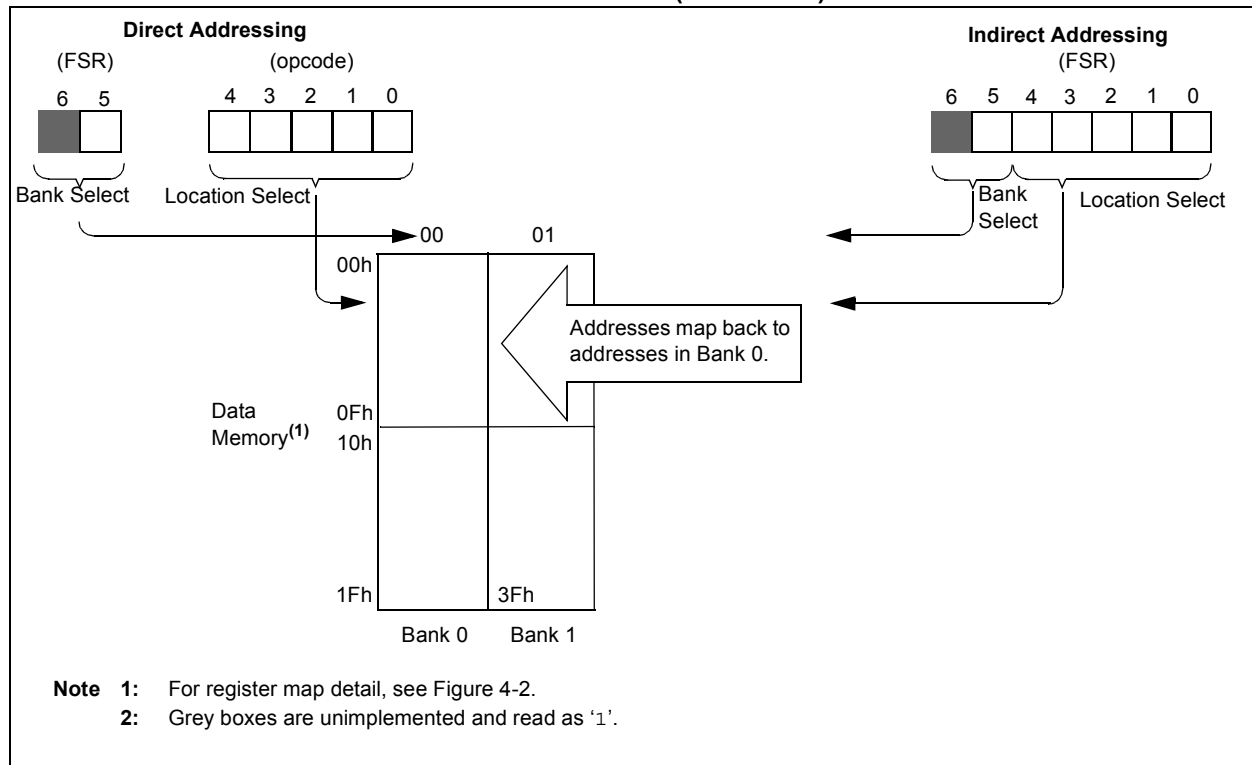
The FSR is a 5-bit wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16F506 – Uses FSR<6:5>. Selects from Bank 0 to Bank 3. FSR<7> is unimplemented, read as '1'.

PIC12F510 – Uses FSR<5>. Selects from Bank 0 to Bank 1. FSR<7:6> are unimplemented, read as '11'.

FIGURE 4-5: DIRECT/INDIRECT ADDRESSING (PIC12F510)



PIC12F510/16F506

FIGURE 5-2: BLOCK DIAGRAM OF GP0/RB0 AND GP1/RB1

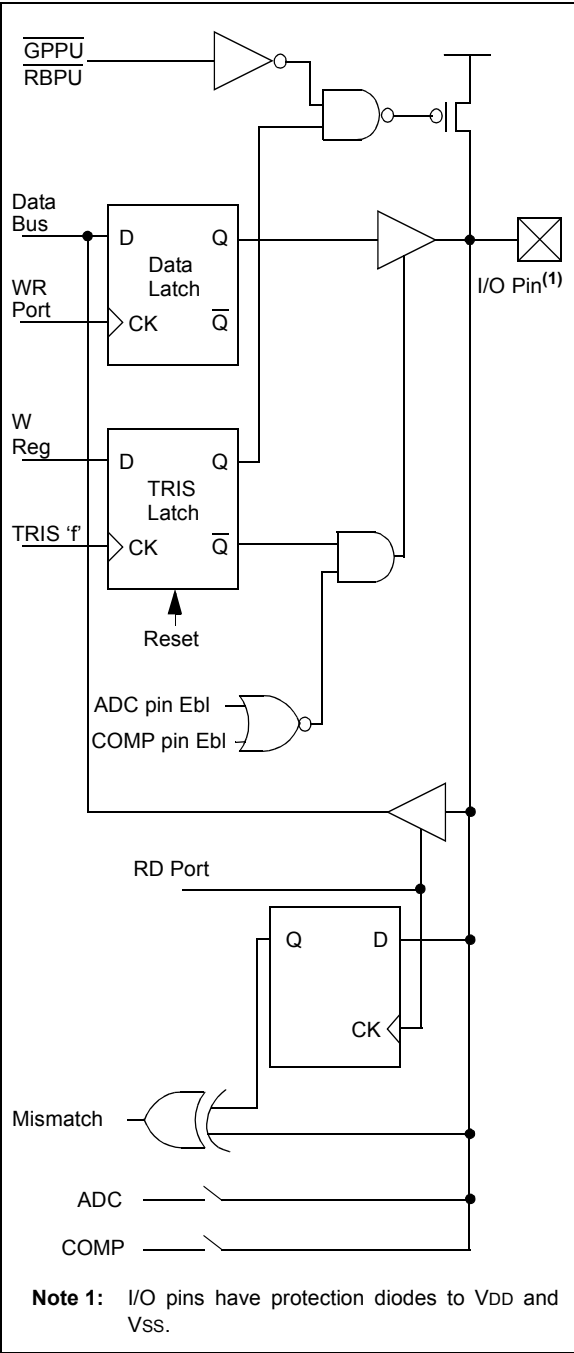
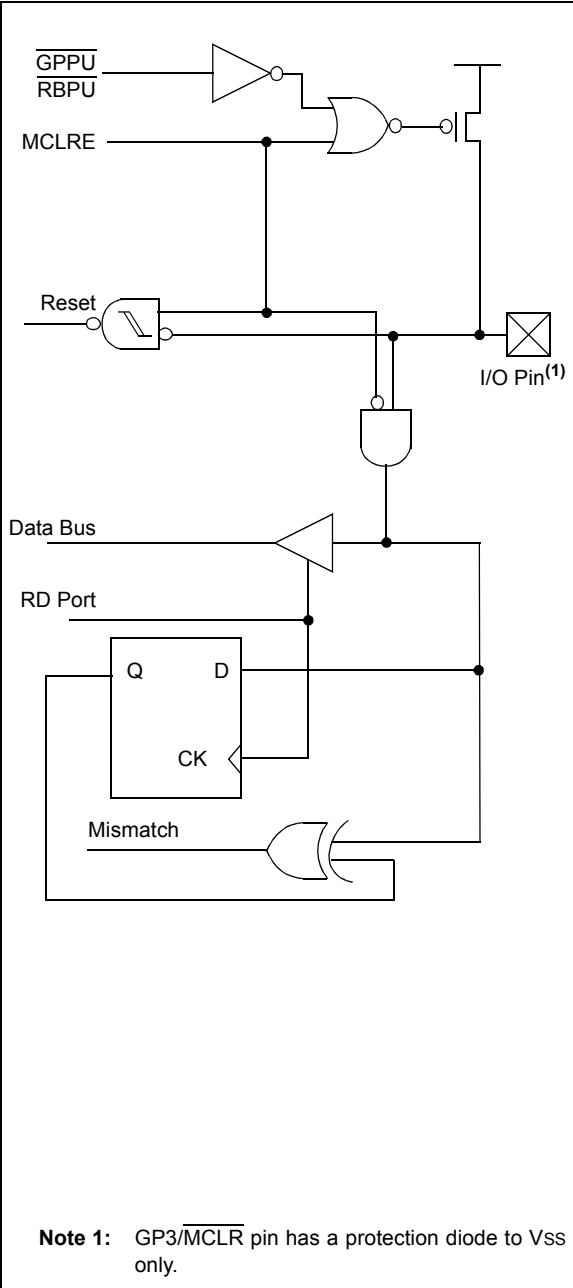


FIGURE 5-3: BLOCK DIAGRAM OF GP3/RB3 (With Weak Pull-up And Wake-up On Change)



5.5 I/O Programming Considerations

5.5.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. For example, the BCF and BSF instructions read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of PORTB/GPIO will cause all eight bits of PORTB/GPIO to be read into the CPU, bit 5 to be set and the PORTB/GPIO value to be written to the output latches. If another bit of PORTB/GPIO is used as a bidirectional I/O pin (say bit '0') and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit '0' is switched into Output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential Read-Modify-Write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired OR", "wired AND"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT (e.g., PIC16F506)

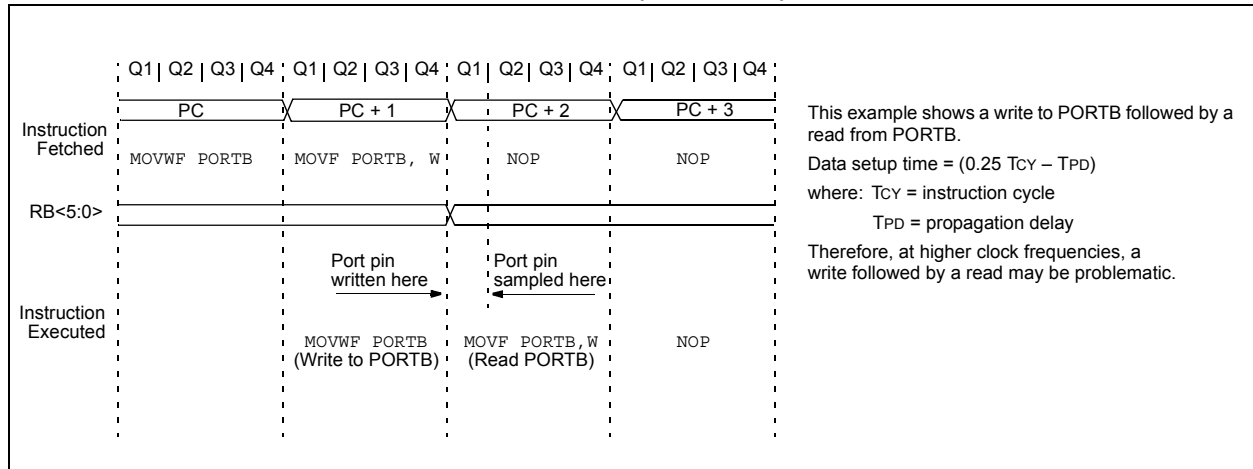
```
;Initial PORTB Settings
;PORTB<5:3> Inputs
;PORTB<2:0> Outputs
;
;          PORTB latch  PORTB pins
;          -----
BCF    PORTB, 5 ;--01 -ppp  --11 pppp
BCF    PORTB, 4 ;--10 -ppp  --11 pppp
MOVLW  007h;
TRIS   PORTB    ;--10 -ppp  --11 pppp
;
```

Note: The user may have expected the pin values to be '--00 pppp'. The 2nd BCF caused RB5 to be latched as the pin value (High).

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle. Whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-14). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes the file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

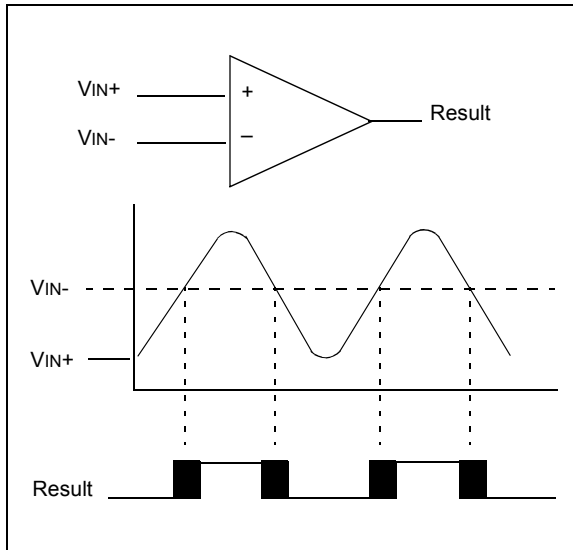
FIGURE 5-14: SUCCESSIVE I/O OPERATION (PIC16F506)



7.1 Comparator Operation

A single comparator is shown in Figure 7-3 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. The shaded area of the output of the comparator in Figure 7-3 represent the uncertainty due to input offsets and response time. See Table 13-1 for Common Mode Voltage.

FIGURE 7-3: SINGLE COMPARATOR



7.2 Comparator Reference

An internal reference signal may be used depending on the comparator operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 7-3). Please see **Section 8.0 “Comparator Voltage Reference Module (PIC16F506 only)”** for internal reference specifications.

7.3 Comparator Response Time

Response time is the minimum time after selecting a new reference voltage or input source before the comparator output is to have a valid level. If the comparator inputs are changed, a delay must be used to allow the comparator to settle to its new state. Please see Table 13-1 for comparator response time specifications.

7.4 Comparator Output

The comparator output is read through the CM1CON0 or CM2CON0 register. This bit is read-only. The comparator output may also be used externally, see Figure 7-3.

Note: Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

7.5 Comparator Wake-up Flag

The Comparator Wake-up Flag is set whenever all of the following conditions are met:

- $\overline{C1WU} = 0$ (CM1CON0<0>) or $\overline{C2WU} = 0$ (CM2CON0<0>)
- CM1CON0 or CM2CON0 has been read to latch the last known state of the C1OUT and C2OUT bit (MOVWF CM1CON0, W)
- Device is in Sleep
- The output of a comparator has changed state

The wake-up flag may be cleared in software or by another device Reset.

7.6 Comparator Operation During Sleep

When the comparator is enabled it is active. To minimize power consumption while in Sleep mode, turn off the comparator before entering Sleep.

7.7 Effects of Reset

A Power-on Reset (POR) forces the CM2CON0 register to its Reset state. This forces the Comparator input pins to analog Reset mode. Device current is minimized when analog inputs are present at Reset time.

7.8 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 7-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

9.1.6 ANALOG CONVERSION RESULT REGISTER

The ADRES register contains the results of the last conversion. These results are present during the sampling period of the next analog conversion process. After the sampling period is over, ADRES is cleared (= 0). A 'leading one' is then right shifted into the ADRES to serve as an internal conversion complete bit. As each bit weight, starting with the MSB, is converted, the leading one is shifted right and the converted bit is stuffed into ADRES. After a total of 9 right

shifts of the 'leading one' have taken place, the conversion is complete; the 'leading one' has been shifted out and the GO/DONE bit is cleared.

If the GO/DONE bit is cleared in software during a conversion, the conversion stops. The data in ADRES is the partial conversion result. This data is valid for the bit weights that have been converted. The position of the 'leading one' determines the number of bits that have been converted. The bits that were not converted before the GO/DONE was cleared are unrecoverable.

REGISTER 9-1: ADCON0: A/D CONTROL REGISTER (PIC12F510)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
ANS1	ANS0	ADCS1	ADCS0	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **ANS<1:0>**: ADC Analog Input Pin Select bits^{(1), (2)}

- 00 = No pins configured for analog input
- 01 = AN2 configured as an analog input
- 10 = AN2 and AN0 configured as analog inputs
- 11 = AN2, AN1 and AN0 configured as analog inputs

bit 5-4 **ADCS<1:0>**: ADC Conversion Clock Select bits

- 00 = Fosc/16
- 01 = Fosc/8
- 10 = Fosc/4
- 11 = INTOSC/4

bit 3-2 **CHS<1:0>**: ADC Channel Select bits

- 00 = Channel AN0
- 01 = Channel AN1
- 10 = Channel AN2
- 11 = 0.6V absolute voltage reference

bit 1 **GO/DONE**: ADC Conversion Status bit⁽⁴⁾

- 1 = ADC conversion in progress. Setting this bit starts an ADC conversion cycle. This bit is automatically cleared by hardware when the ADC is done converting.
- 0 = ADC conversion completed/not in progress. Manually clearing this bit while a conversion is in process terminates the current conversion.

bit 0 **ADON**: ADC Enable bit

- 1 = ADC module is operating
- 0 = ADC module is shut-off and consumes no power

Note 1: When the ANS bits are set, the channels selected will automatically be forced into Analog mode, regardless of the pin function previously defined. The only exception to this is the comparator, where the analog input to the comparator and the ADC will be active at the same time. It is the users responsibility to ensure that the ADC loading on the comparator input does not affect their application.

2: The ANS<1:0> bits are active regardless of the condition of ADON.

3: CHS<1:0> bits default to 11 after any Reset.

4: If the ADON bit is clear, the GO/DONE bit cannot be set.

PIC12F510/16F506

REGISTER 9-2: ADRES REGISTER

R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

EXAMPLE 9-1: PERFORMING AN ANALOG-TO-DIGITAL CONVERSION

;Sample code operates out of BANK0

```

        MOVLW 0xF1      ;configure A/D
        MOVWF ADCON0
        BSF ADCON0, 1   ;start conversion
loop0   BTFSC ADCON0, 1 ;wait for 'DONE'
        GOTO loop0
        MOVF ADRES, W   ;read result
        MOVWF result0   ;save result

        BSF ADCON0, 2   ;setup for read of
                        ;channel 1
        BSF ADCON0, 1   ;start conversion
loop1   BTFSC ADCON0, 1 ;wait for 'DONE'
        GOTO loop1
        MOVF ADRES, W   ;read result
        MOVWF result1   ;save result

        BSF ADCON0, 3   ;setup for read of
        BCF ADCON0, 2   ;channel 2
        BSF ADCON0, 1   ;start conversion
loop2   BTFSC ADCON0, 1 ;wait for 'DONE'
        GOTO loop2
        MOVF ADRES, W   ;read result
        MOVWF result2   ;save result

```

EXAMPLE 9-2: CHANNEL SELECTION CHANGE DURING CONVERSION

```

        MOVLW 0xF1      ;configure A/D
        MOVWF ADCON0
        BSF ADCON0, 1   ;start conversion
        BSF ADCON0, 2   ;setup for read of
                        ;channel 1
loop0   BTFSC ADCON0, 1 ;wait for 'DONE'
        GOTO loop0
        MOVF ADRES, W   ;read result
        MOVWF result0   ;save result

        BSF ADCON0, 1   ;start conversion
        BSF ADCON0, 3   ;setup for read of
        BCF ADCON0, 2   ;channel 2
loop1   BTFSC ADCON0, 1 ;wait for 'DONE'
        GOTO loop1
        MOVF ADRES, W   ;read result
        MOVWF result1   ;save result

        BSF ADCON0, 1   ;start conversion
loop2   BTFSC ADCON0, 1 ;wait for 'DONE'
        GOTO loop2
        MOVF ADRES, W   ;read result
        MOVWF result2   ;save result
        CLRF ADCON0     ;optional: returns
                        ;pins to Digital mode and turns off
                        ;the ADC module

```

PIC12F510/16F506

10.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (TO, PD, GPWUF/RBWUF)

The \overline{TO} , \overline{PD} and (GPWUF/RBWUF) bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a MCLR or Watchdog Timer (WDT) Reset.

TABLE 10-8: $\overline{TO}/\overline{PD}/(GPWUF/RBWUF)$ STATUS AFTER RESET

CWUF	GPWUF/ RBWUF	\overline{TO}	\overline{PD}	Reset Caused By
0	0	0	0	WDT wake-up from Sleep
0	0	0	u	WDT time-out (not from Sleep)
0	0	1	0	MCLR wake-up from Sleep
0	0	1	1	Power-up
0	0	u	u	MCLR not during Sleep
0	1	1	0	Wake-up from Sleep on pin change
1	0	1	0	Wake-up from Sleep on comparator change

Legend: u = unchanged

10.8 Reset on Brown-out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12F510/16F506 devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 10-12 and Figure 10-13.

FIGURE 10-12: BROWN-OUT PROTECTION CIRCUIT 1

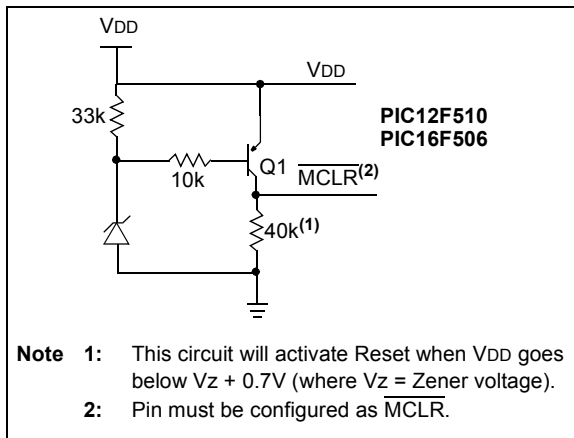


FIGURE 10-13: BROWN-OUT PROTECTION CIRCUIT 2

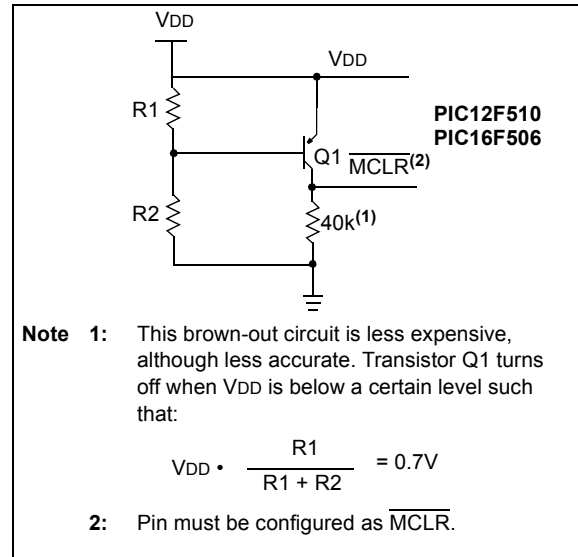
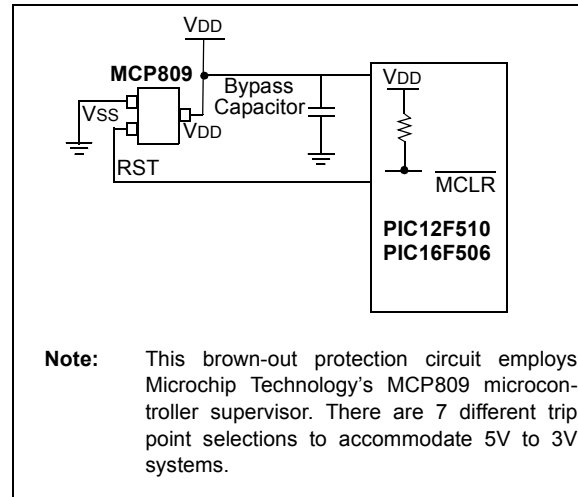


FIGURE 10-14: BROWN-OUT PROTECTION CIRCUIT 3



PIC12F510/16F506

10.12 In-Circuit Serial Programming™ (ICSP™)

The PIC12F510/16F506 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The devices are placed into a Program/Verify mode by holding the GP1/RB1 and GP0/RB0 pins low while raising the MCLR (VPP) pin from V_{IL} to V_{IHH} (see programming specification). GP1/RB1 becomes the programming clock and GP0/RB0 becomes the programming data. Both GP1/RB1 and GP0/RB0 are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is supplied to the device. Depending on the command and if the command was a Load or a Read, 14 bits of program data are then supplied to or from the device. For complete details of serial programming, please refer to the PIC12F510/16F506 Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 10-15.

FIGURE 10-15: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION

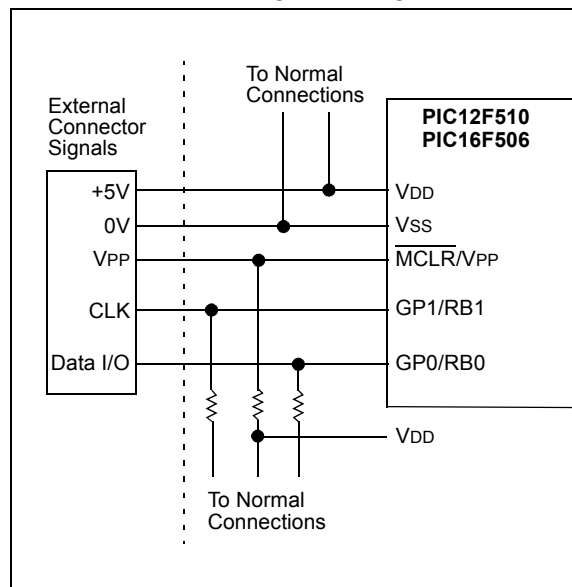


TABLE 13-6: TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)				
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units
17	TosH2ioV	OSC1 \uparrow (Q1 cycle) to Port out valid ^{(2), (3)}	—	—	100*	ns
18	TosH2ioI	OSC1 \uparrow (Q2 cycle) to Port input invalid (I/O in hold time) ⁽²⁾	50	—	—	ns
19	TioV2osH	Port input valid to OSC1 \uparrow (I/O in setup time)	20	—	—	ns
20	TioR	Port output rise time ^{(2), (3)}	—	10	25**	ns
21	TioF	Port output fall time ^{(2), (3)}	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in EXTRC mode.

3: See Figure 13-5 for loading conditions.

FIGURE 13-8: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER TIMING

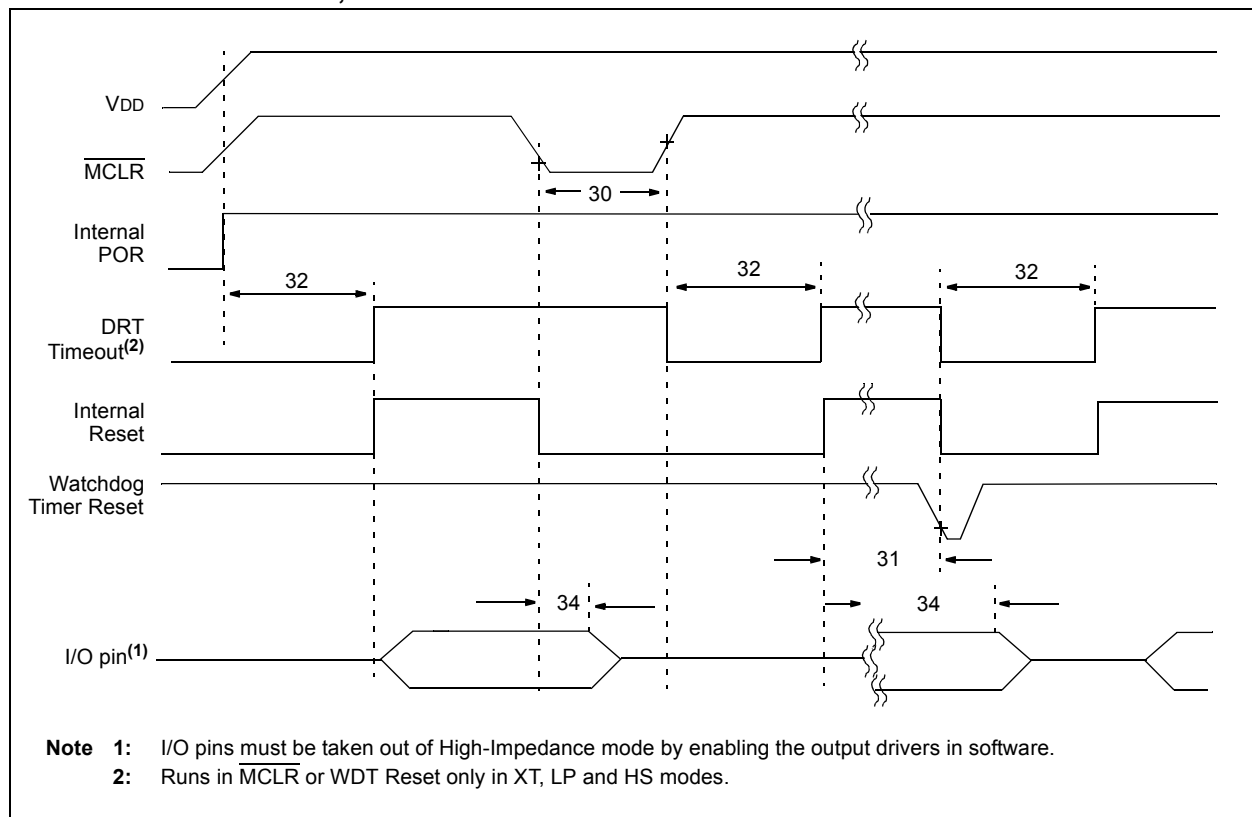


TABLE 13-9: PULL-UP RESISTOR RANGES

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
RB0 (GP0)/RB1 (GP1)					
2.0	-40	73K	105K	186K	Ω
	25	73K	113K	187K	Ω
	85	82K	123K	190K	Ω
	125	86K	132k	190K	Ω
5.5	-40	15K	21K	33K	Ω
	25	15K	22K	34K	Ω
	85	19K	26k	35K	Ω
	125	23K	29K	35K	Ω
RB3 (GP3)					
2.0	-40	63K	81K	96K	Ω
	25	77K	93K	116K	Ω
	85	82K	96k	116K	Ω
	125	86K	100K	119K	Ω
5.5	-40	16K	20k	22K	Ω
	25	16K	21K	23K	Ω
	85	24K	25k	28K	Ω
	125	26K	27K	29K	Ω

PIC12F510/16F506

FIGURE 14-2: TYPICAL I_{PD} vs. V_{DD} (SLEEP MODE, ALL PERIPHERALS DISABLED)

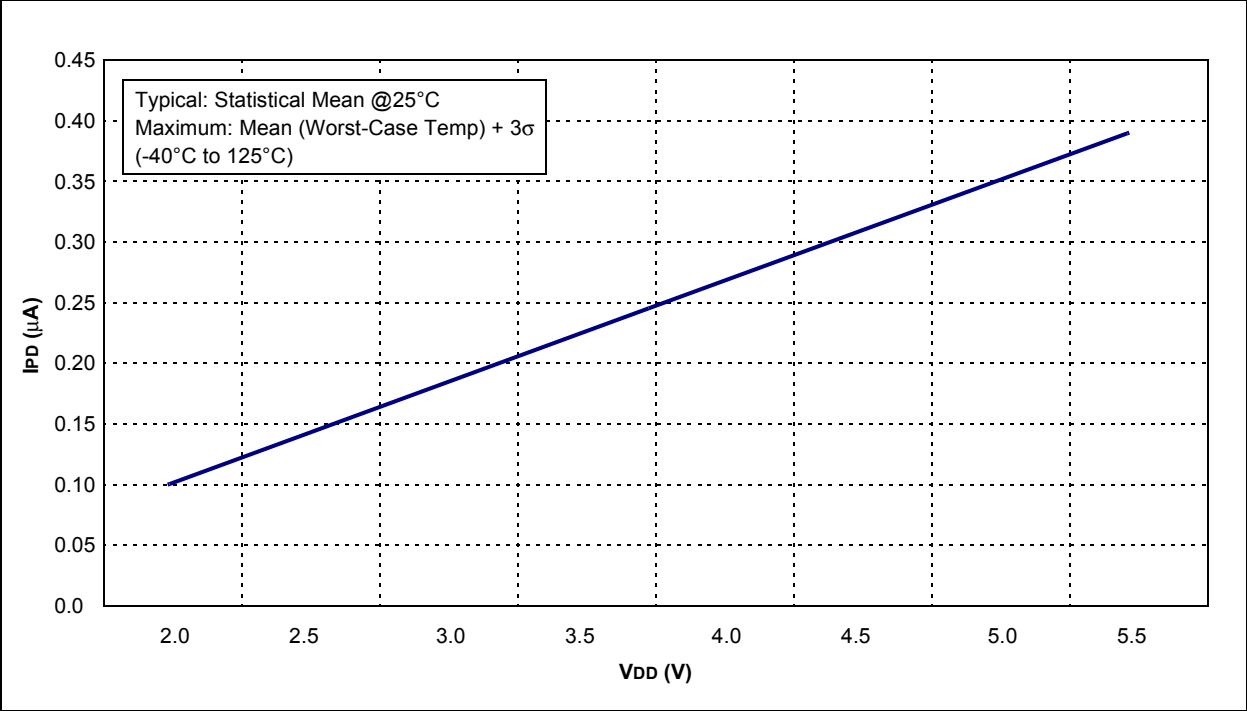


FIGURE 14-3: MAXIMUM I_{PD} vs. V_{DD} (SLEEP MODE, ALL PERIPHERALS DISABLED)

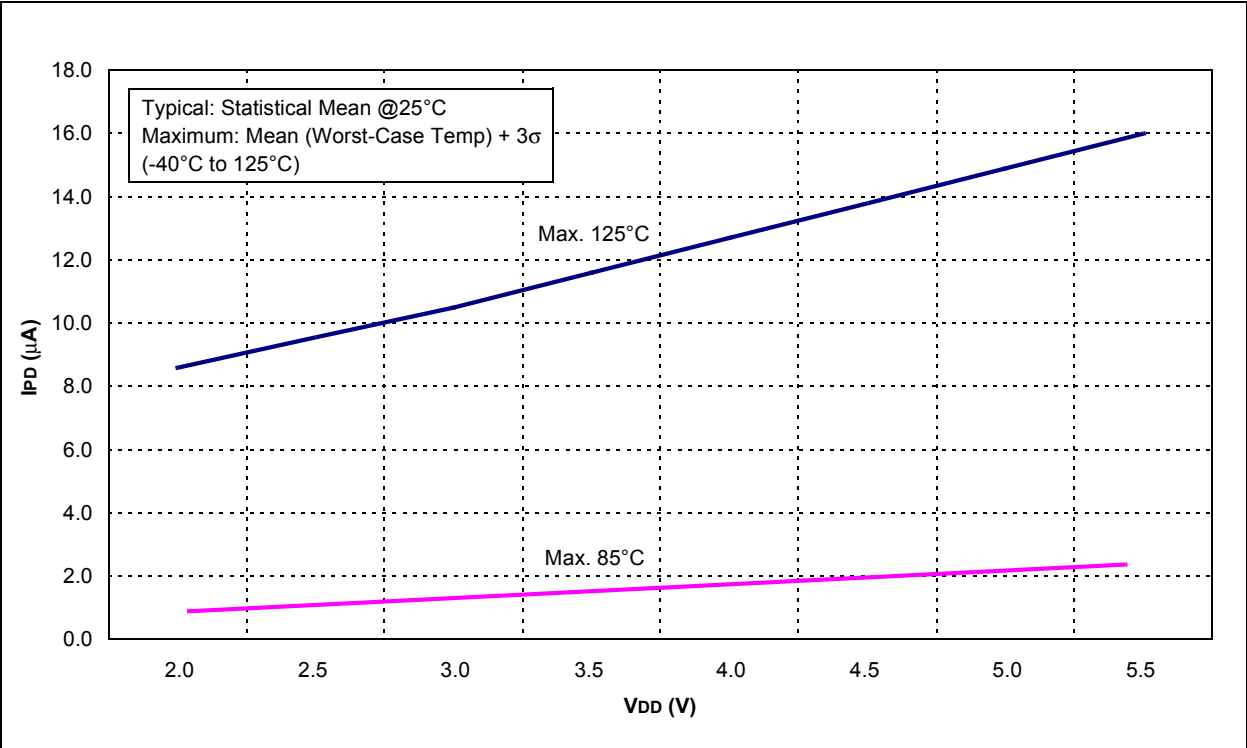


FIGURE 14-4: COMPARATOR I_{PD} vs. V_{DD} (COMPARATOR ENABLED)

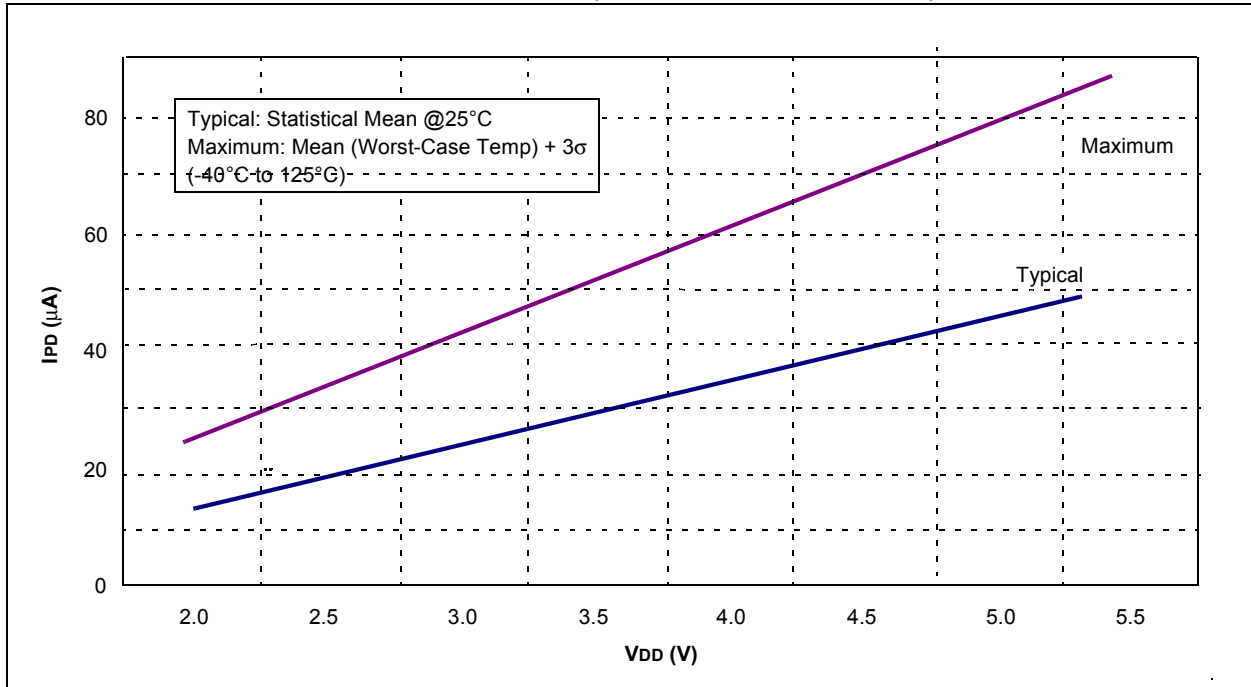
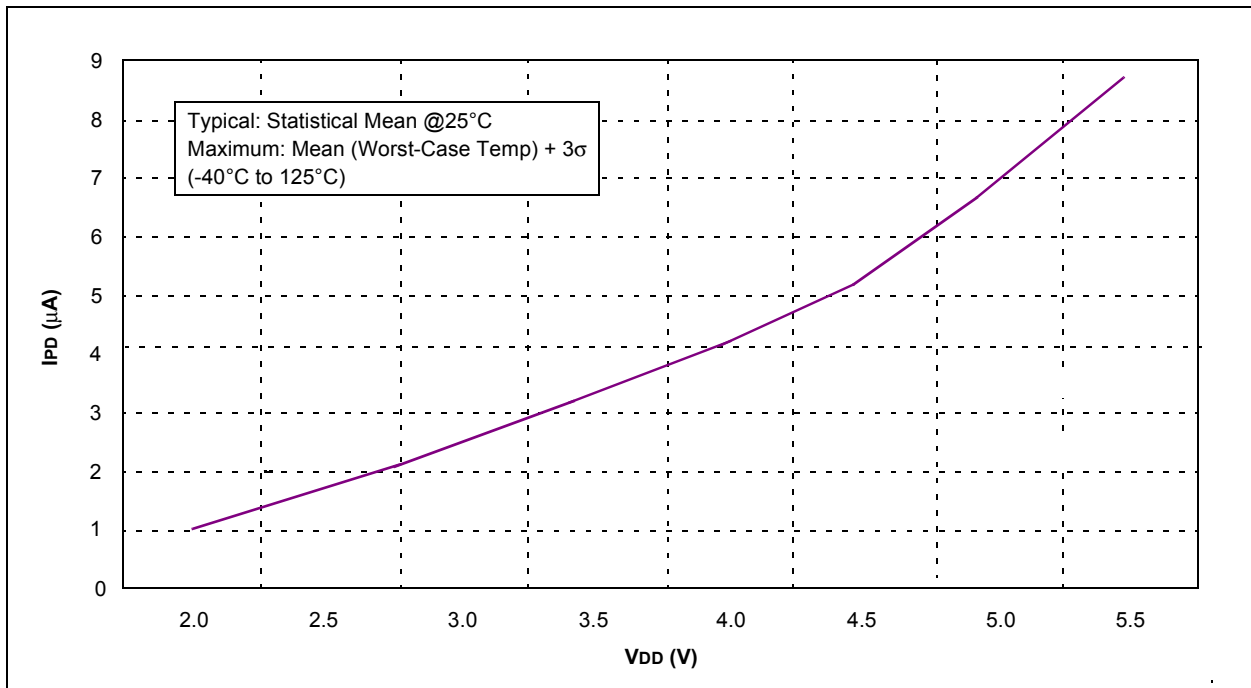
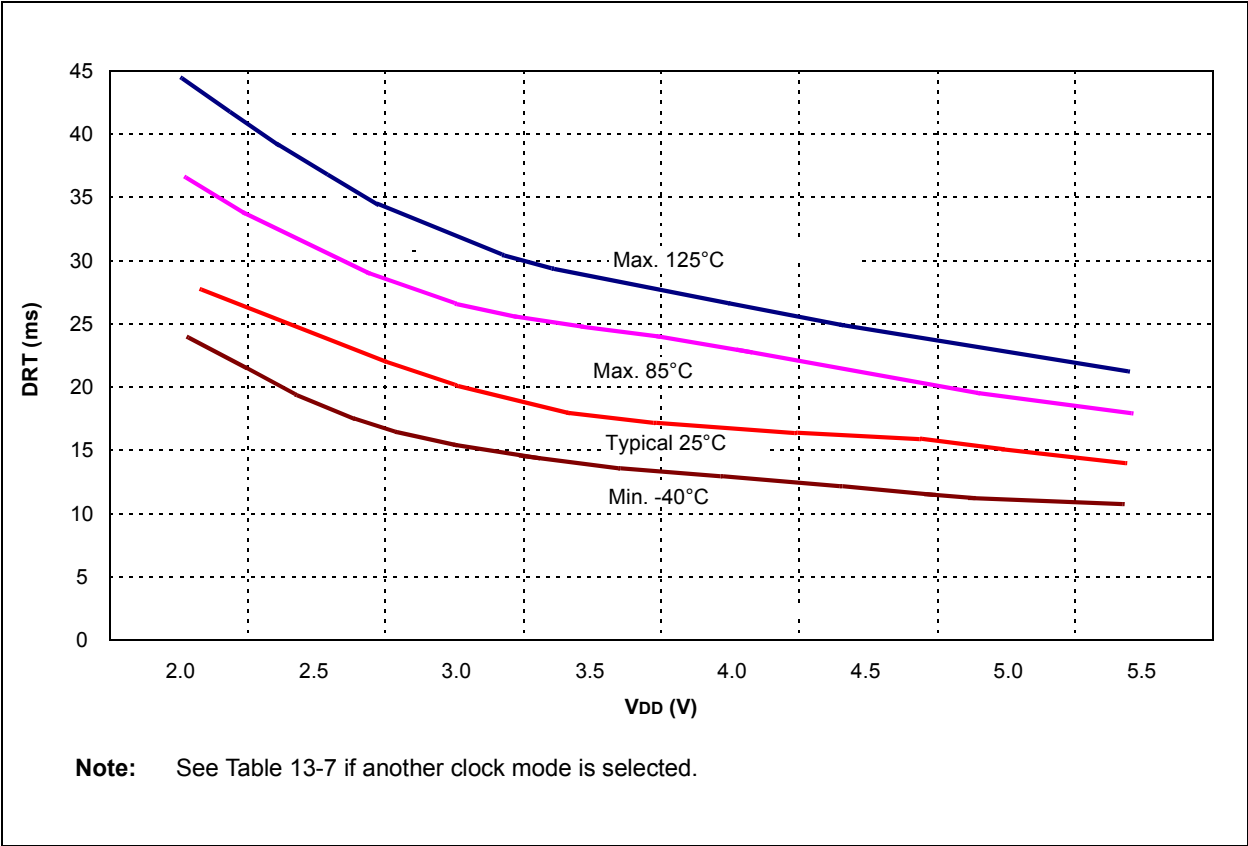


FIGURE 14-5: TYPICAL WDT I_{PD} vs. V_{DD}



PIC12F510/16F506

FIGURE 14-14: DEVICE RESET TIMER (HS, XT AND LP) vs. VDD



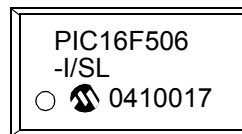
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15.2 Package Marking Information (Cont'd)

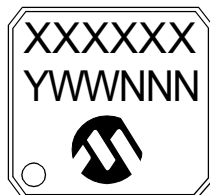
14-Lead SOIC (3.90 mm)



Example



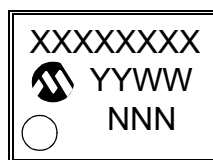
8-Lead MSOP



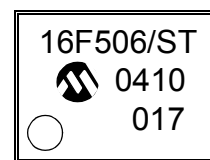
Example



14-Lead TSSOP (4.4 mm)

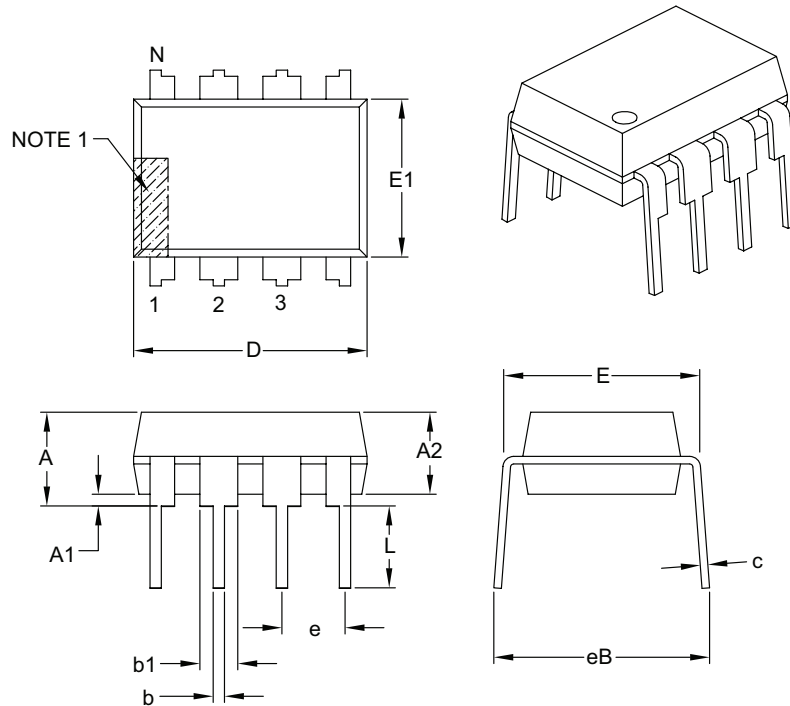


Example



8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

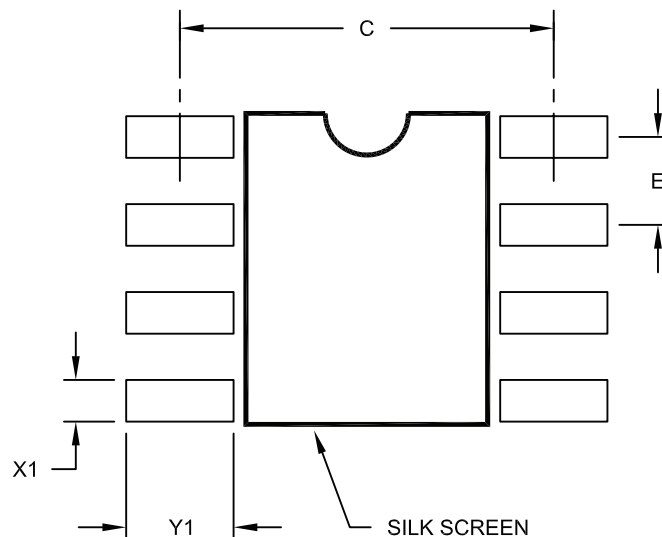
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

PIC12F510/16F506

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

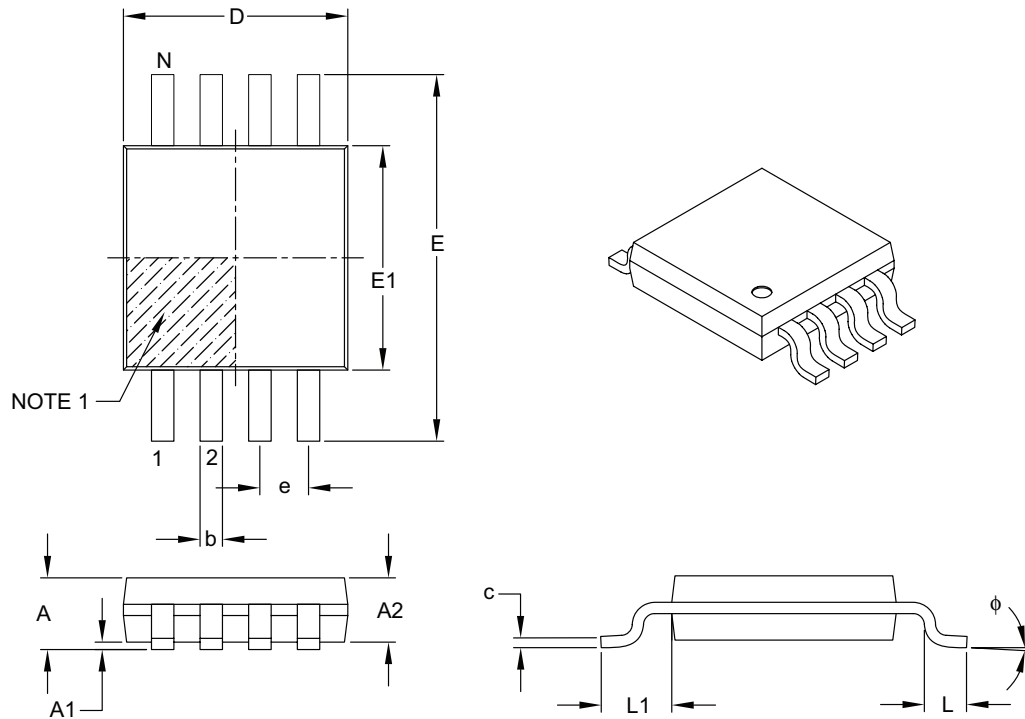
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	—	—	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	—	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	φ	0°	—	8°
Lead Thickness	c	0.08	—	0.23
Lead Width	b	0.22	—	0.40

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B