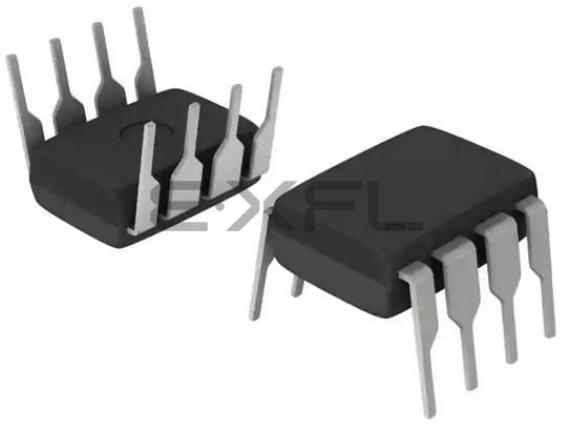

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Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	38 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
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4.2 Data Memory Organization

Data memory is composed of registers or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers (SFRs) and General Purpose Registers (GPRs).

The Special Function Registers include the TMR0 register, the Program Counter (PCL), the STATUS register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Function Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

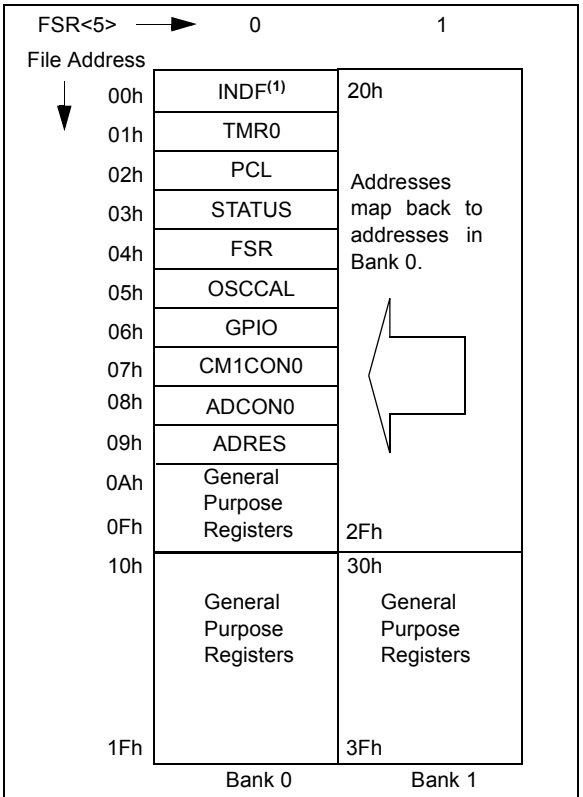
For the PIC12F510, the register file is composed of 10 Special Function Registers, 6 General Purpose Registers and 32 General Purpose Registers accessed by banking (see Figure 4-2).

For the PIC16F506, the register file is composed of 13 Special Function Registers, 3 General Purpose Registers and 64 General Purpose Registers, accessed by banking (see Figure 4-3).

4.2.1 GENERAL PURPOSE REGISTER FILE

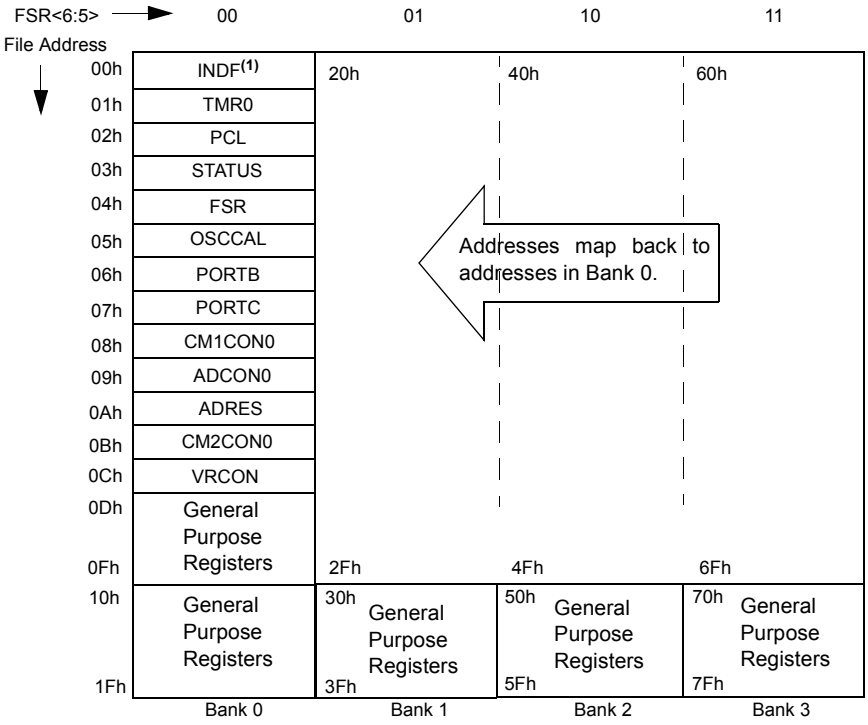
The General Purpose Register file is accessed either directly or indirectly through the File Select Register (FSR). See **Section 4.8 "Indirect Data Addressing: INDF and FSR Registers"**.

FIGURE 4-2: PIC12F510 REGISTER FILE MAP



Note 1: Not a physical register.

FIGURE 4-3: PIC16F506 REGISTER FILE MAP



Note 1: Not a physical register.

TABLE 4-2: SPECIAL FUNCTION REGISTER SUMMARY – PIC16F506

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset
N/A	TRIS	I/O Control Registers (TRISB, TRISC)								--11 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT Prescaler								1111 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
01h	TMR0	Timer0 Module Register								xxxx xxxx
02h(1)	PCL	Low Order 8 bits of PC								1111 1111
03h	STATUS	RBWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
04h	FSR	Indirect Data Memory Address Pointer								100x xxxx
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	1111 111-
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx
08h	CM1CON0	C1OUT	$\overline{C1OUTEN}$	C1POL	$\overline{C1T0CS}$	C1ON	C1NREF	C1PREF	$\overline{C1WU}$	1111 1111
09h	ADCON0	ANS1	ANS0	ADCS1	ADCS0	CHS1	CHS0	GO/$\overline{DONE}$	ADON	1111 1100
0Ah	ADRES	ADC Conversion Result								xxxx xxxx
0Bh	CM2CON0	C2OUT	$\overline{C2OUTEN}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{C2WU}$	1111 1111
0Ch	VRCON	VREN	VROE	VRR	—(2)	VR3	VR2	VR1	VR0	0011 1111

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused.

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.6 "Program Counter"** for an explanation of how to access these bits.

2: Unimplemented bit VRCON<4> read as '1'.

4.3 STATUS Register

This register contains the arithmetic status of the ALU, the Reset status and the page preselect bit.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS, will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u u1uu (where u = unchanged).

Therefore, it is recommended that only BCF, BSF and MOVWF instructions be used to alter the STATUS register. These instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions which do affect Status bits, see **Section 11.0 "Instruction Set Summary"**.

REGISTER 4-1: STATUS: STATUS REGISTER (PIC12F510)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
GPWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **GPWUF**: GPIO Reset bit
1 = Reset due to wake-up from Sleep on pin change
0 = After power-up or other Reset

bit 6 **CWUF**: Comparator Reset bit
1 = Reset due to wake-up from Sleep on comparator change
0 = After power-up or other Reset

bit 5 **PA0**: Program Page Preselect bit
1 = Page 1 (200h-3FFh)
0 = Page 0 (000h-1FFh)
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.

bit 4 **$\overline{TO}$**: Time-Out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$**: Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit Carry/$\overline{Borrow}$ bit (for ADDWF and SUBWF instructions)
ADDWF:
1 = A carry from the 4th low-order bit of the result occurred
0 = A carry from the 4th low-order bit of the result did not occur
SUBWF:
1 = A borrow from the 4th low-order bit of the result did not occur
0 = A borrow from the 4th low-order bit of the result occurred

bit 0 **C**: Carry/$\overline{Borrow}$ bit (for ADDWF, SUBWF and RRF, RLF instructions)

ADDWF:	SUBWF:	RRF or RLF:
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSb or MSb, respectively
0 = A carry did not occur	0 = A borrow occurred	

4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register, that contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A Reset sets the OPTION<7:0> bits.

Note 1:	If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin (i.e., note that TRIS overrides Option control of $\overline{\text{GPPU}}$/RBPU and $\overline{\text{GPWU}}$/$\overline{\text{RBWU}}$).
2:	If the T0CS bit is set to '1', it will override the TRIS function on the T0CKI pin.

REGISTER 4-3: OPTION_REG: OPTION REGISTER (PIC12F510)

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{GPWU}}$:** Enable Wake-up On Pin Change bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6 **$\overline{\text{GPPU}}$:** Enable Weak Pull-Ups bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

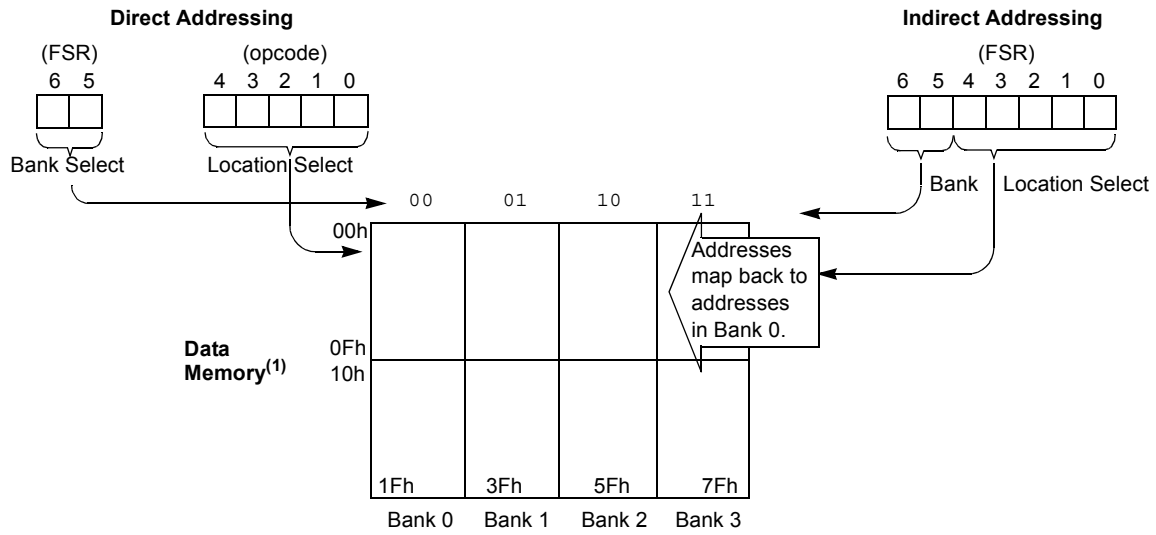
bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

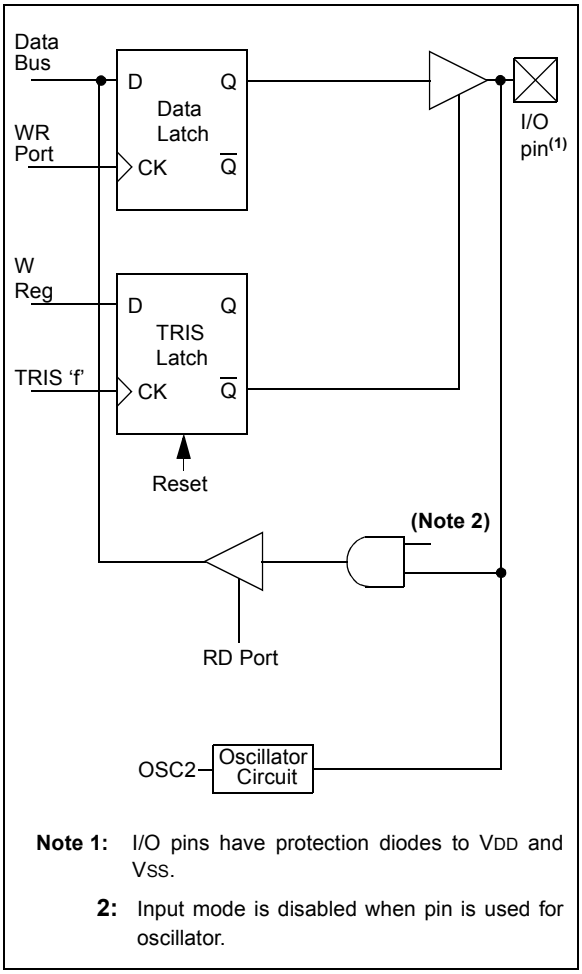
Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

FIGURE 4-6: DIRECT/INDIRECT ADDRESSING (PIC16F506)



Note 1: For register map detail, see Figure 4-3.

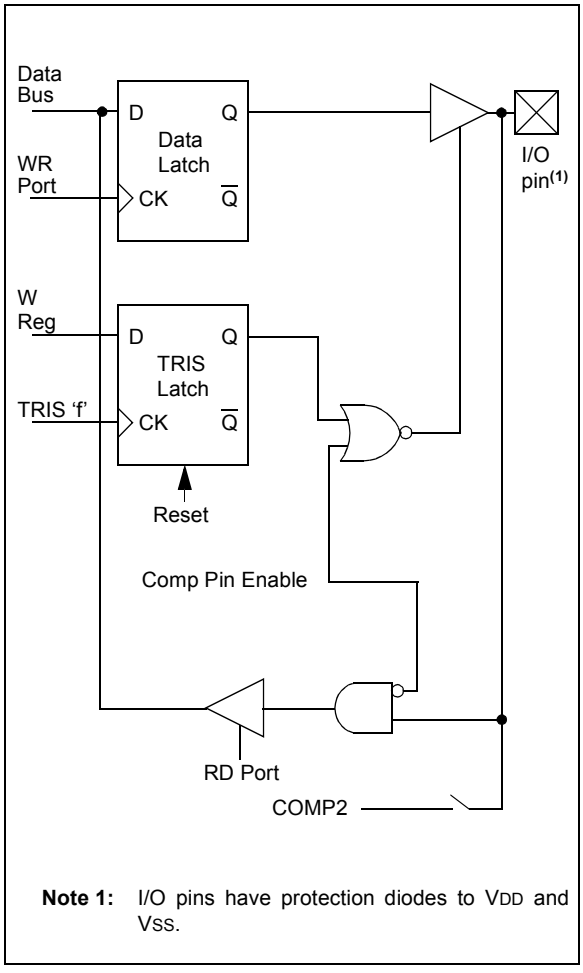
FIGURE 5-8: BLOCK DIAGRAM OF RB5/GP5



Note 1: I/O pins have protection diodes to VDD and VSS.

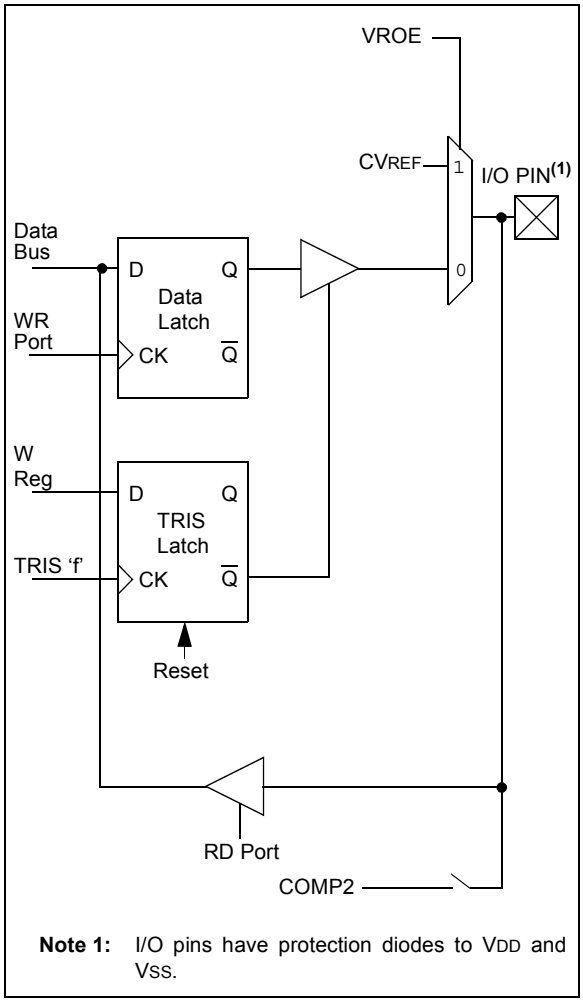
2: Input mode is disabled when pin is used for oscillator.

FIGURE 5-9: BLOCK DIAGRAM OF RC0/RC1



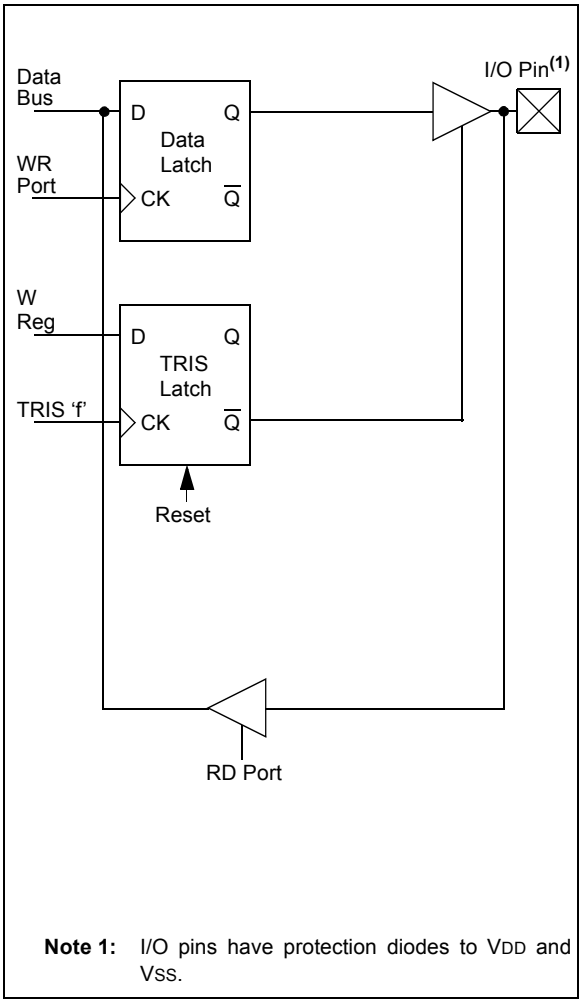
Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 5-10: BLOCK DIAGRAM OF RC2



Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 5-11: BLOCK DIAGRAM OF RC3



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRISGPIO(1)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISB(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISC(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	OPTION(1)	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION(2)	$\overline{RBWU}$	$\overline{RBPU}$	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS(1)	GPWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	qq0q quuu(3)
03h	STATUS(2)	RBWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	qq0q quuu(3)
06h	GPIO(1)	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
06h	PORTB(2)	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC(2)	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: – = unimplemented read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: PIC12F510 only.

2: PIC16F506 only.

3: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

TABLE 5-2: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)

Priority	RB0	RB1	RB2	RB3	RB4	RB5
1	AN0/C1IN+	AN1/C1IN-	AN2	Input/$\overline{MCLR}$	OSC2/CLKOUT	OSC1/CLKIN
2	TRISB	TRISB	C1OUT	—	TRISB	TRISB
3	—	—	TRISB	—	—	—

TABLE 5-3: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)

Priority	RC0	RC1	RC2	RC3	RC4	RC5
1	C2IN+	C2IN-	CV_{REF}	TRISC	C2OUT	T0CKI
2	TRISC	TRISC	TRISC	—	TRISC	TRISC

TABLE 5-4: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC12F510)

Priority	GP0	GP1	GP2	GP3	GP4	GP5
1	AN0/C1IN+	AN1/C1IN-	AN2	Input/$\overline{MCLR}$	OSC2	OSC1/CLKIN
2	TRISIO	TRISIO	C1OUT	—	TRISIO	TRISIO
3	—	—	T0CKI	—	—	—
4	—	—	TRISIO	—	—	—

TABLE 5-5: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC12F510)

	GP0	GP0	GP1	GP1	GP2	GP2	GP3	GP4	GP5
CM1CON0									
C1ON	0	1	0	1	0	1	—	—	—
C1PREF	—	0	—	1	—	—	—	—	—
C1NREF	—	—	—	0	—	—	—	—	—
$\overline{\text{C1T0CS}}$	—	—	—	—	—	1	—	—	—
$\overline{\text{C1OUTEN}}$	—	—	—	—	—	1	—	—	—
CM2CON0									
C2ON	—	—	—	—	—	—	—	—	—
C2PREF1	—	—	—	—	—	—	—	—	—
C2PREF2	—	—	—	—	—	—	—	—	—
C2NREF	—	—	—	—	—	—	—	—	—
$\overline{\text{C2OUTEN}}$	—	—	—	—	—	—	—	—	—
VRCON0									
VROE	—	—	—	—	—	—	—	—	—
VREN	—	—	—	—	—	—	—	—	—
OPTION									
T0CS	—	—	—	—	—	0	—	—	—
ADCON0									
ANS<1:0>	00, 01	00, 01	00, 01, 10	00, 01, 10	00	00	—	—	—
CONFIG									
MCLRE	—	—	—	—	—	—	—	—	—
INTOSC	—	—	—	—	—	—	—	—	—
LP	—	—	—	—	—	—	—	Disabled	Disabled
EXTRC	—	—	—	—	—	—	—	—	Disabled
XT	—	—	—	—	—	—	—	Disabled	Disabled

Note 1: Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

2: Shaded cells indicate the bit status does not affect the pins digital functionality.

TABLE 5-6: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC16F506 PORTB)(1), (2)

	RB0	RB0	RB0	RB1	RB1	RB2	RB2	RB3	RB4	RB5
CM1CON0										
C1ON	—	0	1	0	1	0	1	—	—	—
C1PREF	—	—	0	—	—	—	—	—	—	—
C1NREF	—	—	—	—	0	—	—	—	—	—
$\overline{\text{C1T0CS}}$	—	—	—	—	—	—	—	—	—	—
$\overline{\text{C1OUTEN}}$	—	—	—	—	—	—	1	—	—	—
CM2CON0										
C2ON	1	—	—	—	—	—	—	—	—	—
C2PREF1	0	—	—	—	—	—	—	—	—	—
C2PREF2	1	—	—	—	—	—	—	—	—	—
C2NREF	—	—	—	—	—	—	—	—	—	—
$\overline{\text{C2OUTEN}}$	—	—	—	—	—	—	—	—	—	—
OPTION										
T0CS	—	—	—	—	—	—	—	—	—	—
ADCON0										
ANS<1:0>	00, 01	00, 01	00, 01	00, 01, 10	00, 01, 10	00	00	—	—	—
CONFIG										
MCLRE	—	—	—	—	—	—	—	0	—	—
INTOSC	—	—	—	—	—	—	—	—	—	—
LP	—	—	—	—	—	—	—	—	Disabled	Disabled
EXTRC	—	—	—	—	—	—	—	—	—	Disabled
XT	—	—	—	—	—	—	—	—	Disabled	Disabled
EC	—	—	—	—	—	—	—	—	—	Disabled
HS	—	—	—	—	—	—	—	—	Disabled	Disabled
INTOSC CLKOUT	—	—	—	—	—	—	—	—	Disabled	Disabled
EXTRC CLOCKOUT	—	—	—	—	—	—	—	—	Disabled	Disabled

Note 1: Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

2: Shaded cells indicate the bit status does not affect the pins digital functionality.

TABLE 5-7: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC16F506 PORTC)(1), (2)

	RC0	RC0	RC1	RC1	RC2	RC3	RC4	RC4	RC5	RC5
CM2CON0										
C2ON	0	1	0	1	—	—	0	1	—	—
C2PREF1	—	0	—	—	—	—	—	—	—	—
C2PREF2	—	0	—	—	—	—	—	—	—	—
C2NREF	—	—	—	0	—	—	—	—	—	—
$\overline{\text{C2OUTEN}}$	—	—	—	—	—	—	—	1	—	—
VRCON0										
VROE	—	—	—	—	0	—	—	—	—	—
OPTION										
T0CS	—	—	—	—	—	—	—	—	0	—

Note 1: Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

2: Shaded cells indicate the bit status does not affect the pins digital functionality.

FIGURE 8-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

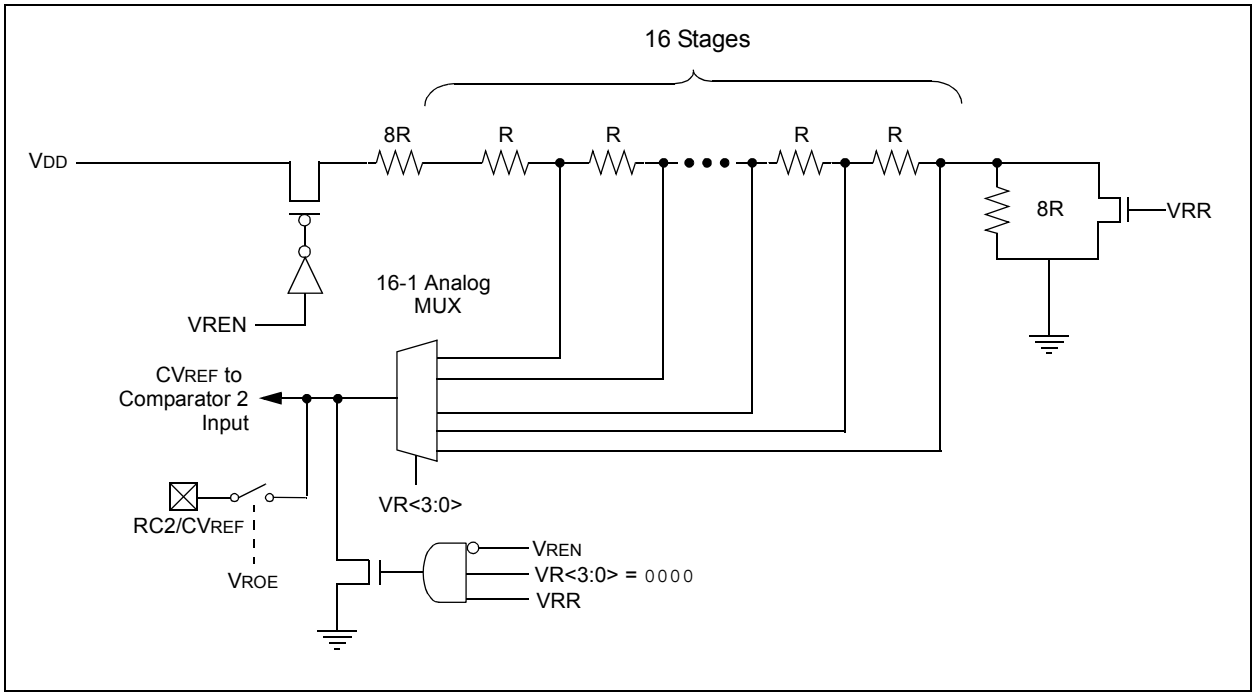


TABLE 8-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Add	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
0Ch	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	001- 1111	001- 1111
08h	CM1CON0(1)	C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$	1111 1111	uuuu uuuu
0Bh	CM2CON0(1)	C2OUT	$\overline{\text{C2OUTEN}}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{\text{C2WU}}$	1111 1111	uuuu uuuu

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'.
Note 1: PIC16F506 only.

REGISTER 10-1: CONFIG: CONFIGURATION WORD REGISTER (PIC12F510)(1)

—	—	—	—	—	—	—	—
bit 15							bit 8

—	—	IOSCFS	MCLRE	$\overline{CP}$	WDTE	FOSC1	FOSC0
bit 7							bit 0

bit 15-6 **Unimplemented**: Read as '1'

bit 5 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz INTOSC speed
0 = 4 MHz INTOSC speed

bit 4 **MCLRE:** Master Clear Enable bit
1 = GP3/$\overline{MCLR}$ pin functions as $\overline{MCLR}$
0 = GP3/$\overline{MCLR}$ pin functions as GP3, $\overline{MCLR}$ internally tied to V_{DD}

bit 3 **$\overline{CP}$:** Code Protection bit
1 = Code protection off
0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
00 = LP oscillator with 18 ms DRT
01 = XT oscillator with 18 ms DRT
10 = INTOSC with 1.125 ms DRT (2)
11 = EXTRC with 1.125 ms DRT (2)

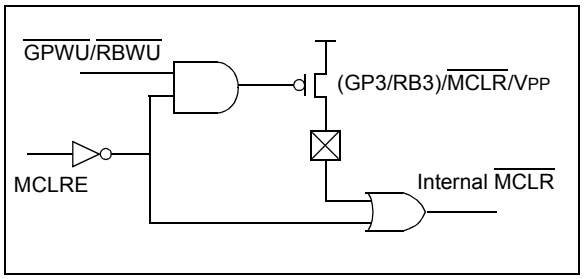
Note 1: Refer to the "*PIC12F510 Memory Programming Specification*" (DS41257) to determine how to access the Configuration Word.

2: It is the responsibility of the application designer to ensure the use of the 1.125 ms (nominal) DRT will result in acceptable operation. Refer to Electrical Specifications for V_{DD} rise time and stability requirements for this mode of operation.

10.3.1 MCLR ENABLE

This Configuration bit, when unprogrammed (left in the '1' state), enables the external MCLR function. When programmed, the MCLR function is tied to the internal VDD and the pin is assigned to be a I/O. See Figure 10-6.

FIGURE 10-6: MCLR SELECT



10.4 Power-on Reset (POR)

The PIC12F510/16F506 devices incorporate an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. The POR is active regardless of the state of the MCLR enable bit. An internal weak pull-up resistor is implemented using a transistor (refer to Table 13-3 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create an external Power-on Reset. A maximum rise time for VDD is specified. See **Section 13.0 "Electrical Characteristics"** for details.

When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the devices must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 10-7.

The Power-on Reset circuit and the Device Reset Timer (see **Section 10.5 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects MCLR, internal or external, to be high. After the time-out period, it will reset the Reset latch and thus end the on-chip Reset signal.

A power-up example where MCLR is held low is shown in Figure 10-8. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of Reset TDRT msec after MCLR goes high.

In Figure 10-9, the on-chip Power-on Reset feature is being used (MCLR and VDD are tied together or the pin is programmed to be (GP3/RB3). The VDD is stable before the Start-up timer times out and there is no problem in getting a proper Reset. However, Figure 10-10 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that MCLR is high and when MCLR and VDD actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 10-9).

Note:	When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Notes AN522, *"Power-Up Considerations"* (DS00522) and AN607, *"Power-up Trouble Shooting"* (DS00607).

RETLW **Return with Literal in W**

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: $k \rightarrow (W)$;
$TOS \rightarrow PC$

Status Affected: None

Description: The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RLF **Rotate Left f through Carry**

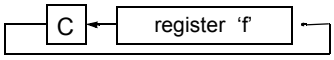
Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



RRF **Rotate Right f through Carry**

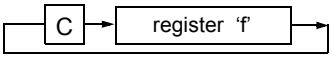
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: $00h \rightarrow WDT$;
$0 \rightarrow$ WDT prescaler;
$1 \rightarrow \overline{TO}$;
$0 \rightarrow \overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$, RBWUF

Description: Time-out Status bit ($\overline{TO}$) is set. The Power-down Status bit ($\overline{PD}$) is cleared.
RBWUF is unaffected.
The WDT and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.
See **Section 10.9 "Power-Down Mode (Sleep)"** on Sleep for more details.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f) - (W) \rightarrow (dest)$

Status Affected: C, DC, Z

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (dest<7:4>)$;
$(f<7:4>) \rightarrow (dest<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W register. If 'd' is '1', the result is placed in register 'f'.

12.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

12.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

12.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart® battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest *"Product Selector Guide"* (DS00148) for the complete list of demonstration, development and evaluation kits.

13.4 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

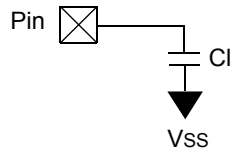
Lowercase (pp) and their meanings:

pp			
2	To	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	Oscillator
cy	Cycle Time	os	OSC1
drt	Device Reset Timer	t0	T0CKI
io	I/O port	wdt	Watchdog Timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (high-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 13-5: LOAD CONDITIONS

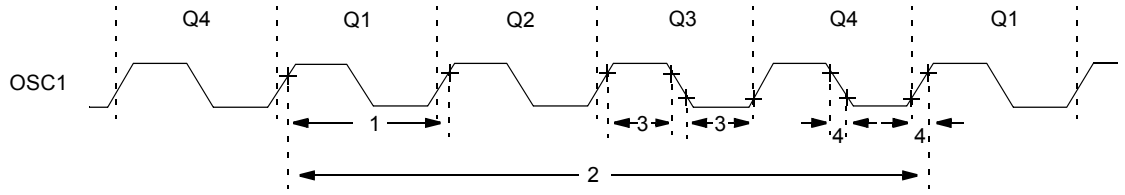


Legend:

C_L = 50 pF for all pins except OSC2

15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

FIGURE 13-6: EXTERNAL CLOCK TIMING



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