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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	38 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP, 8-MSOP (0.118", 3.00mm Width)
Supplier Device Package	8-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f510t-i-ms

TABLE 3-3: PIN DESCRIPTIONS – PIC16F506

Name	Function	Input Type	Output Type	Description
RB0/AN0/C1IN+/ICSPDAT	RB0	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	AN0	AN	—	ADC channel input.
	C1IN+	AN	—	Comparator 1 input.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming data pin.
RB1/AN1/C1IN-/ICSPCLK	RB1	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	AN1	AN	—	ADC channel input.
	C1IN-	AN	—	Comparator 1 input.
	ICSPCLK	ST	—	In-Circuit Serial Programming clock pin.
RB2/AN2/C1OUT	RB2	TTL	CMOS	Bidirectional I/O port.
	AN2	AN	—	ADC channel input.
	C1OUT	—	CMOS	Comparator 1 output.
RB3/$\overline{\text{MCLR}}$/V_{PP}	RB3	TTL	—	Standard TTL input. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	$\overline{\text{MCLR}}$ input – weak pull-up always enabled in this mode.
	V_{PP}	HV	—	Programming voltage input.
RB4/OSC2/CLKOUT	RB4	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	OSC2	—	XTAL	XTAL oscillator output pin.
	CLKOUT	—	CMOS	EXTRC/INTOSC CLKOUT pin (F_{OSC}/4).
RB5/OSC1/CLKIN	RB5	TTL	CMOS	Bidirectional I/O port.
	OSC1	XTAL	—	XTAL oscillator input pin.
	CLKIN	ST	—	EXTRC/EC Schmitt Trigger input.
RC0/C2IN+	RC0	TTL	CMOS	Bidirectional I/O port.
	C2IN+	AN	—	Comparator 2 input.
RC1/C2IN-	RC1	TTL	CMOS	Bidirectional I/O port.
	C2IN-	AN	—	Comparator 2 input.
RC2/CV_{REF}	RC2	TTL	CMOS	Bidirectional I/O port.
	CV_{REF}	—	AN	Programmable Voltage Reference output.
RC3	RC3	TTL	CMOS	Bidirectional I/O port.
RC4/C2OUT	RC4	TTL	CMOS	Bidirectional I/O port.
	C2OUT	—	CMOS	Comparator 2 output.
RC5/T0CKI	RC5	TTL	CMOS	Bidirectional I/O port.
	T0CKI	ST	—	Timer0 clock input.
V_{DD}	V_{DD}	P	—	Positive supply for logic and I/O pins.
V_{SS}	V_{SS}	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog Voltage, HV = High Voltage

4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register, that contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A Reset sets the OPTION<7:0> bits.

Note 1:	If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin (i.e., note that TRIS overrides Option control of $\overline{\text{GPPU}}$/RBPU and $\overline{\text{GPWU}}$/$\overline{\text{RBWU}}$).
2:	If the T0CS bit is set to '1', it will override the TRIS function on the T0CKI pin.

REGISTER 4-3: OPTION_REG: OPTION REGISTER (PIC12F510)

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{GPWU}}$:** Enable Wake-up On Pin Change bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6 **$\overline{\text{GPPU}}$:** Enable Weak Pull-Ups bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

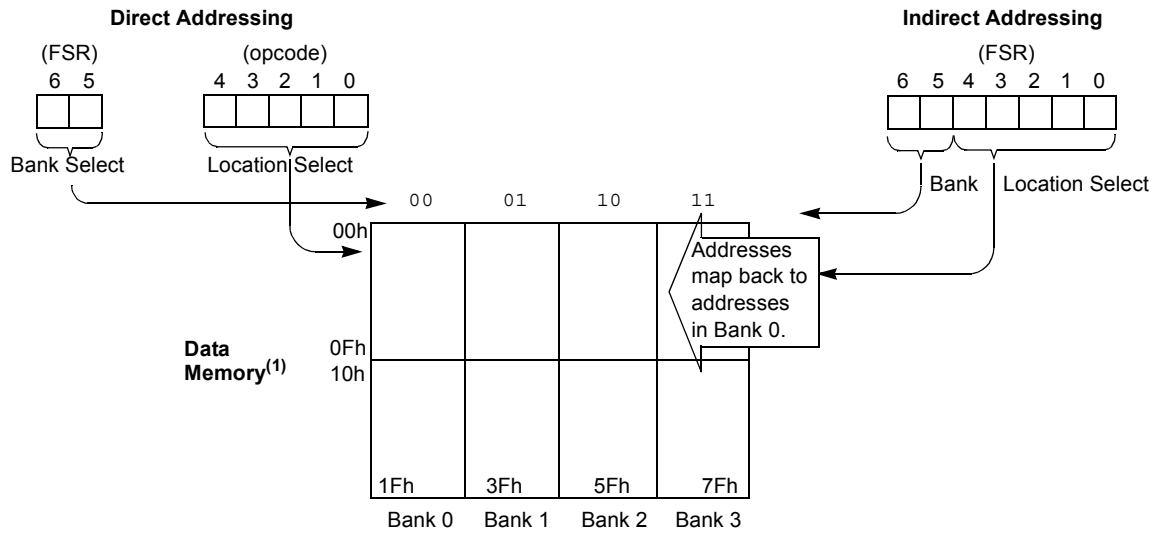
bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

FIGURE 4-6: DIRECT/INDIRECT ADDRESSING (PIC16F506)



Note 1: For register map detail, see Figure 4-3.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRISGPIO(1)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISB(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISC(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	OPTION(1)	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION(2)	$\overline{RBWU}$	$\overline{RBPU}$	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS(1)	GPWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	qq0q quuu(3)
03h	STATUS(2)	RBWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	qq0q quuu(3)
06h	GPIO(1)	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
06h	PORTB(2)	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC(2)	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: – = unimplemented read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: PIC12F510 only.

2: PIC16F506 only.

3: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

TABLE 5-2: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)

Priority	RB0	RB1	RB2	RB3	RB4	RB5
1	AN0/C1IN+	AN1/C1IN-	AN2	Input/$\overline{MCLR}$	OSC2/CLKOUT	OSC1/CLKIN
2	TRISB	TRISB	C1OUT	—	TRISB	TRISB
3	—	—	TRISB	—	—	—

TABLE 5-3: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)

Priority	RC0	RC1	RC2	RC3	RC4	RC5
1	C2IN+	C2IN-	CV_{REF}	TRISC	C2OUT	T0CKI
2	TRISC	TRISC	TRISC	—	TRISC	TRISC

TABLE 5-4: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC12F510)

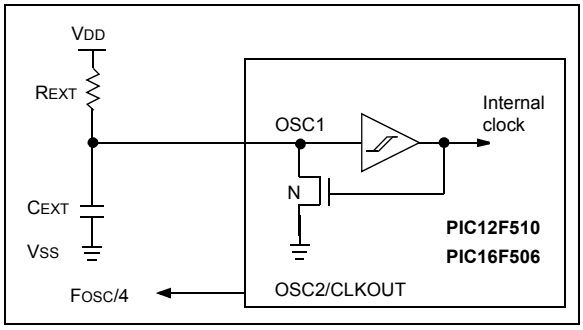
Priority	GP0	GP1	GP2	GP3	GP4	GP5
1	AN0/C1IN+	AN1/C1IN-	AN2	Input/$\overline{MCLR}$	OSC2	OSC1/CLKIN
2	TRISIO	TRISIO	C1OUT	—	TRISIO	TRISIO
3	—	—	T0CKI	—	—	—
4	—	—	TRISIO	—	—	—

Although the oscillator will operate with no external capacitor (C_{EXT} = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no capacitance or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

Section 13.0 "Electrical Characteristics", shows RC frequency variation from part-to-part due to normal process variation. The variation is larger for larger values of R (since leakage current variation will affect RC frequency more for large R) and for smaller values of C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications section for variation of oscillator frequency due to V_{DD} for given R_{EXT}/C_{EXT} values, as well as frequency variation due to operating temperature for given R, C and V_{DD} values.

FIGURE 10-5: EXTERNAL RC OSCILLATOR MODE



10.2.5 INTERNAL 4/8 MHz RC OSCILLATOR

The internal RC oscillator provides a fixed 4/8 MHz (nominal) system clock (see **Section 13.0 "Electrical Characteristics"** for information on variation over voltage and temperature).

In addition, a calibration instruction is programmed into the last address of memory, which contains the calibration value for the internal RC oscillator. This location is always uncode protected, regardless of the code-protect settings. This value is programmed as a `MOVLW XX` instruction where `XX` is the calibration value, and is placed at the Reset vector. This will load the W register with the calibration value upon Reset and the PC will then roll over to the users program at address 0x000. The user then has the option of writing the value to the OSCCAL Register (05h) or ignoring it.

OSCCAL, when written to with the calibration value, will "trim" the internal oscillator to remove process variation from the oscillator frequency.

Note:	Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part so it can be reprogrammed correctly later.

For the PIC12F510/16F506 devices, only bits <7:1> of OSCCAL are used for calibration. See Register 4-5 for more information.

Note:	The 0 bit of OSCCAL is unimplemented and should be written as '0' when modifying OSCCAL for compatibility with future devices.

10.3 Reset

The device differentiates between various kinds of Reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Time-out Reset during normal operation
- WDT Time-out Reset during Sleep
- Wake-up from Sleep Reset on pin change
- Wake-up from Sleep Reset on comparator change

Some registers are not reset in any way, they are unknown on POR and unchanged in any other Reset. Most other registers are reset to "Reset state" on Power-on Reset (POR), $\overline{\text{MCLR}}$, WDT or Wake-up from Sleep Reset on pin change or wake-up from Sleep Reset on comparator change. The exceptions are $\overline{\text{TO}}$, $\overline{\text{PD}}$, CWUF and RBWUF/GPWUF bits. They are set or cleared differently in different Reset situations. These bits are used in software to determine the nature of Reset. See Table 10-4 for a full description of Reset states of all registers.

TABLE 10-3: RESET CONDITIONS FOR REGISTERS – PIC12F510

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up On Pin Change, Wake-up on Comparator Change
W	—	qqqq qqqu(1)	qqqq qqqu(1)
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	qq0q quuu(2)
FSR	04h	110x xxxx	11uu uuuu
OSCCAL	05h	1111 111-	uuuu uuu-
GPIO	06h	--xx xxxx	--uu uuuu
CM1CON0	07h	1111 1111	uuuu uuuu
ADCON0	08h	1111 1100	uu11 1100
ADRES	09h	xxxx xxxx	uuuu uuuu
OPTION	—	1111 1111	1111 1111
TRISIO	—	--11 1111	--11 1111

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition.

Note 1: Bits <7:2> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.

2: See Table 10-5 for Reset value for specific conditions.

TABLE 10-4: RESET CONDITIONS FOR REGISTERS – PIC16F506

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up On Pin Change, Wake-up on Comparator Change
W	—	qqqq qqqu(1)	qqqq qqqu(1)
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	10uq quuu(2)
FSR	04h	100x xxxx	10uu uuuu
OSCCAL	05h	1111 111-	uuuu uuu-
PORTB	06h	--xx xxxx	--uu uuuu
PORTC	07h	--xx xxxx	--uu uuuu
CM1CON0	08h	1111 1111	uuuu uuuu
ADCON0	09h	1111 1100	uu11 1100
ADRES	0Ah	xxxx xxxx	uuuu uuuu
CM2CON0	0Bh	1111 1111	uuuu uuuu
VRCON	0Ch	0011 1111	uuuu uuuu
OPTION	—	1111 1111	1111 1111
TRISB	—	--11 1111	--11 1111
TRISC	—	--11 1111	--11 1111

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition.

Note 1: Bits <7:2> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.

2: See Table 10-5 for Reset value for specific conditions.

TABLE 10-5: RESET CONDITION FOR SPECIAL REGISTERS

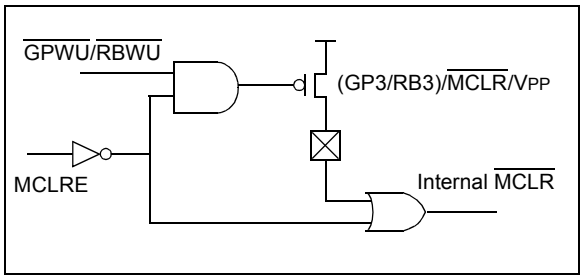
	STATUS Addr: 03h	PCL Addr: 02h
Power-on Reset	0001 1xxx	1111 1111
$\overline{\text{MCLR}}$ Reset during normal operation	000u uuuu	1111 1111
$\overline{\text{MCLR}}$ Reset during Sleep	0001 0uuu	1111 1111
WDT Reset during Sleep	0000 0uuu	1111 1111
WDT Reset normal operation	0000 uuuu	1111 1111
Wake-up from Sleep Reset on pin change	1001 0uuu	1111 1111
Wake from Sleep Reset on Comparator Change	0101 0uuu	1111 1111

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as '0'.

10.3.1 MCLR ENABLE

This Configuration bit, when unprogrammed (left in the '1' state), enables the external MCLR function. When programmed, the MCLR function is tied to the internal VDD and the pin is assigned to be a I/O. See Figure 10-6.

FIGURE 10-6: MCLR SELECT



10.4 Power-on Reset (POR)

The PIC12F510/16F506 devices incorporate an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. The POR is active regardless of the state of the MCLR enable bit. An internal weak pull-up resistor is implemented using a transistor (refer to Table 13-3 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create an external Power-on Reset. A maximum rise time for VDD is specified. See **Section 13.0 "Electrical Characteristics"** for details.

When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the devices must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 10-7.

The Power-on Reset circuit and the Device Reset Timer (see **Section 10.5 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects MCLR, internal or external, to be high. After the time-out period, it will reset the Reset latch and thus end the on-chip Reset signal.

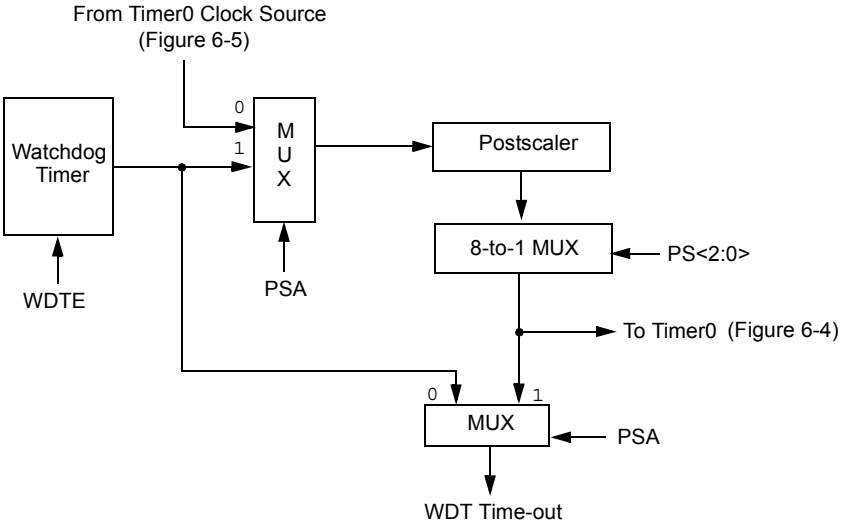
A power-up example where MCLR is held low is shown in Figure 10-8. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of Reset TDRT msec after MCLR goes high.

In Figure 10-9, the on-chip Power-on Reset feature is being used (MCLR and VDD are tied together or the pin is programmed to be (GP3/RB3). The VDD is stable before the Start-up timer times out and there is no problem in getting a proper Reset. However, Figure 10-10 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that MCLR is high and when MCLR and VDD actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 10-9).

Note:	When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Notes AN522, *"Power-Up Considerations"* (DS00522) and AN607, *"Power-up Trouble Shooting"* (DS00607).

FIGURE 10-11: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

TABLE 10-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	OPTION(1)	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION(2)	$\overline{RBWU}$	$\overline{RBPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded boxes = Not used by Watchdog Timer. – = unimplemented, read as '0', u = unchanged.

Note 1: PIC12F510 only.

2: PIC16F506 only.

11.0 INSTRUCTION SET SUMMARY

The PIC16 instruction set is highly orthogonal and is comprised of three basic categories.

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 12-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 11-1, while the various opcode fields are summarized in Table 11-1.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bits affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 11-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top-of-Stack
PC	Program Counter
WDT	Watchdog Timer counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

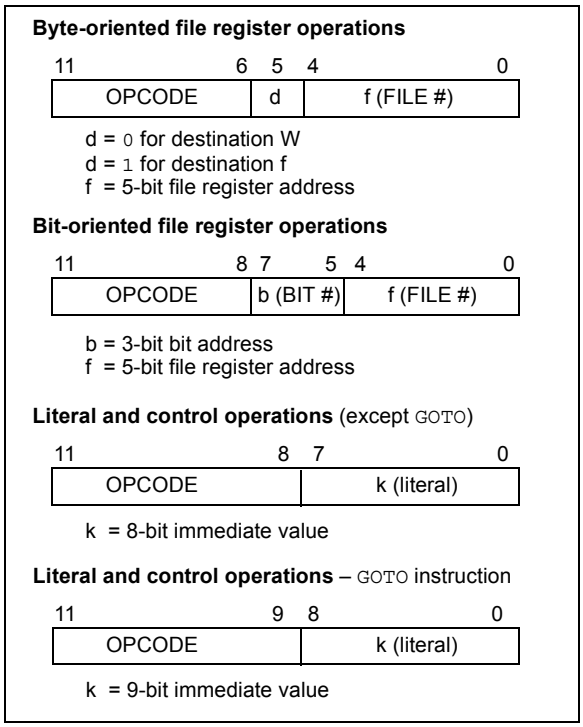
All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Figure 11-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 11-1: GENERAL FORMAT FOR INSTRUCTIONS



RETLW **Return with Literal in W**

Syntax: [*label*] RETLW k

Operands: $0 \le k \le 255$

Operation: $k \rightarrow (W)$;
$TOS \rightarrow PC$

Status Affected: None

Description: The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RLF **Rotate Left f through Carry**

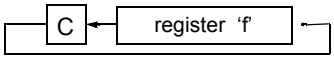
Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



RRF **Rotate Right f through Carry**

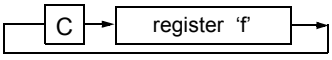
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: $00h \rightarrow WDT$;
$0 \rightarrow$ WDT prescaler;
$1 \rightarrow \overline{TO}$;
$0 \rightarrow \overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$, RBWUF

Description: Time-out Status bit ($\overline{TO}$) is set. The Power-down Status bit ($\overline{PD}$) is cleared.
RBWUF is unaffected.
The WDT and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.
See **Section 10.9 "Power-Down Mode (Sleep)"** on Sleep for more details.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f) - (W) \rightarrow (dest)$

Status Affected: C, DC, Z

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (dest<7:4>)$;
$(f<7:4>) \rightarrow (dest<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W register. If 'd' is '1', the result is placed in register 'f'.

12.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

12.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

12.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

12.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

12.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

FIGURE 13-1: VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C (PIC12F510)

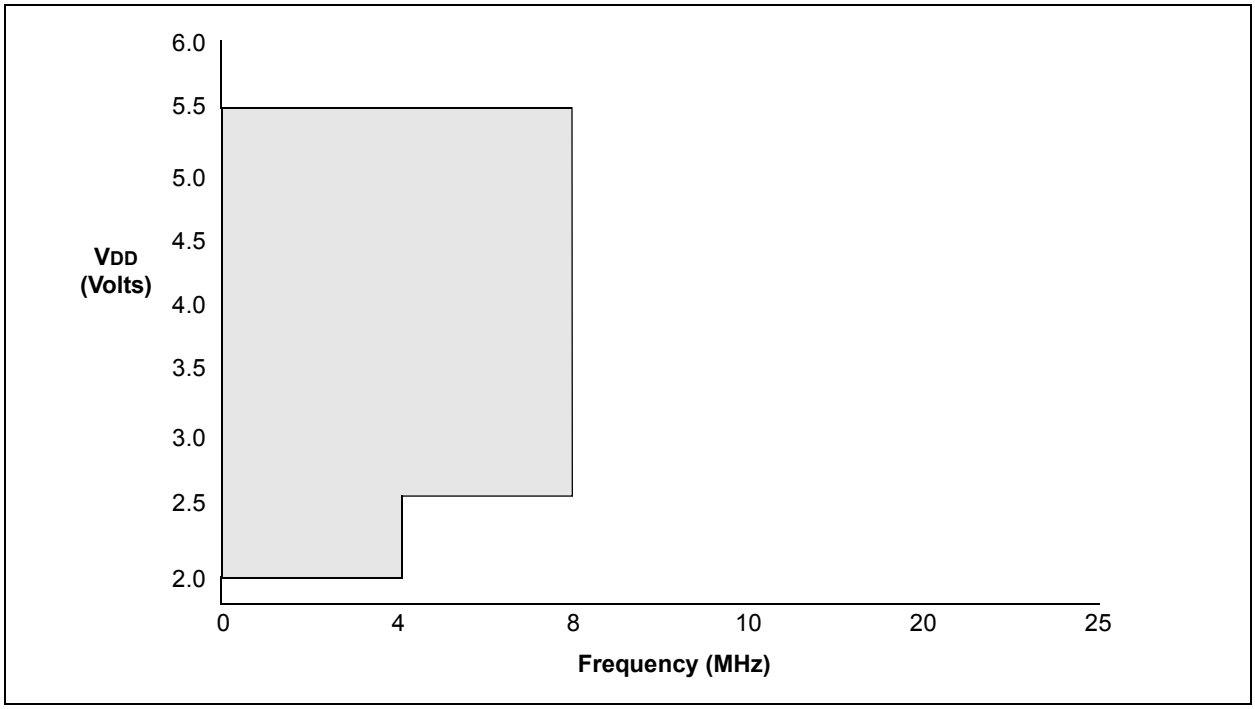
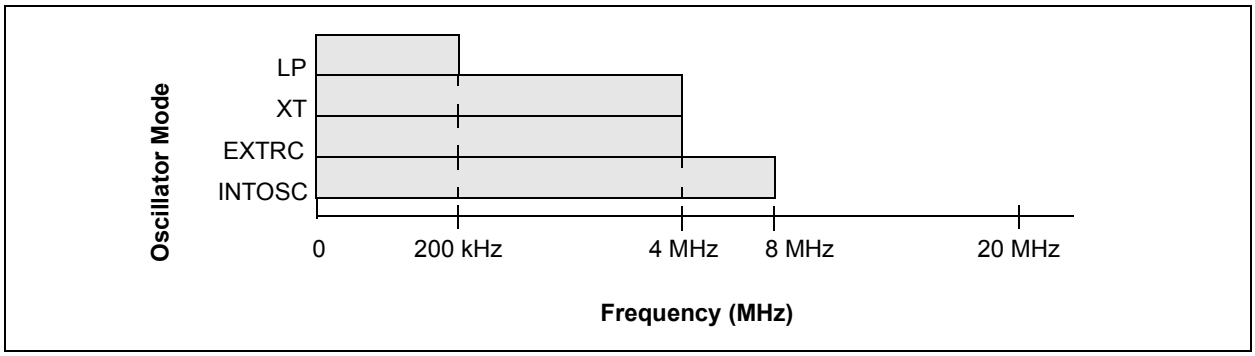


FIGURE 13-2: MAXIMUM OSCILLATOR FREQUENCY TABLE (PIC12F510)



13.1 DC Characteristics: PIC12F510/16F506 (Industrial)

DC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 40°C ≤ TA ≤ +85°C (industrial)				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	See **Figure 14-1**
D002	VDR	**RAM Data Retention Voltage(2)**	—	1.5*	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See **Section 10.4 "Power-on Reset (POR)"** for details
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See **Section 10.4 "Power-on Reset (POR)"** for details
D010	IDD	**Supply Current(3,4)**	— —	175 0.625	275 1.1	µA mA	FOSC = 4 MHz, VDD = 2.0V FOSC = 4 MHz, VDD = 5.0V
			— —	250 1.0	450 1.5	µA mA	FOSC = 8 MHz, VDD = 2.0V FOSC = 8 MHz, VDD = 5.0V
			—	1.4	2.0	mA	FOSC = 20 MHz, VDD = 5.0V
			— —	11 38	15 52	µA µA	FOSC = 32 kHz, VDD = 2.0V FOSC = 32 kHz, VDD = 5.0V
D020	IPD	**Power-down Current(5)**	— —	0.1 0.35	1.2 2.4	µA µA	VDD = 2.0V VDD = 5.0V
D022	IWDT	**WDT Current(5)**	— —	1.0 7.0	3.0 16.0	µA µA	VDD = 2.0V VDD = 5.0V
D023	ICMP	**Comparator Current(5)**	— —	15 55	22 67	µA µA	VDD = 2.0V (per comparator) VDD = 5.0V (per comparator)
D022	ICVREF	**CVREF Current(5)**	— —	30 75	60 125	µA µA	VDD = 2.0V (high range) VDD = 5.0V (high range)
D023	IFVR	**Internal 0.6V Fixed Voltage Reference Current(5)**	— —	85 175	120 205	µA µA	VDD = 2.0V (0.6V reference and 1 comparator enabled) VDD = 5.0V (0.6V reference and 1 comparator enabled)
D024	ΔIAD	**A/D Conversion Current(5)**	—	120	150	µA	2.0V
			—	200	250	µA	5.0V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

4: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

5: For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

6: Does not include current through REXT. The current through the resistor can be estimated by the formula: I = VDD/2REXT (mA) with REXT in kΩ.

TABLE 13-7: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TMCL	$\overline{MCLR}$ Pulse Width (low)	2000*	—	—	ns	VDD = 5.0V
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	9* 9*	18* 18*	30* 40*	ms ms	VDD = 5.0V (Industrial) VDD = 5.0V (Extended)
32	TDRT	Device Reset Timer Period					
		Standard	9* 9*	18* 18*	30* 40*	ms ms	VDD = 5.0V (Industrial) VDD = 5.0V (Extended)
		Short	0.5* 0.5*	1.125* 1.125*	2* 2.5*	ms ms	VDD = 5.0V (Industrial) VDD = 5.0V (Extended)
34	TIOZ	I/O high-impedance from $\overline{MCLR}$ low	—	—	2000*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-9: TIMER0 CLOCK TIMINGS

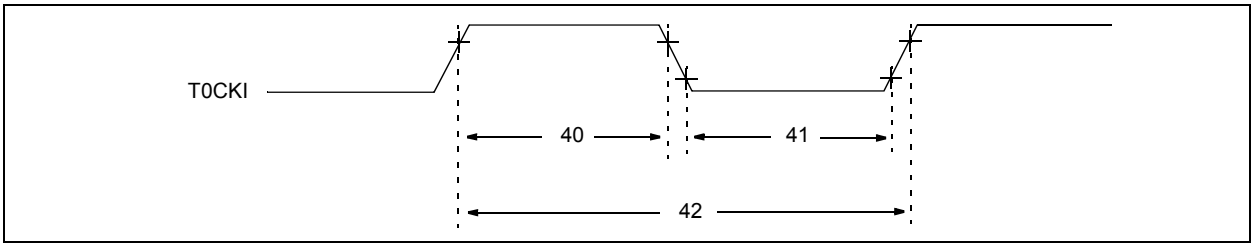


TABLE 13-8: TIMER0 CLOCK REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)				
Parm No.	**Sym**	**Characteristic**		**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		20 or TCY + 40* N	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

FIGURE 14-6: MAXIMUM WDT IPD vs. VDD OVER TEMPERATURE

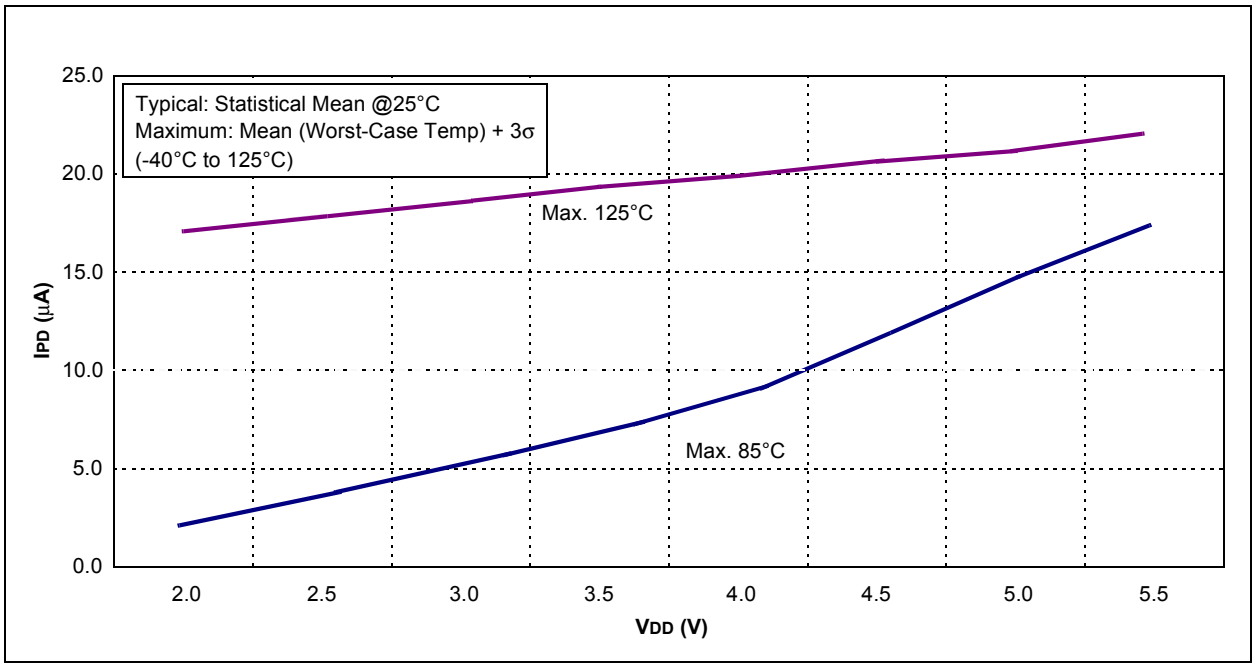
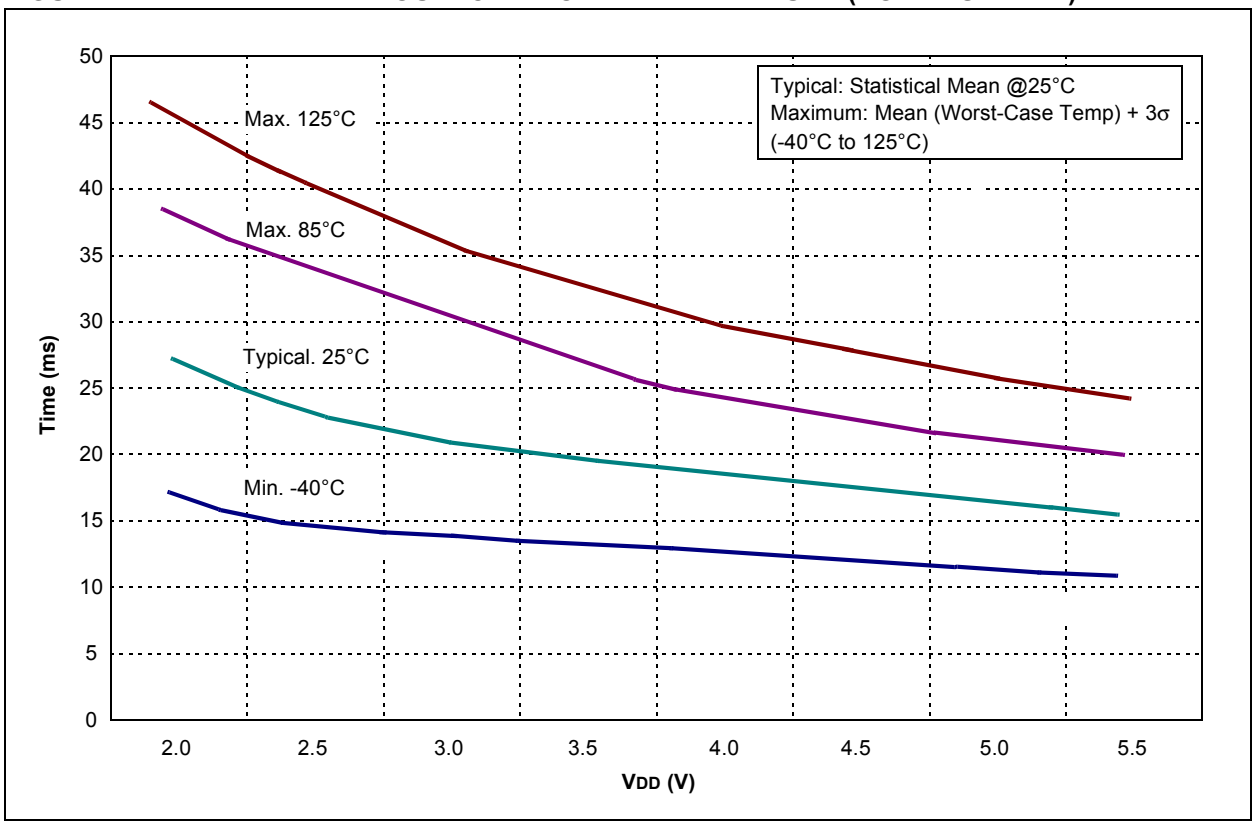
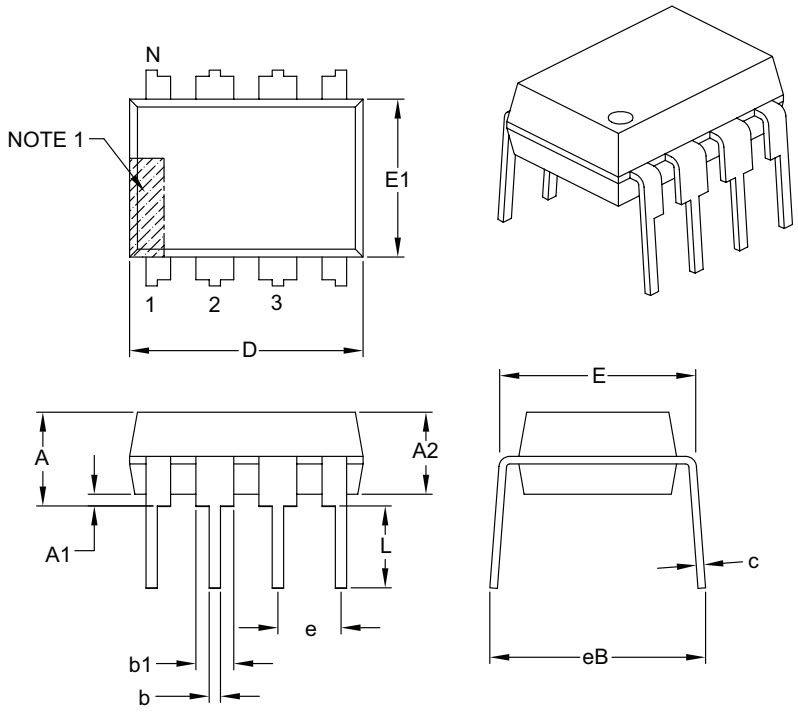


FIGURE 14-7: WDT TIME-OUT vs. VDD OVER TEMPERATURE (NO PRESCALER)



8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

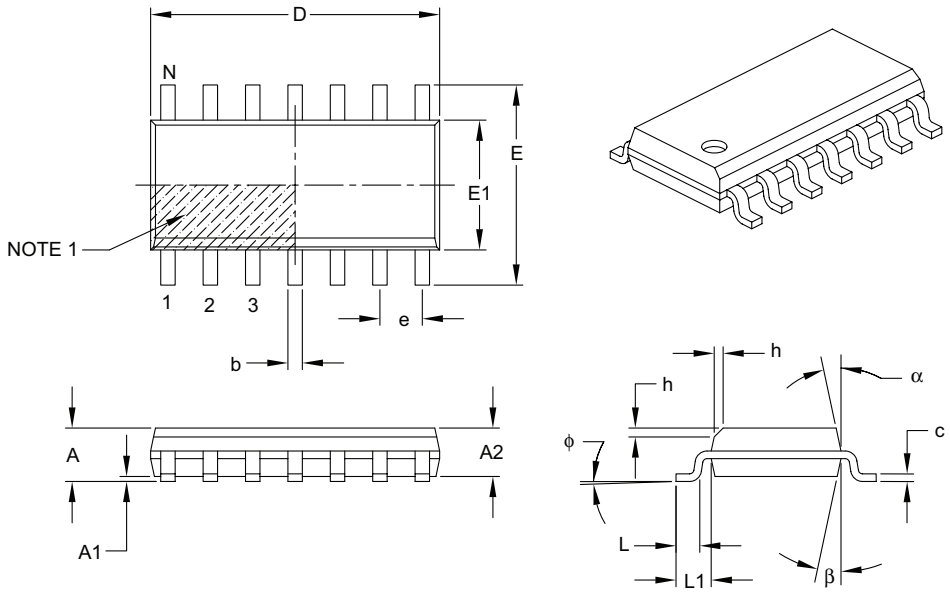
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

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