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Details	
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Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	38 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
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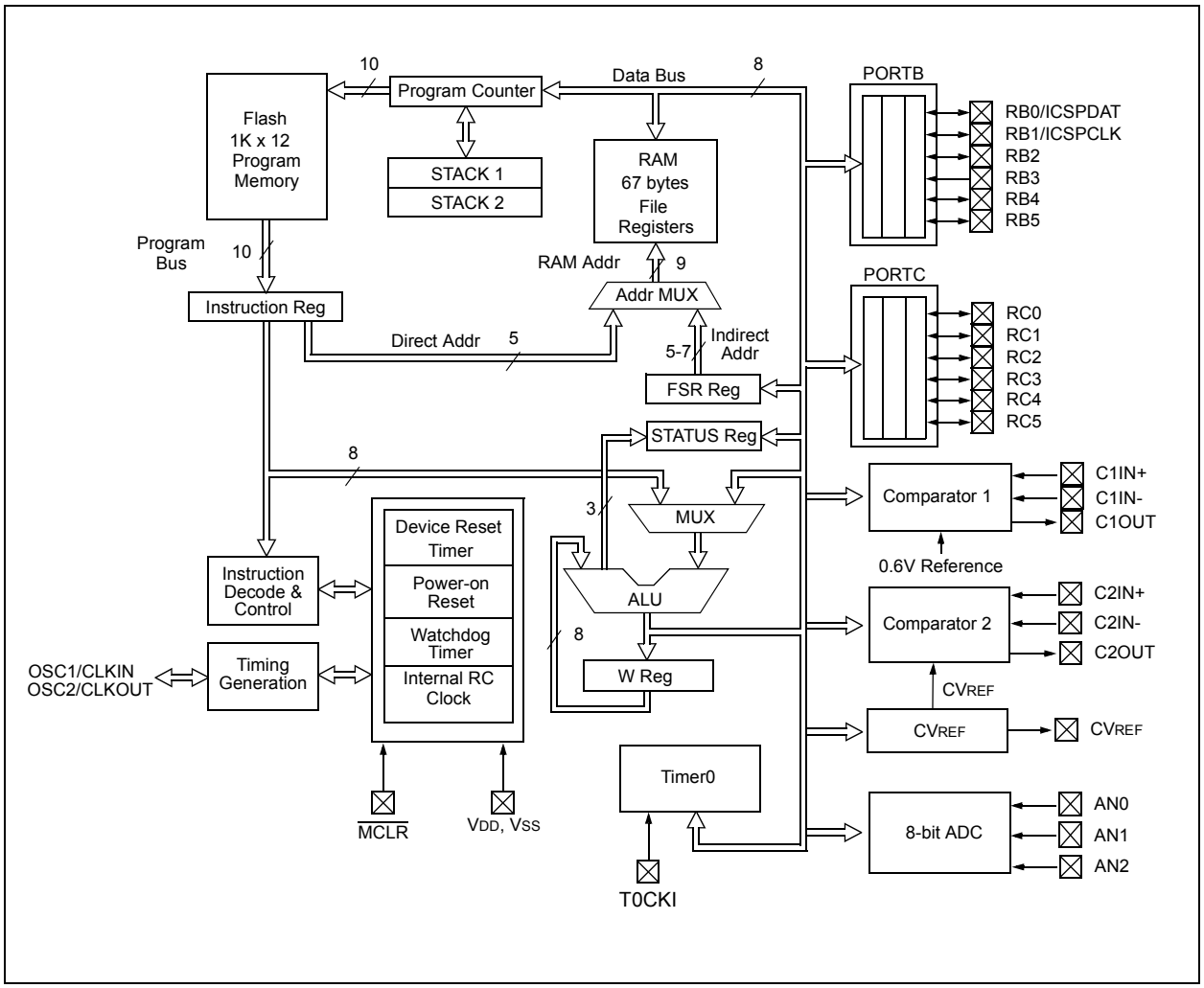
FIGURE 3-2: PIC16F506 SERIES BLOCK DIAGRAM



4.0 MEMORY ORGANIZATION

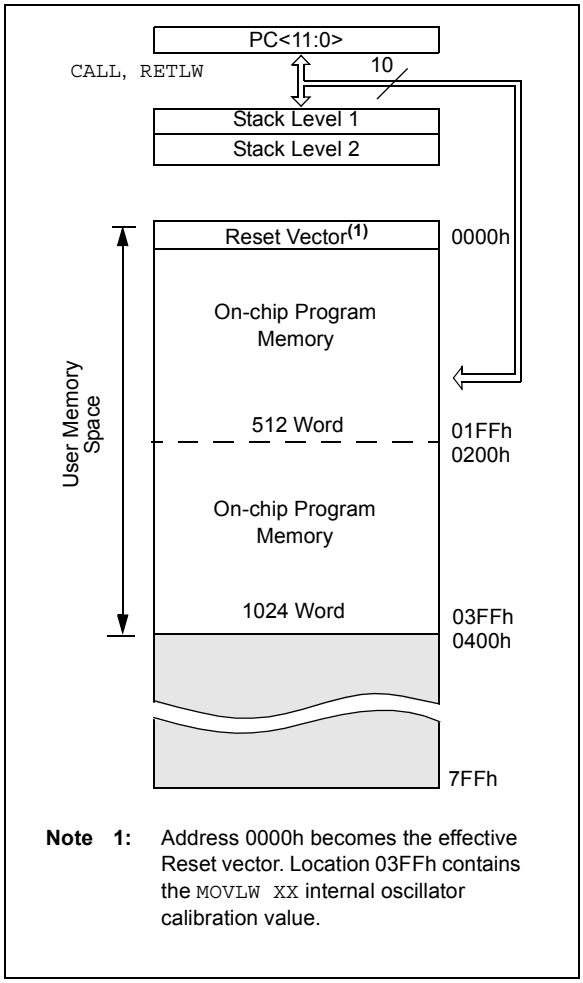
The PIC12F510/16F506 memories are organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using STATUS register bit PA0. For the PIC12F510 and PIC16F506, with data memory register files of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Select Register (FSR).

4.1 Program Memory Organization for the PIC12F510/16F506

The PIC12F510/16F506 devices have a 10-bit Program Counter (PC) capable of addressing a 2K x 12 program memory space.

Only the first 1K x 12 (0000h-03FFh) are physically implemented (see Figure 4-1). Accessing a location above these boundaries will cause a wraparound within the 1K x 12 space. The effective Reset vector is a 0000h (see Figure 4-1). Location 03FFh contains the internal clock oscillator calibration value. This value should never be overwritten.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F510/16F506



Note 1: Address 0000h becomes the effective Reset vector. Location 03FFh contains the `MOVLW XX` internal oscillator calibration value.

4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register, that contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A Reset sets the OPTION<7:0> bits.

Note 1:	If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin (i.e., note that TRIS overrides Option control of $\overline{\text{GPPU}}$/RBPU and $\overline{\text{GPWU}}$/$\overline{\text{RBWU}}$).
2:	If the T0CS bit is set to '1', it will override the TRIS function on the T0CKI pin.

REGISTER 4-3: OPTION_REG: OPTION REGISTER (PIC12F510)

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{GPWU}}$:** Enable Wake-up On Pin Change bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6 **$\overline{\text{GPPU}}$:** Enable Weak Pull-Ups bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

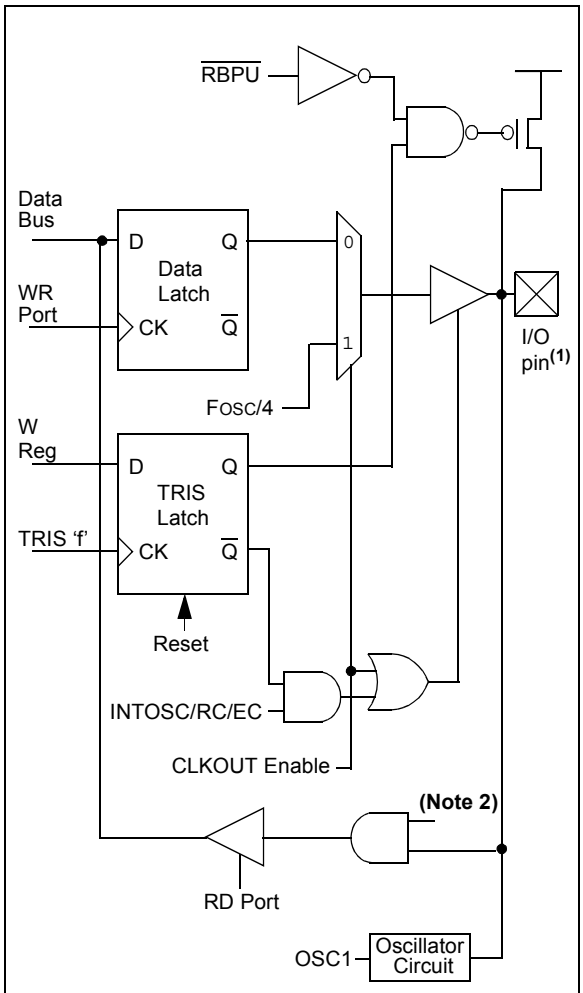
bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

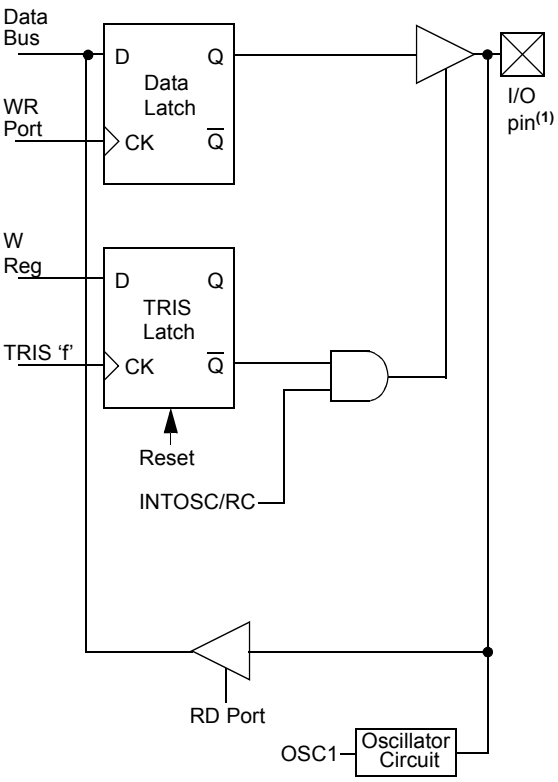
FIGURE 5-6: BLOCK DIAGRAM OF RB4



Note 1: I/O pins have protection diodes to VDD and VSS.

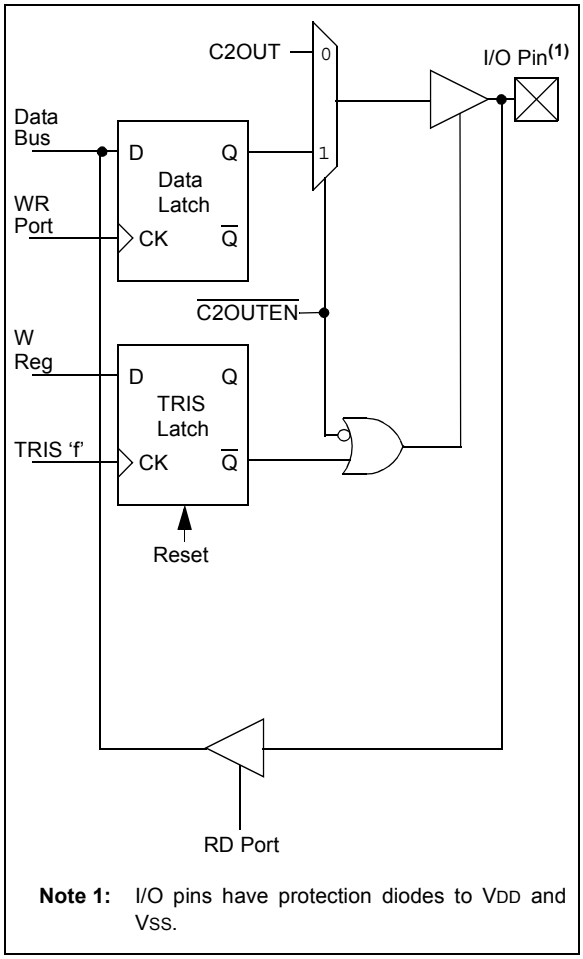
2: Input mode is disabled when pin is used for oscillator.

FIGURE 5-7: BLOCK DIAGRAM OF GP4



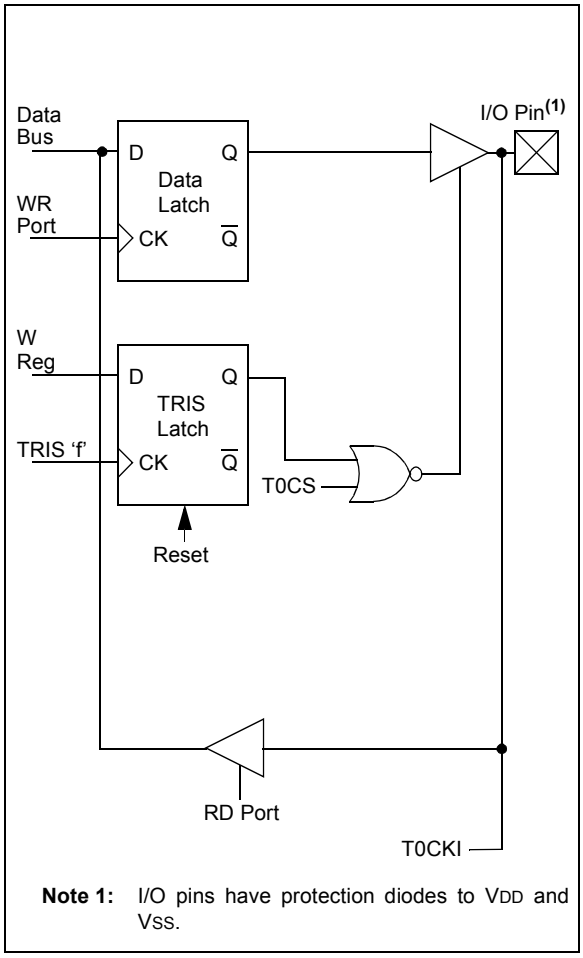
Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 5-12: BLOCK DIAGRAM OF RC4



Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 5-13: BLOCK DIAGRAM OF RC5



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 5-6: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC16F506 PORTB)(1), (2)

	RB0	RB0	RB0	RB1	RB1	RB2	RB2	RB3	RB4	RB5
CM1CON0										
C1ON	—	0	1	0	1	0	1	—	—	—
C1PREF	—	—	0	—	—	—	—	—	—	—
C1NREF	—	—	—	—	0	—	—	—	—	—
$\overline{\text{C1T0CS}}$	—	—	—	—	—	—	—	—	—	—
$\overline{\text{C1OUTEN}}$	—	—	—	—	—	—	1	—	—	—
CM2CON0										
C2ON	1	—	—	—	—	—	—	—	—	—
C2PREF1	0	—	—	—	—	—	—	—	—	—
C2PREF2	1	—	—	—	—	—	—	—	—	—
C2NREF	—	—	—	—	—	—	—	—	—	—
$\overline{\text{C2OUTEN}}$	—	—	—	—	—	—	—	—	—	—
OPTION										
T0CS	—	—	—	—	—	—	—	—	—	—
ADCON0										
ANS<1:0>	00, 01	00, 01	00, 01	00, 01, 10	00, 01, 10	00	00	—	—	—
CONFIG										
MCLRE	—	—	—	—	—	—	—	0	—	—
INTOSC	—	—	—	—	—	—	—	—	—	—
LP	—	—	—	—	—	—	—	—	Disabled	Disabled
EXTRC	—	—	—	—	—	—	—	—	—	Disabled
XT	—	—	—	—	—	—	—	—	Disabled	Disabled
EC	—	—	—	—	—	—	—	—	—	Disabled
HS	—	—	—	—	—	—	—	—	Disabled	Disabled
INTOSC CLKOUT	—	—	—	—	—	—	—	—	Disabled	Disabled
EXTRC CLOCKOUT	—	—	—	—	—	—	—	—	Disabled	Disabled

Note 1: Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

2: Shaded cells indicate the bit status does not affect the pins digital functionality.

TABLE 5-7: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC16F506 PORTC)(1), (2)

	RC0	RC0	RC1	RC1	RC2	RC3	RC4	RC4	RC5	RC5
CM2CON0										
C2ON	0	1	0	1	—	—	0	1	—	—
C2PREF1	—	0	—	—	—	—	—	—	—	—
C2PREF2	—	0	—	—	—	—	—	—	—	—
C2NREF	—	—	—	0	—	—	—	—	—	—
$\overline{\text{C2OUTEN}}$	—	—	—	—	—	—	—	1	—	—
VRCON0										
VROE	—	—	—	—	0	—	—	—	—	—
OPTION										
T0CS	—	—	—	—	—	—	—	—	0	—

Note 1: Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

2: Shaded cells indicate the bit status does not affect the pins digital functionality.

6.1 Using Timer0 With An External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

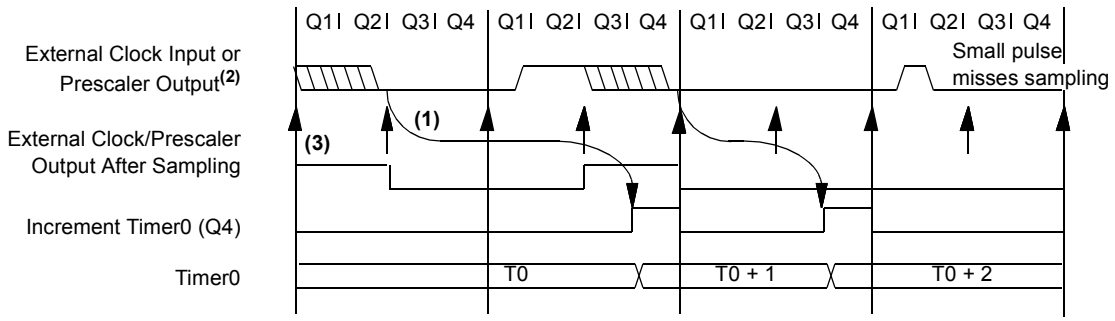
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of an external clock with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI or the comparator output to be high for at least 2TOSC (and a small RC delay of 2Tt0H) and low for at least 2TOSC (and a small RC delay of 2Tt0H). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI or the comparator output to have a period of at least 4TOSC (and a small RC delay of 4Tt0H) divided by the prescaler value. The only requirement on T0CKI or the comparator output high and low time is that they do not violate the minimum pulse width requirement of Tt0H. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3TOSC to 7TOSC. (Duration of Q = TOSC). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4TOSC max.

2: External clock if no prescaler selected; prescaler output otherwise.

3: The arrows indicate the points in time where sampling occurs.

6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (see Figure 10-12). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet.

Note:	The prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1, x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a Reset, the prescaler contains all ‘`0`’s.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on-the-fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0 → WDT)

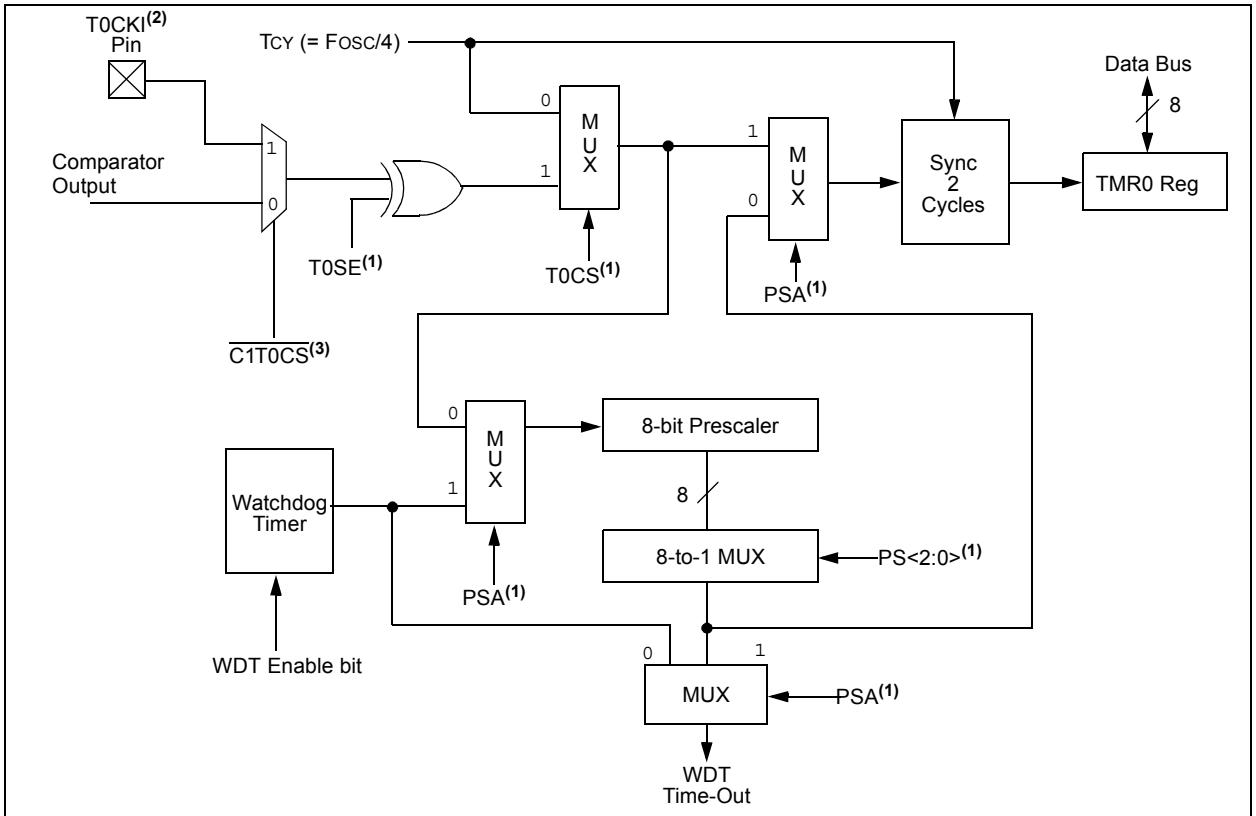
```
CLRWDT              ;Clear WDT
CLRF   TMR0         ;Clear TMR0 & Prescaler
MOVLW  '00xx1111'b  ;These 3 lines (5, 6, 7)
OPTION              ;are required only if
                    ;desired
CLRWDT              ;PS<2:0> are 000 or 001
MOVLW  '00xx1xxx'b  ;Set Postscaler to
OPTION              ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT              ;Clear WDT and
                    ;prescaler
MOVLW  'xxxx0xxx'   ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

FIGURE 6-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

2: T0CKI is shared with pin GP2 on the PIC12F510 and shared with RC5 on the PIC16F506.

3: Bit $\overline{C1T0CS}$ is located in the CM1CON0 register.

REGISTER 7-2: CM1CON0: COMPARATOR C1 CONTROL REGISTER (PIC16F506)

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C1OUT:** Comparator Output bit
1 = VIN+ > VIN-
0 = VIN+ < VIN-

bit 6 **$\overline{\text{C1OUTEN}}$:** Comparator Output Enable bit(1), (2)
1 = Output of comparator is NOT placed on the C1OUT pin
0 = Output of comparator is placed in the C1OUT pin

bit 5 **C1POL:** Comparator Output Polarity bit(2)
1 = Output of comparator is not inverted
0 = Output of comparator is inverted

bit 4 **$\overline{\text{C1T0CS}}$:** Comparator TMR0 Clock Source bit(2)
1 = TMR0 clock source selected by T0CS control bit
0 = Comparator output used as TMR0 clock source

bit 3 **C1ON:** Comparator Enable bit
1 = Comparator is on
0 = Comparator is off

bit 2 **C1NREF:** Comparator Negative Reference Select bit(2)
1 = C1IN- pin
0 = 0.6V internal reference

bit 1 **C1PREF:** Comparator Positive Reference Select bit(2)
1 = C1IN+ pin
0 = C1IN- pin

bit 0 **$\overline{\text{C1WU}}$:** Comparator Wake-up On Change Enable bit(2)
1 = Wake-up On Comparator Change is disabled
0 = Wake-up On Comparator Change is enabled

Note 1: Overrides T0CS bit for TRIS control of RB2.
2: When comparator is turned on, these control bits assert themselves. Otherwise, the other registers have precedence.

REGISTER 7-3: CM2CON0: COMPARATOR C2 CONTROL REGISTER (PIC16F506)

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
C2OUT	$\overline{\text{C2OUTEN}}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{\text{C2WU}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C2OUT:** Comparator Output bit
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$

bit 6 **$\overline{\text{C2OUTEN}}$:** Comparator Output Enable bit(1), (2)
1 = Output of comparator is NOT placed on the C2OUT pin
0 = Output of comparator is placed in the C2OUT pin

bit 5 **C2POL:** Comparator Output Polarity bit(2)
1 = Output of comparator not inverted
0 = Output of comparator inverted

bit 4 **C2PREF2:** Comparator Positive Reference Select bit(2)
1 = C1IN+ pin
0 = C2IN- pin

bit 3 **C2ON:** Comparator Enable bit
1 = Comparator is on
0 = Comparator is off

bit 2 **C2NREF:** Comparator Negative Reference Select bit(2)
1 = C2IN- pin
0 = CV_{REF}

bit 1 **C2PREF1:** Comparator Positive Reference Select bit(2)
1 = C2IN+ pin
0 = C2PREF2 controls analog input selection

bit 0 **$\overline{\text{C2WU}}$:** Comparator Wake-up on Change Enable bit(2)
1 = Wake-up on Comparator change is disabled
0 = Wake-up on Comparator change is enabled.

Note 1: Overrides TOCS bit for TRIS control of RC4.

2: When comparator is turned on, these control bits assert themselves. Otherwise, the other registers have precedence.

10.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC12F510/16F506 microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These features are:

- Oscillator Selection
- Reset:
  - Power-on Reset (POR)
  - Device Reset Timer (DRT)
  - Wake-up from Sleep on Pin Change
- Watchdog Timer (WDT)
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™ (ICSP™)
- Clock Out

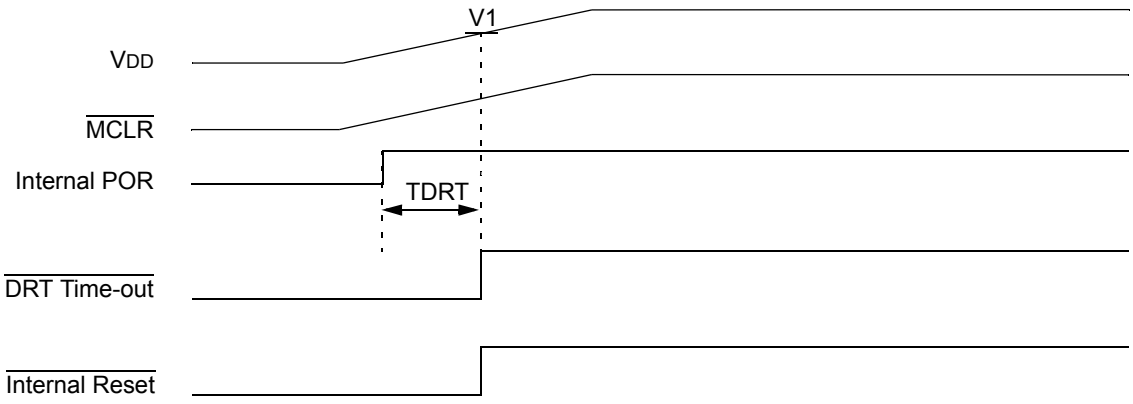
The PIC12F510/16F506 devices have a Watchdog Timer, which can be shut off only through Configuration bit WDTE. It runs off of its own RC oscillator for added reliability. If using HS (PIC16F506), XT or LP selectable oscillator options, there is always a delay, provided by the Device Reset Timer (DRT), intended to keep the chip in Reset until the crystal oscillator is stable. If using INTOSC, EXTRC or EC there is an 1.125 ms (nominal) delay only on V_{DD} power-up. With this timer on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through a change-on-input pin or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application, including an internal 4/8 MHz oscillator. The EXTRC oscillator option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options.

10.1 Configuration Bits

The PIC12F510/16F506 Configuration Words consist of 12 bits. Configuration bits can be programmed to select various device configurations. Three bits are for the selection of the oscillator type; (two bits on the PIC12F510), one bit is the Watchdog Timer enable bit, one bit is the $\overline{MCLR}$ enable bit and one bit is for code protection (Register 10-1, Register 10-2).

FIGURE 10-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



Note: When V_{DD} rises slowly, the T_{DRT} time-out expires long before V_{DD} has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ V_{DD} min.

10.5 Device Reset Timer (DRT)

On the PIC12F510/16F506 devices, the DRT runs any time the device is powered up. DRT runs from Reset and varies based on oscillator selection and Reset type (see Table 10-6).

The DRT operates from a free running on-chip oscillator that is separate from INTOSC. The processor is kept in Reset as long as the DRT is active. The DRT delay allows VDD to rise above VDD minimum and for the oscillator to stabilize.

Oscillator circuits, based on crystals or ceramic resonators, require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the devices in a Reset for a set period, as stated in Table 10-6, after $\overline{MCLR}$ has reached a logic high (VIH $\overline{MCLR}$) level. Programming (GP3/RB3)/$\overline{MCLR}$/VPP as $\overline{MCLR}$ and using an external RC network connected to the $\overline{MCLR}$ input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the (GP3/RB3)/$\overline{MCLR}$/VPP pin as a general purpose input.

The DRT delays will vary from chip-to-chip due to VDD, temperature and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out from Sleep. This is particularly important for applications using the WDT to wake from Sleep mode automatically.

Reset sources are POR, $\overline{MCLR}$, WDT time-out, Wake-up on Pin Change and Wake-up on Comparator Change. See **Section 10.9.2 "Wake-up from Sleep Reset", Notes 1, 2 and 3**.

10.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator that does not require any external components. This RC oscillator is separate from the external RC oscillator of the (GP5/RB5)/OSC1/CLKIN pin and the internal 4/8 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset generates a device Reset.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see **Section 10.1 "Configuration Bits"**). Refer to the PIC12F510/16F506 Programming Specifications to determine how to access the Configuration Word.

TABLE 10-6: TYPICAL DRT PERIODS

Oscillator Configuration	POR Reset	Subsequent Resets
LP	18 ms	18 ms
XT	18 ms	18 ms
HS(1)	18 ms	18 ms
EC(1)	1.125 ms	10 µs
INTOSC	1.125 ms	10 µs
EXTRC	1.125 ms	10 µs

Note 1: PIC16F506 only

Note:	It is the responsibility of the application designer to ensure the use of the 1.125 ms nominal DRT will result in acceptable operation. Refer to Electrical Specifications for VDD rise time and stability requirements for this mode of operation.

10.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a divisor ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

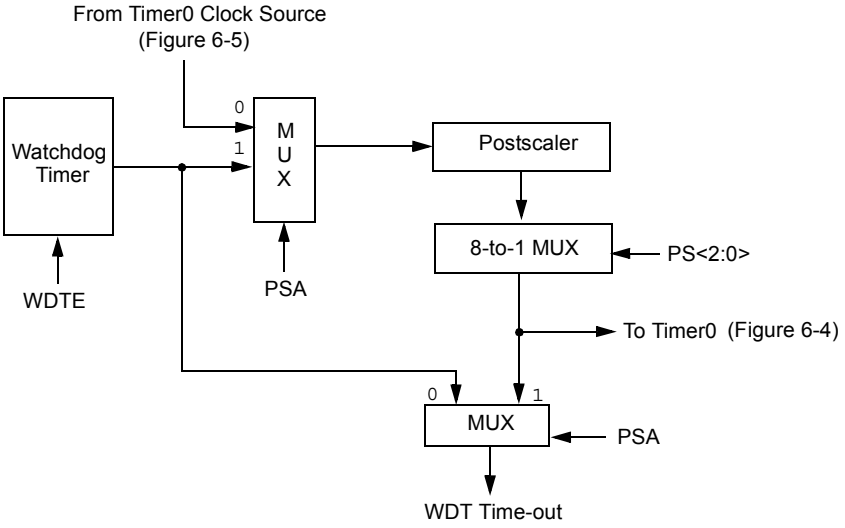
Under worst-case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

10.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

FIGURE 10-11: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

TABLE 10-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	OPTION(1)	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION(2)	$\overline{RBWU}$	$\overline{RBPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded boxes = Not used by Watchdog Timer. – = unimplemented, read as '0', u = unchanged.

Note 1: PIC12F510 only.

2: PIC16F506 only.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(W).OR. (f) → (dest)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(f) → (dest)
Status Affected:	Z
Description:	The contents of register 'f' are moved to destination 'd'. If 'd' is '0', destination is the W register. If 'd' is '1', the destination is file register 'f'. 'd' = 1 is useful as a test of a file register, since Status flag Z is affected.

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W)
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into the W register. The "don't cares" will be assembled as '0's.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	0 ≤ f ≤ 31
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from the W register to register 'f'.

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

OPTION	Load OPTION Register
Syntax:	[*label*] Option
Operands:	None
Operation:	(W) → Option
Status Affected:	None
Description:	The content of the W register is loaded into the OPTION register.

FIGURE 13-3: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C (PIC16F506)

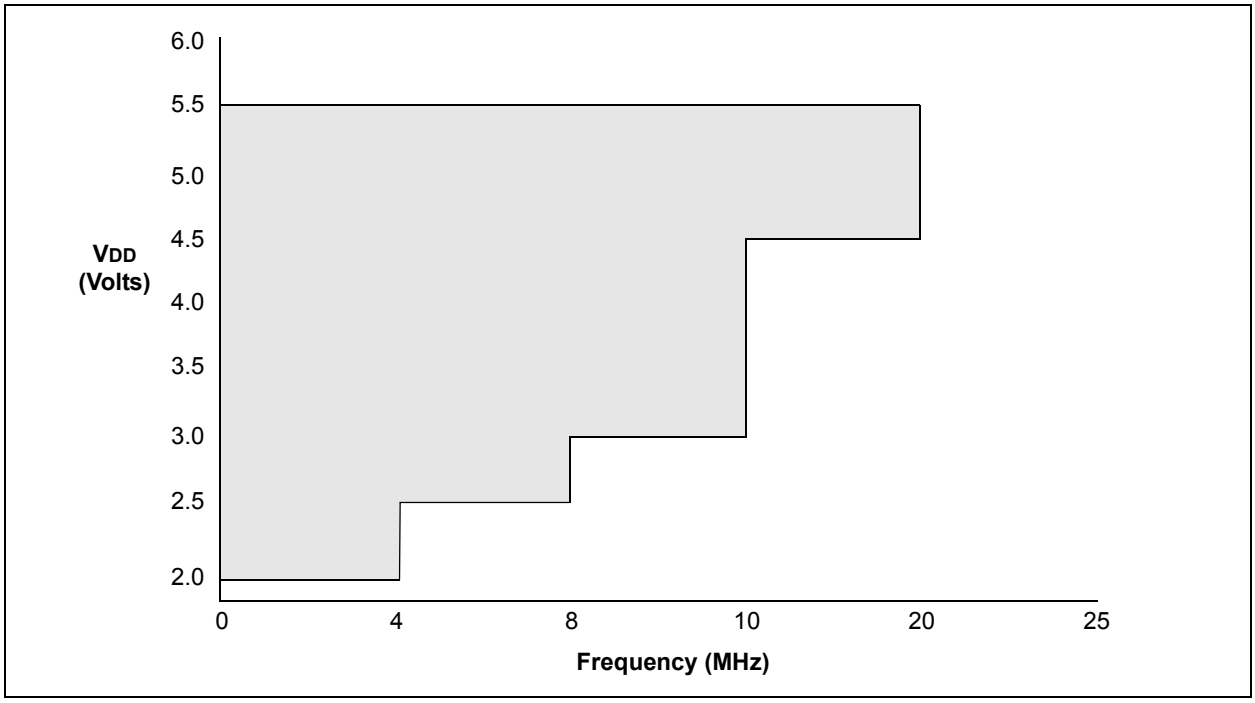


FIGURE 13-4: MAXIMUM OSCILLATOR FREQUENCY TABLE (PIC16F506)

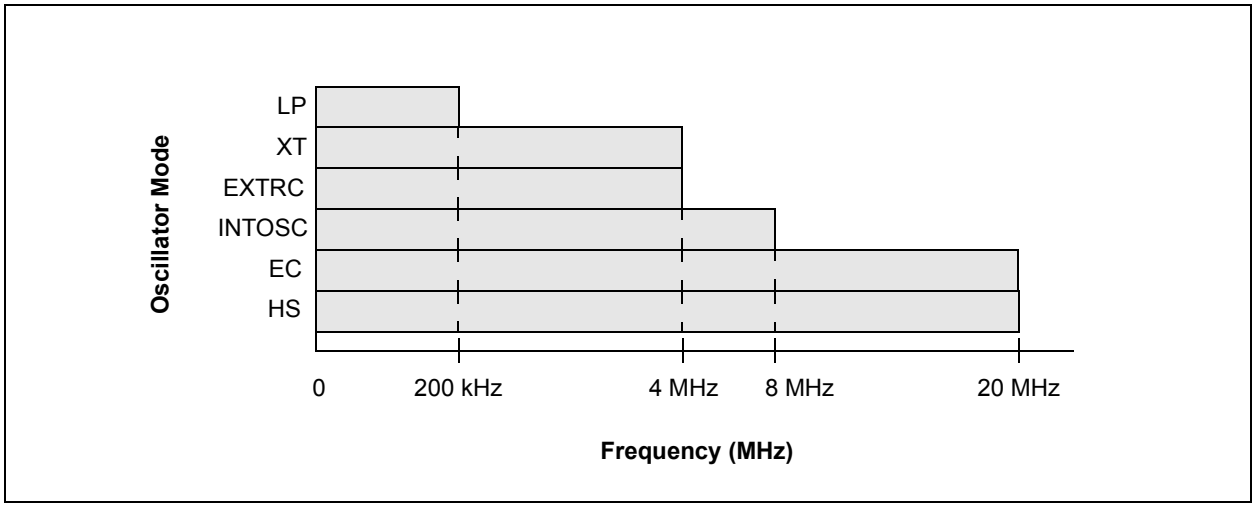


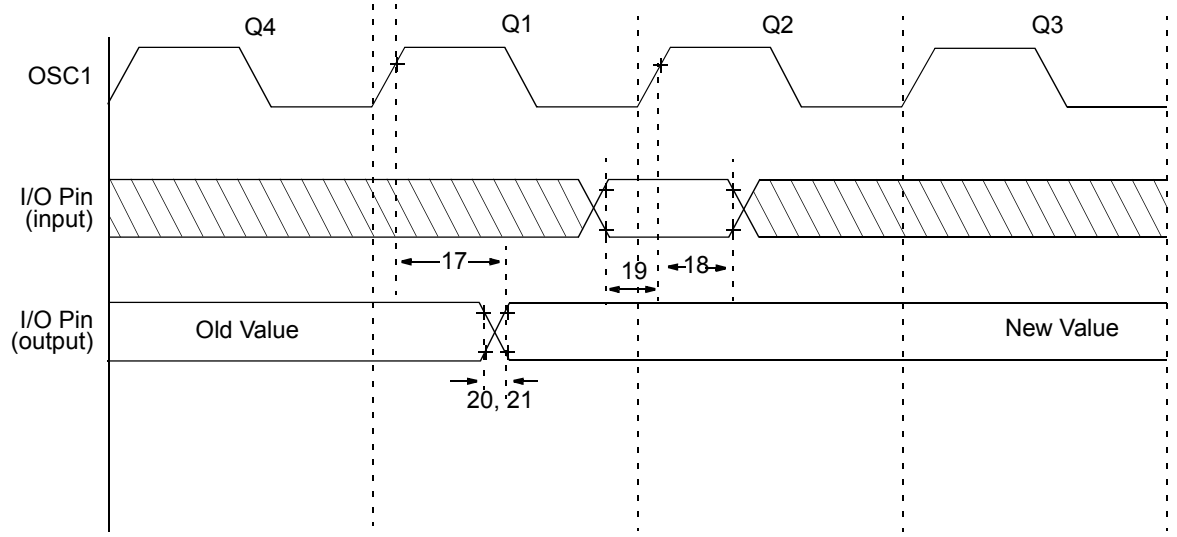
TABLE 13-5: CALIBRATED INTERNAL RC FREQUENCIES

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial), -40°C ≤ TA ≤ +125°C (extended)					
Param No.	**Sym**	**Characteristic**	**Freq. Tolerance**	**Min**	**Typ(1)**	**Max***	**Units**	**Conditions**
F10	FOSC	Internal Calibrated INTOSC Frequency(1)	±1% ±2% ±5%	7.92 7.84 7.60	8.00 8.00 8.00	8.08 8.16 8.40	MHz MHz MHz	VDD = 3.5V TA = 25°C 2.5V ≤ VDD ≤ 5.5V 0°C ≤ TA ≤ +85°C 2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (Ind.) -40°C ≤ TA ≤ +125°C (Ext.)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-7: I/O TIMING



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

FIGURE 14-4: COMPARATOR IPD vs. VDD (COMPARATOR ENABLED)

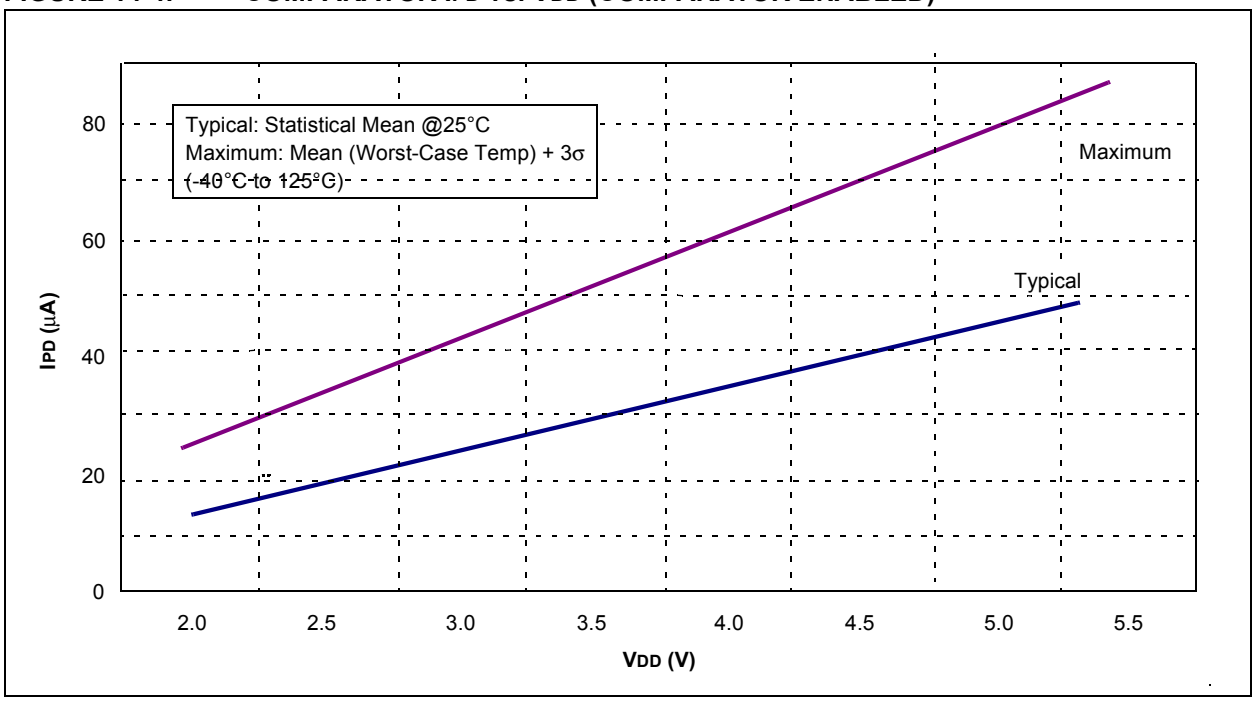
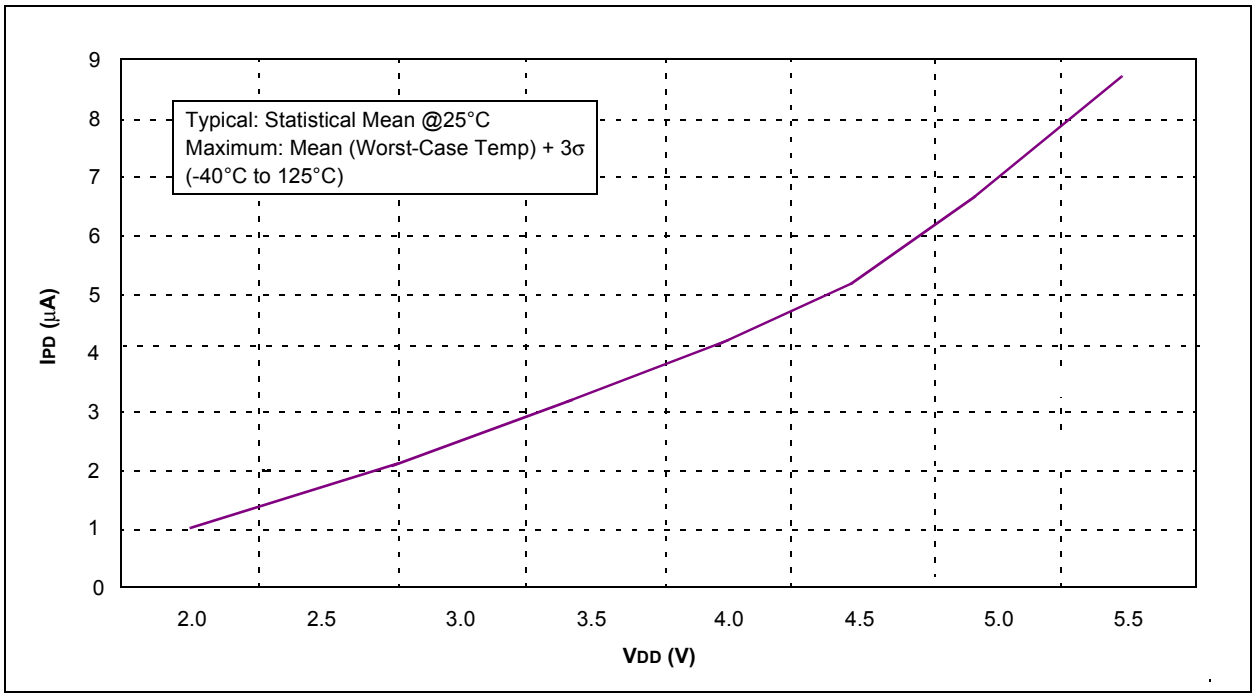
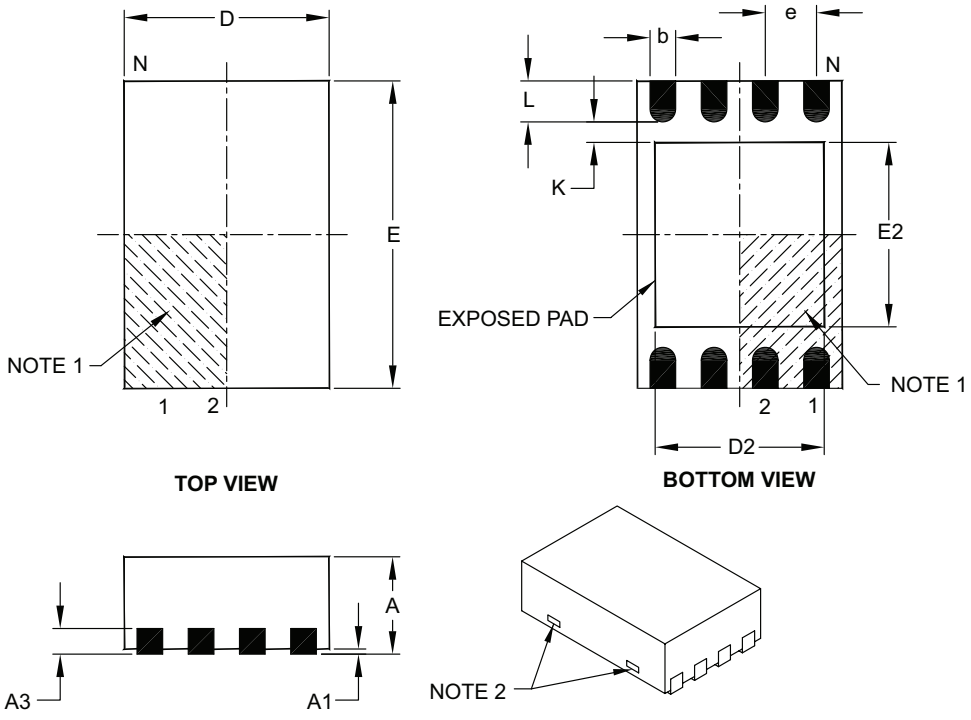


FIGURE 14-5: TYPICAL WDT IPD vs. VDD



8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.75
Exposed Pad Width	E2	1.50	–	1.90
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123B