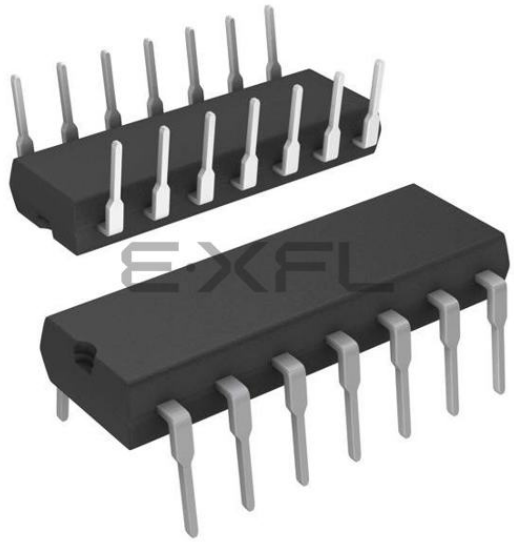

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	67 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f506-e-p

Table of Contents

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NOTES:

2.0 PIC12F510/16F506 DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC12F510/16F506 Product Identification System at the back of this data sheet to specify the correct part number.

2.1 Quick Turn Programming (QTP) Devices

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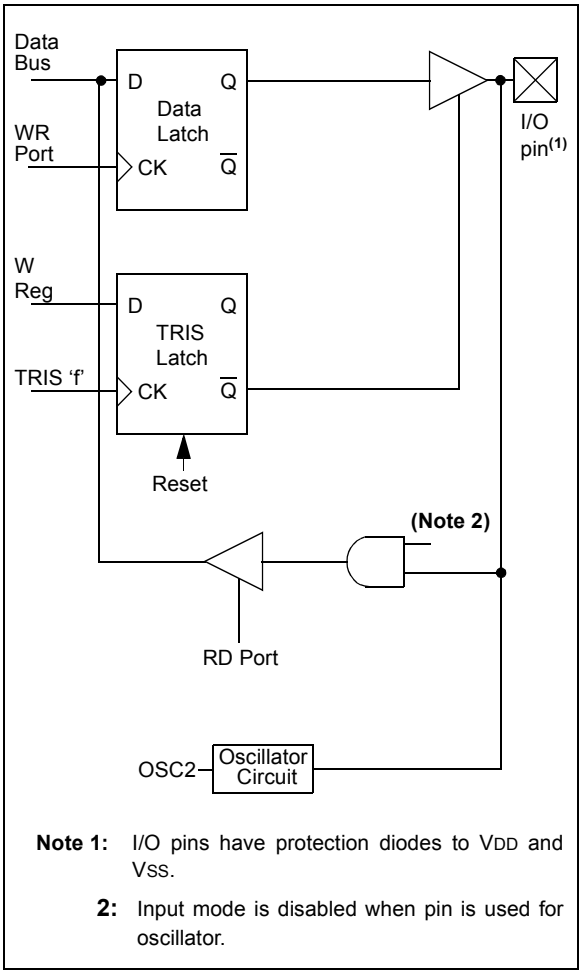
NOTES:

TABLE 3-2: PIN DESCRIPTIONS – PIC12F510

Name	I/O/P Type	Input Type	Output Type	Description
GP0/AN0/C1IN+/ICSPDAT	GP0	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	AN0	AN	—	ADC channel input.
	C1IN+	AN	—	Comparator input.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming data pin.
GP1/AN1/C1IN-/ICSPCLK	GP1	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	AN1	AN	—	ADC channel input.
	C1IN-	AN	—	Comparator input.
	ICSPCLK	ST	—	In-Circuit Serial Programming clock pin.
GP2/AN2/T0CKI/C1OUT	GP2	TTL	CMOS	Bidirectional I/O port.
	AN2	AN	—	ADC channel input.
	T0CKI	ST	—	Timer0 clock input.
	C1OUT	—	CMOS	Comparator output.
GP3/$\overline{\text{MCLR}}$/V_{PP}	GP3	TTL	—	Standard TTL input. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	$\overline{\text{MCLR}}$ input – weak pull-up always enabled in this mode.
	V_{PP}	HV	—	Programming Voltage input.
GP4/OSC2	GP4	TTL	CMOS	Bidirectional I/O port.
	OSC2	—	XTAL	XTAL oscillator output pin.
GP5/OSC1/CLKIN	GP5	TTL	CMOS	Bidirectional I/O port.
	OSC1	XTAL	—	XTAL oscillator input pin.
	CLKIN	ST	—	EXTRC Schmitt Trigger input.
V_{DD}	V_{DD}	P	—	Positive supply for logic and I/O pins.
V_{SS}	V_{SS}	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog Voltage, HV = High Voltage

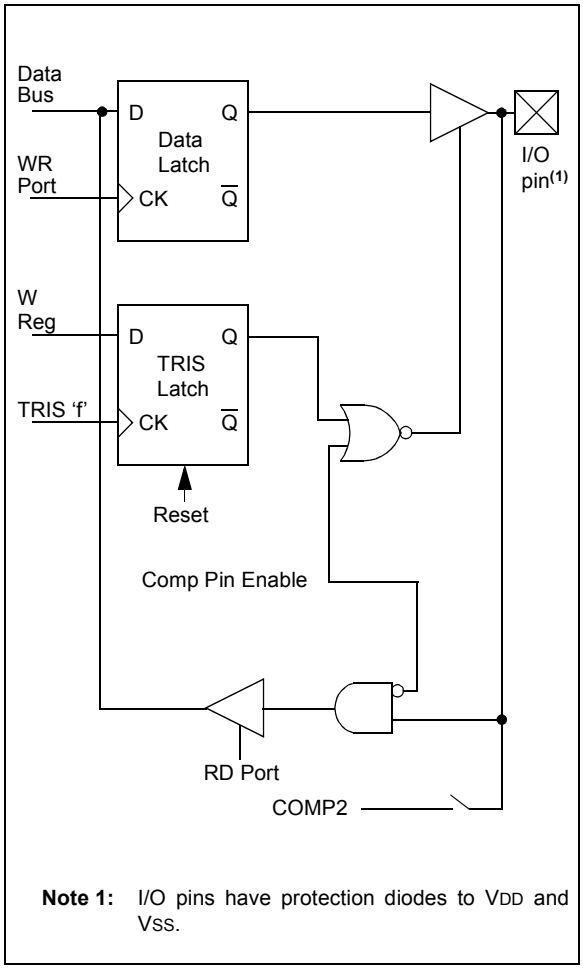
FIGURE 5-8: BLOCK DIAGRAM OF RB5/GP5



Note 1: I/O pins have protection diodes to VDD and VSS.

2: Input mode is disabled when pin is used for oscillator.

FIGURE 5-9: BLOCK DIAGRAM OF RC0/RC1



Note 1: I/O pins have protection diodes to VDD and VSS.

6.0 TMR0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock
  - External clock from either the T0CKI pin or from the output of the comparator

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

There are two types of Counter mode. The first Counter mode uses the T0CKI pin to increment Timer0. It is selected by setting the T0CKI bit (OPTION<5>), setting the $\overline{\text{C1T0CS}}$ bit (CM1CON0<4>) and setting the $\overline{\text{C1OUTEN}}$ bit (CM1CON0<6>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 6.1 "Using Timer0 With An External Clock"**.

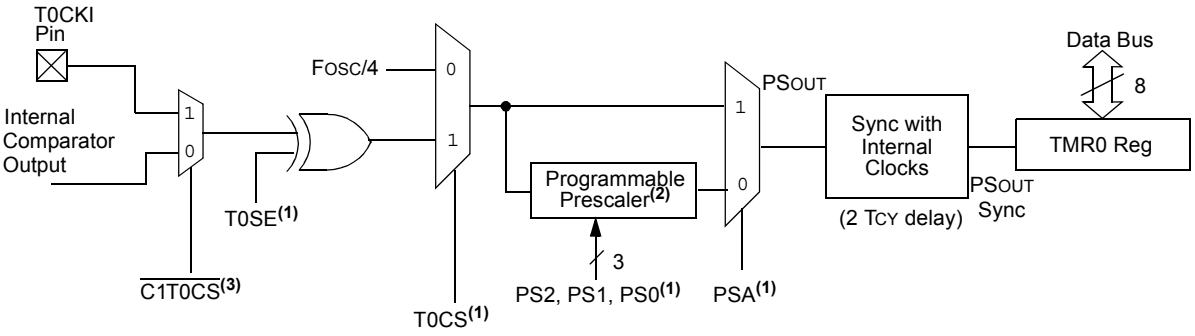
The second Counter mode uses the output of the comparator to increment Timer0. It can be entered in two different ways. The first way is selected by setting the T0CS bit (OPTION<5>), and clearing the $\overline{\text{C1T0CS}}$ bit (CM1CON0<4>) ($\overline{\text{C1OUTEN}}$ [CM1CON0<6>] does not affect this mode of operation). This enables an internal connection between the comparator and the Timer0.

The second way is selected by setting the T0CS bit (OPTION<5>), setting the $\overline{\text{C1T0CS}}$ bit (CM1CON0) and clearing the $\overline{\text{C1OUTEN}}$ bit (CM1CON0<6>). This allows the output of the comparator onto the T0CKI pin, while keeping the T0CKI input active. Therefore, any comparator change on the COUT pin is fed back into the T0CKI input. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input as discussed in **Section 6.1 "Using Timer0 With An External Clock"**.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. **Section 6.2 "Prescaler"** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-5).
3: Bit $\overline{\text{C1T0CS}}$ is located in the CM1CON0 register, CM1CON0<4>.

FIGURE 7-4: ANALOG INPUT MODE

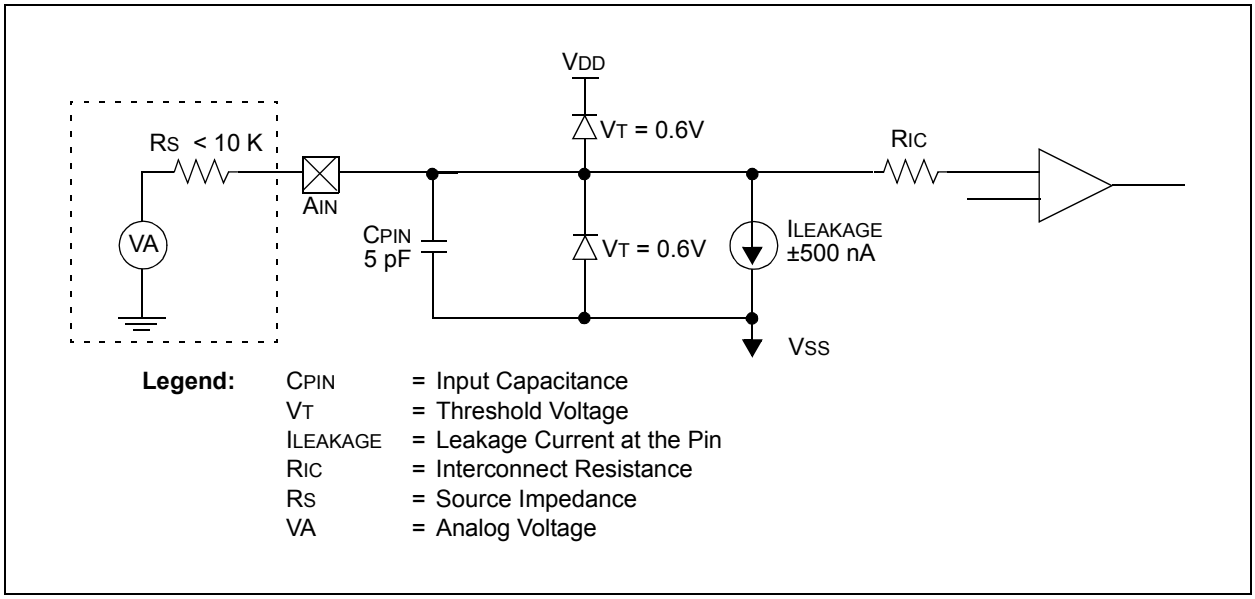


TABLE 7-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Add	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other Resets
03h	STATUS	GPWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	qq0q quuu
07h	CM1CON0(1)	C1OUT	$\overline{C1OUTEN}$	C1POL	$\overline{C1T0CS}$	C1ON	C1NREF	C1PREF	$\overline{C1WU}$	1111 1111	uuuu uuuu
08h	CM1CON0(2)	C1OUT	$\overline{C1OUTEN}$	C1POL	$\overline{C1T0CS}$	C1ON	C1NREF	C1PREF	$\overline{C1WU}$	1111 1111	uuuu uuuu
0Bh	CM2CON0(2)	C2OUT	$\overline{C2OUTEN}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{C2WU}$	1111 1111	uuuu uuuu
N/A	TRISB(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISC(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISGPIO(1)	—	—	I/O Control Register						--11 1111	--11 1111

Legend: x = Unknown, u = Unchanged, – = Unimplemented, read as '0', q = Depends on condition.
Note 1: PIC12F510 only.
2: PIC16F506 only.

FIGURE 8-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

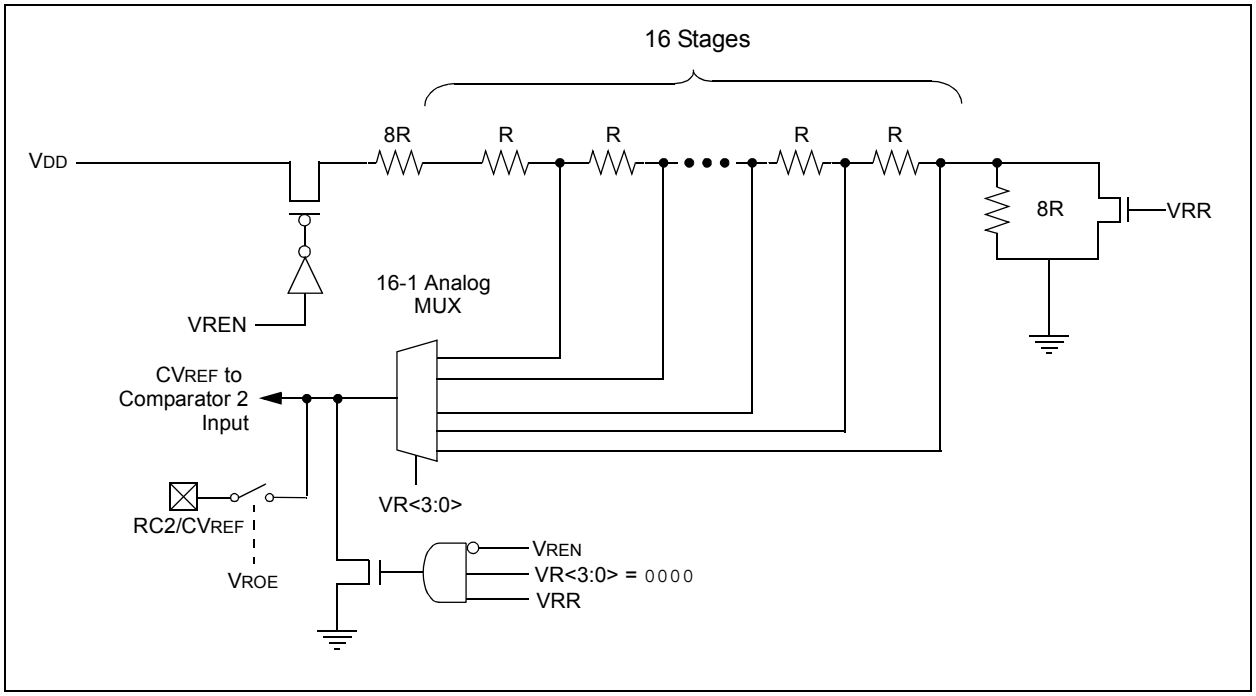


TABLE 8-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Add	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
0Ch	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	001- 1111	001- 1111
08h	CM1CON0(1)	C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$	1111 1111	uuuu uuuu
0Bh	CM2CON0(1)	C2OUT	$\overline{\text{C2OUTEN}}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{\text{C2WU}}$	1111 1111	uuuu uuuu

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'.
Note 1: PIC16F506 only.

9.0 ANALOG-TO-DIGITAL (A/D) CONVERTER

The A/D Converter allows conversion of an analog signal into an 8-bit digital signal.

9.1 Clock Divisors

The ADC has 4 clock source settings ADCS<1:0>. There are 3 divisor values 16, 8 and 4. The fourth setting is INTOSC with a divisor of 4. These settings will allow a proper conversion when using an external oscillator at speeds from 20 MHz to 350 kHz. Using an external oscillator at a frequency below 350 kHz (TAD > 50 μs) requires the ADC oscillator setting to be INTOSC/4 for valid ADC results.

The ADC requires 13 TAD periods to complete a conversion. The divisor values do not affect the number of TAD periods required to perform a conversion. The divisor values determine the length of the TAD period.

When the ADCS<1:0> bits are changed while an ADC conversion is in process, the new ADC clock source will not be selected until the next conversion is started. This clock source selection will be lost when the device enters Sleep.

9.1.1 VOLTAGE REFERENCE

There is no external voltage reference for the ADC. The ADC reference voltage will always be VDD.

9.1.2 ANALOG MODE SELECTION

The ANS<1:0> bits are used to configure pins for analog input. Upon any Reset, ANS<1:0> defaults to 11. This configures pins AN0, AN1 and AN2 as analog inputs. Pins configured as analog inputs are not available for digital output. Users should not change the ANS bits while a conversion is in process. ANS bits are active regardless of the condition of ADON.

9.1.3 ADC CHANNEL SELECTION

The CHS bits are used to select the analog channel to be sampled by the ADC. The CHS<1:0> bits can be changed at any time without adversely effecting a conversion. To acquire an analog signal the CHS<1:0> selection must match one of the pin(s) selected by the ANS<1:0> bits. When the ADC is on (ADON = 1) and a channel is selected that is also being used by the comparator, then both the comparator and the ADC will see the analog voltage on the pin.

Note:	It is the users responsibility to ensure that use of the ADC and comparator simultaneously on the same pin, does not adversely affect the signal being monitored or adversely effect device operation.

When the CHS<1:0> bits are changed during an ADC conversion, the new channel will not be selected until the current conversion is completed. This allows the current conversion to complete with valid results. All channel selection information will be lost when the device enters Sleep.

TABLE 9-1: CHANNEL SELECT (ADCS) BITS AFTER AN EVENT

Event	ADCS<1:0>
$\overline{\text{MCLR}}$	11
Conversion completed	CS<1:0>
Conversion terminated	CS<1:0>
Power-on	11
Wake from Sleep	11

9.1.4 THE GO/$\overline{\text{DONE}}$ BIT

The GO/$\overline{\text{DONE}}$ bit is used to determine the status of a conversion, to start a conversion and to manually halt a conversion in process. Setting the GO/$\overline{\text{DONE}}$ bit starts a conversion. When the conversion is complete, the ADC module clears the GO/$\overline{\text{DONE}}$ bit. A conversion can be terminated by manually clearing the GO/$\overline{\text{DONE}}$ bit while a conversion is in process. Manual termination of a conversion may result in a partially converted result in ADRES.

The GO/$\overline{\text{DONE}}$ bit is cleared when the device enters Sleep, stopping the current conversion. The ADC does not have a dedicated oscillator, it runs off of the instruction clock. Therefore, no conversion can occur in sleep.

The GO/$\overline{\text{DONE}}$ bit cannot be set when ADON is clear.

9.1.5 SLEEP

This ADC does not have a dedicated ADC clock, and therefore, no conversion in Sleep is possible. If a conversion is underway and a Sleep command is executed, the GO/$\overline{\text{DONE}}$ and ADON bit will be cleared. This will stop any conversion in process and power-down the ADC module to conserve power. Due to the nature of the conversion process, the ADRES may contain a partial conversion. At least 1 bit must have been converted prior to Sleep to have partial conversion data in ADRES. The ADCS and CHS bits are reset to their default condition; ANS<1:0> = 11 and CHS<1:0> = 11.

- For accurate conversions, TAD must meet the following:
- 500 ns < TAD < 50 µs
- TAD = 1/(FOSC/divisor)

Shaded areas indicate TAD out of range for accurate conversions. If analog input is desired at these frequencies, use INTOSC/4 for the ADC clock source.

TABLE 9-2: TAD FOR ADCS SETTINGS WITH VARIOUS OSCILLATORS

Source	ADCS <1:0>	Divisor	20(1) MHz	16(1) MHz	8 MHz	4 MHz	1 MHz	500 kHz	350 kHz	200 kHz	100 kHz	32 kHz
INTOSC	11	4	—	—	.5 µs	1 µs	—	—	—	—	—	—
FOSC	10	4	.2 µs	.25 µs	.5 µs	1 µs	4 µs	8 µs	11 µs	20 µs	40 µs	125 µs
FOSC	01	8	.4 µs	.5 µs	1 µs	2 µs	8 µs	16 µs	23 µs	40 µs	80 µs	250 µs
FOSC	00	16	.8 µs	1 µs	2 µs	4 µs	16 µs	32 µs	46 µs	80 µs	160 µs	500 µs

Note 1: When operating with external oscillator frequencies of 16 MHz or higher, better ADC performance will result from selection of a suitable FOSC divisor value from Table 9-2 than from use of the INTOSC/4 option for the ADC clock.

TABLE 9-3: EFFECTS OF SLEEP ON ADCON0

	ANS1	ANS0	ADCS1	ADCS0	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
Entering Sleep	Unchanged	Unchanged	1	1	1	1	0	0
Wake or Reset	1	1	1	1	1	1	0	0

9.1.6 ANALOG CONVERSION RESULT REGISTER

The ADRES register contains the results of the last conversion. These results are present during the sampling period of the next analog conversion process. After the sampling period is over, ADRES is cleared (= 0). A 'leading one' is then right shifted into the ADRES to serve as an internal conversion complete bit. As each bit weight, starting with the MSB, is converted, the leading one is shifted right and the converted bit is stuffed into ADRES. After a total of 9 right shifts of the 'leading one' have taken place, the conversion is complete; the 'leading one' has been shifted out and the GO/$\overline{\text{DONE}}$ bit is cleared.

If the GO/$\overline{\text{DONE}}$ bit is cleared in software during a conversion, the conversion stops. The data in ADRES is the partial conversion result. This data is valid for the bit weights that have been converted. The position of the 'leading one' determines the number of bits that have been converted. The bits that were not converted before the GO/$\overline{\text{DONE}}$ was cleared are unrecoverable.

REGISTER 9-1: ADCON0: A/D CONTROL REGISTER (PIC12F510)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
ANS1	ANS0	ADCS1	ADCS0	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **ANS<1:0>:** ADC Analog Input Pin Select bits[1), (2)]
- 00 = No pins configured for analog input
- 01 = AN2 configured as an analog input
- 10 = AN2 and AN0 configured as analog inputs
- 11 = AN2, AN1 and AN0 configured as analog inputs

bit 5-4 **ADCS<1:0>:** ADC Conversion Clock Select bits
- 00 = FOSC/16
- 01 = FOSC/8
- 10 = FOSC/4
- 11 = INTOSC/4

bit 3-2 **CHS<1:0>:** ADC Channel Select bits
- 00 = Channel AN0
- 01 = Channel AN1
- 10 = Channel AN2
- 11 = 0.6V absolute voltage reference

bit 1 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit[(4)]
- 1 = ADC conversion in progress. Setting this bit starts an ADC conversion cycle. This bit is automatically cleared by hardware when the ADC is done converting.
- 0 = ADC conversion completed/not in progress. Manually clearing this bit while a conversion is in process terminates the current conversion.

bit 0 **ADON:** ADC Enable bit
- 1 = ADC module is operating
- 0 = ADC module is shut-off and consumes no power

Note 1: When the ANS bits are set, the channels selected will automatically be forced into Analog mode, regardless of the pin function previously defined. The only exception to this is the comparator, where the analog input to the comparator and the ADC will be active at the same time. It is the users responsibility to ensure that the ADC loading on the comparator input does not affect their application.

2: The ANS<1:0> bits are active regardless of the condition of ADON.

3: CHS<1:0> bits default to 11 after any Reset.

4: If the ADON bit is clear, the GO/$\overline{\text{DONE}}$ bit cannot be set.

REGISTER 10-2: CONFIG: CONFIGURATION WORD REGISTER (PIC16F506)(1)

—	—	—	—	—	—	—	—
bit 15							bit 8

—	IOSCFS	MCLRE	$\overline{CP}$	WDTE	FOSC2	FOSC1	FOSC0
bit 7							bit 0

bit 11-7 **Unimplemented**: Read as '1'

bit 6 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz INTOSC speed
0 = 4 MHz INTOSC speed

bit 5 **MCLRE:** Master Clear Enable bit
1 = RB3/$\overline{MCLR}$ pin functions as $\overline{MCLR}$
0 = RB3/$\overline{MCLR}$ pin functions as RB3, $\overline{MCLR}$ tied internally to V_{DD}

bit 4 **$\overline{CP}$:** Code Protection bit
1 = Code protection off
0 = Code protection on

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
000 = LP oscillator and 18 ms DRT
001 = XT oscillator and 18 ms DRT
010 = HS oscillator and 18 ms DRT
011 = EC oscillator with RB4 function on RB4/OSC2/CLKOUT and 1.125 ms DRT(2)
100 = INTOSC with RB4 function on RB4/OSC2/CLKOUT and 1.125 ms DRT(2)
101 = INTOSC with CLKOUT function on RB4/OSC2/CLKOUT and 1.125 ms DRT(2)
110 = EXTRC with RB4 function on RB4/OSC2/CLKOUT and 1.125 ms DRT (2)
111 = EXTRC with CLKOUT function on RB4/OSC2/CLKOUT and 1.125 ms DRT(2)

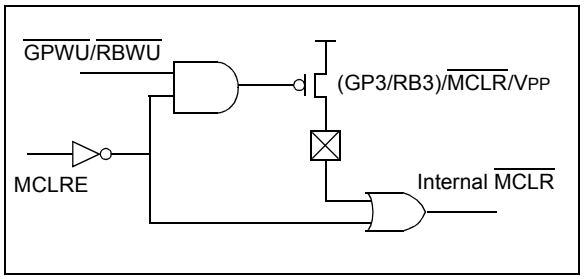
Note 1: Refer to the "*PIC16F506 Memory Programming Specification*" (DS41258) to determine how to access the Configuration Word.

2: It is the responsibility of the application designer to ensure the use of the 1.125 ms (nominal) DRT will result in acceptable operation. Refer to Electrical Specifications for V_{DD} rise time and stability requirements for this mode of operation.

10.3.1 MCLR ENABLE

This Configuration bit, when unprogrammed (left in the '1' state), enables the external MCLR function. When programmed, the MCLR function is tied to the internal VDD and the pin is assigned to be a I/O. See Figure 10-6.

FIGURE 10-6: MCLR SELECT



10.4 Power-on Reset (POR)

The PIC12F510/16F506 devices incorporate an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. The POR is active regardless of the state of the MCLR enable bit. An internal weak pull-up resistor is implemented using a transistor (refer to Table 13-3 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create an external Power-on Reset. A maximum rise time for VDD is specified. See **Section 13.0 "Electrical Characteristics"** for details.

When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the devices must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 10-7.

The Power-on Reset circuit and the Device Reset Timer (see **Section 10.5 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects MCLR, internal or external, to be high. After the time-out period, it will reset the Reset latch and thus end the on-chip Reset signal.

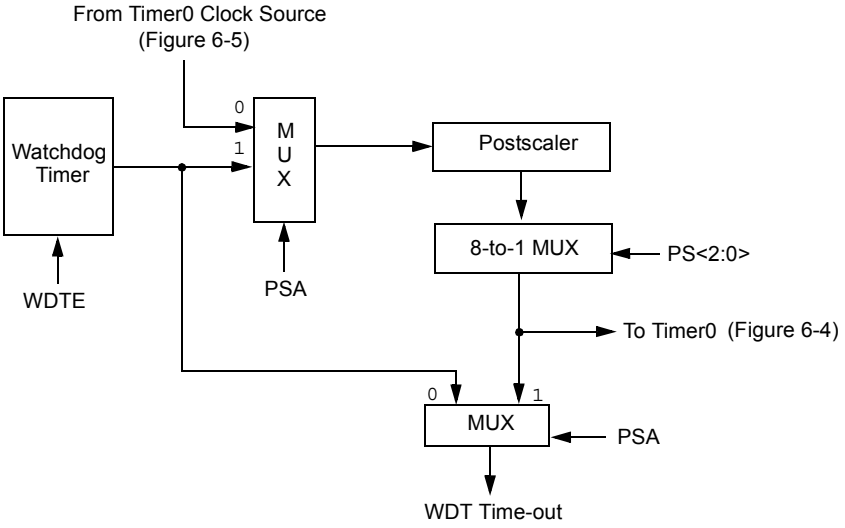
A power-up example where MCLR is held low is shown in Figure 10-8. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of Reset TDRT msec after MCLR goes high.

In Figure 10-9, the on-chip Power-on Reset feature is being used (MCLR and VDD are tied together or the pin is programmed to be (GP3/RB3). The VDD is stable before the Start-up timer times out and there is no problem in getting a proper Reset. However, Figure 10-10 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that MCLR is high and when MCLR and VDD actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 10-9).

Note:	When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Notes AN522, *"Power-Up Considerations"* (DS00522) and AN607, *"Power-up Trouble Shooting"* (DS00607).

FIGURE 10-11: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

TABLE 10-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	OPTION(1)	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION(2)	$\overline{RBWU}$	$\overline{RBPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded boxes = Not used by Watchdog Timer. – = unimplemented, read as '0', u = unchanged.

Note 1: PIC12F510 only.

2: PIC16F506 only.

11.0 INSTRUCTION SET SUMMARY

The PIC16 instruction set is highly orthogonal and is comprised of three basic categories.

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 12-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 11-1, while the various opcode fields are summarized in Table 11-1.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bits affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 11-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top-of-Stack
PC	Program Counter
WDT	Watchdog Timer counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

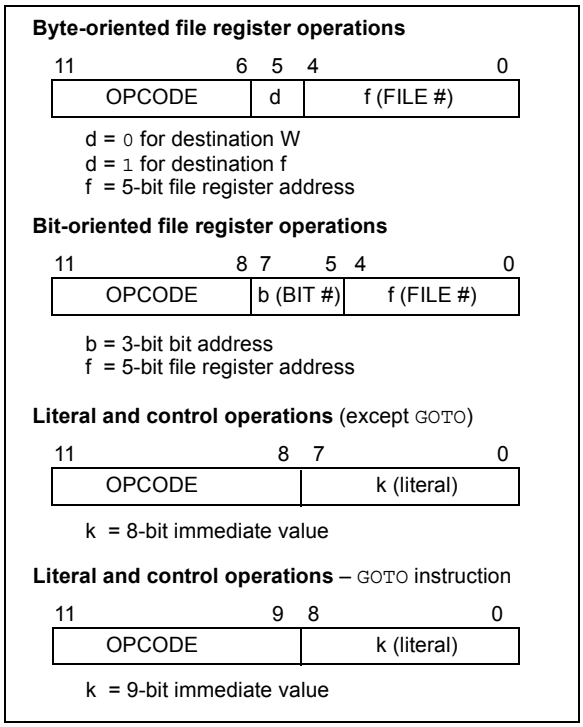
All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Figure 11-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 11-1: GENERAL FORMAT FOR INSTRUCTIONS



TRIS	Load TRIS Register
Syntax:	[*label*] TRIS f
Operands:	f = 6
Operation:	(W) → TRIS register f
Status Affected:	None
Description:	TRIS register 'f' (f = 6 or 7) is loaded with the contents of the W register

XORLW	Exclusive OR literal with W
Syntax:	[*label*] XORLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF	Exclusive OR W with f
Syntax:	[*label*] XORWF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(W) .XOR. (f) → (dest)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

14.0 DC AND CHARACTERISTICS GRAPHS AND CHARTS.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where s is a standard deviation, over each temperature range.

FIGURE 14-1: IDD vs. VDD OVER FOSC

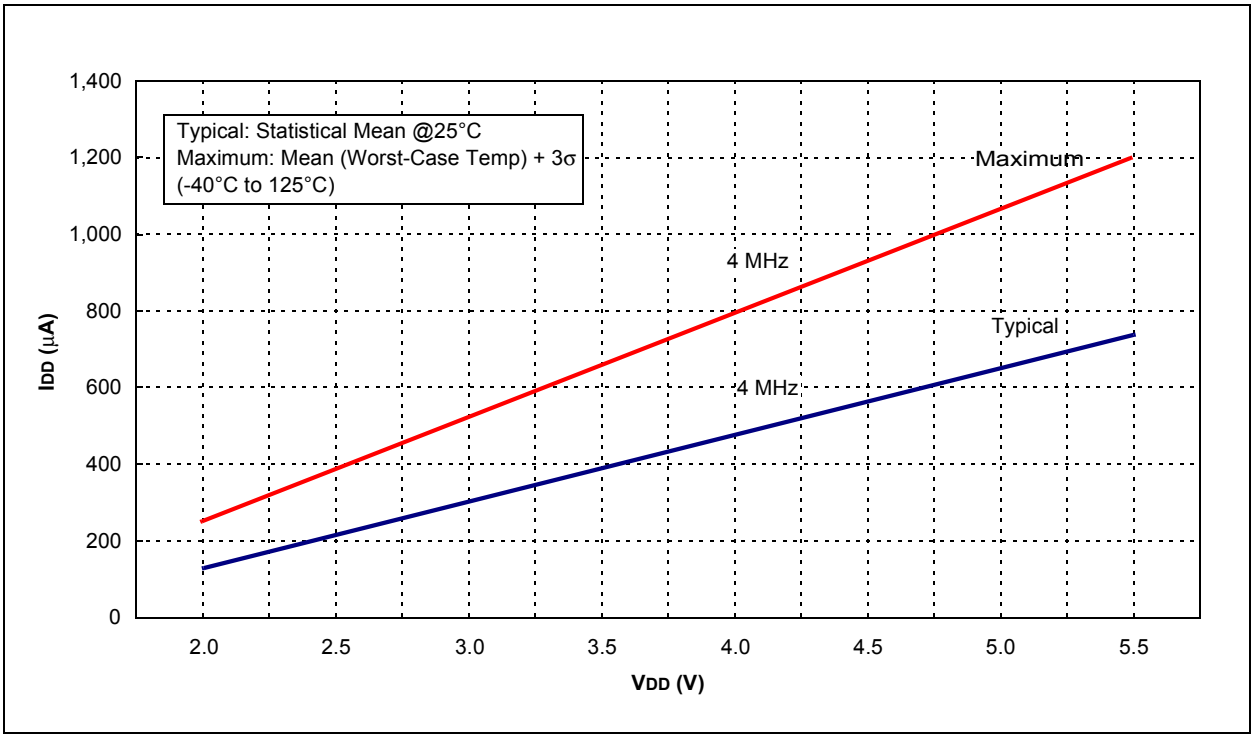


FIGURE 14-8: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

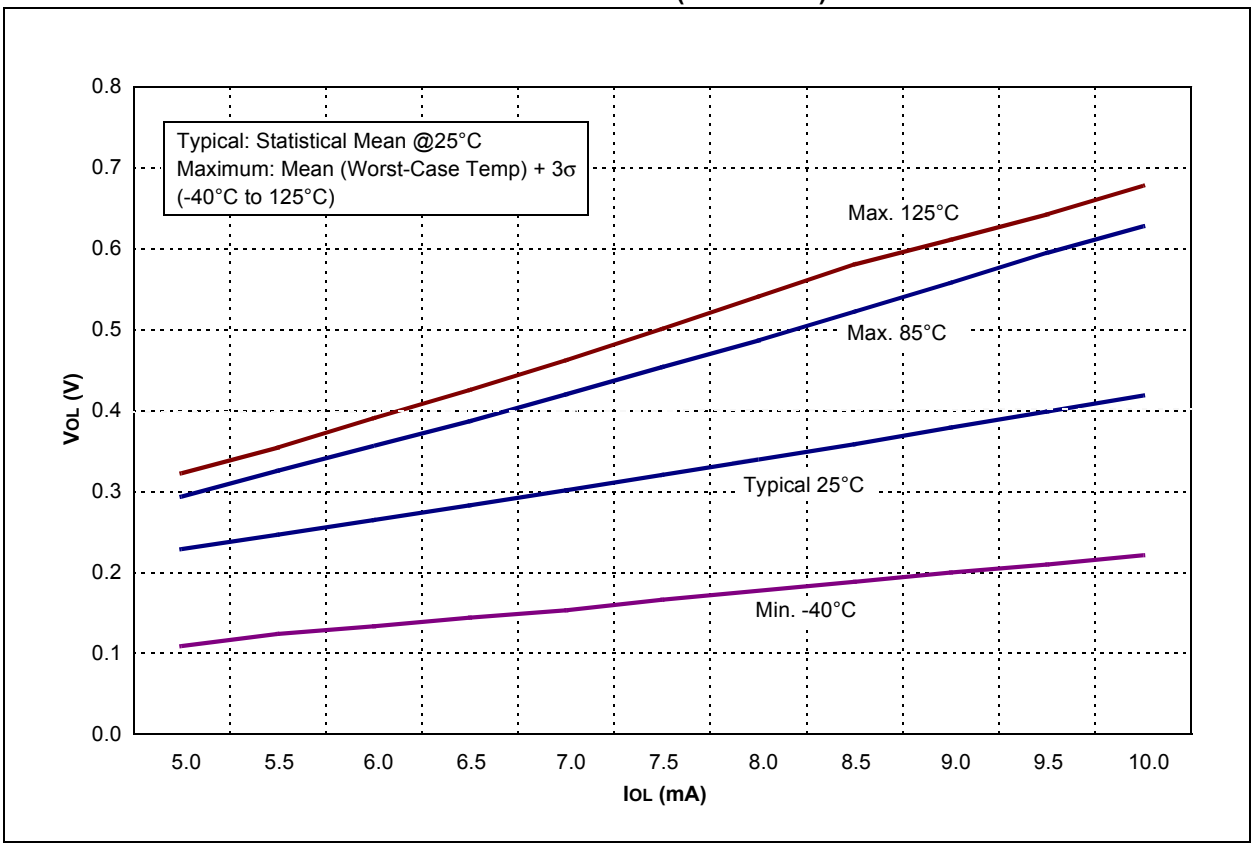
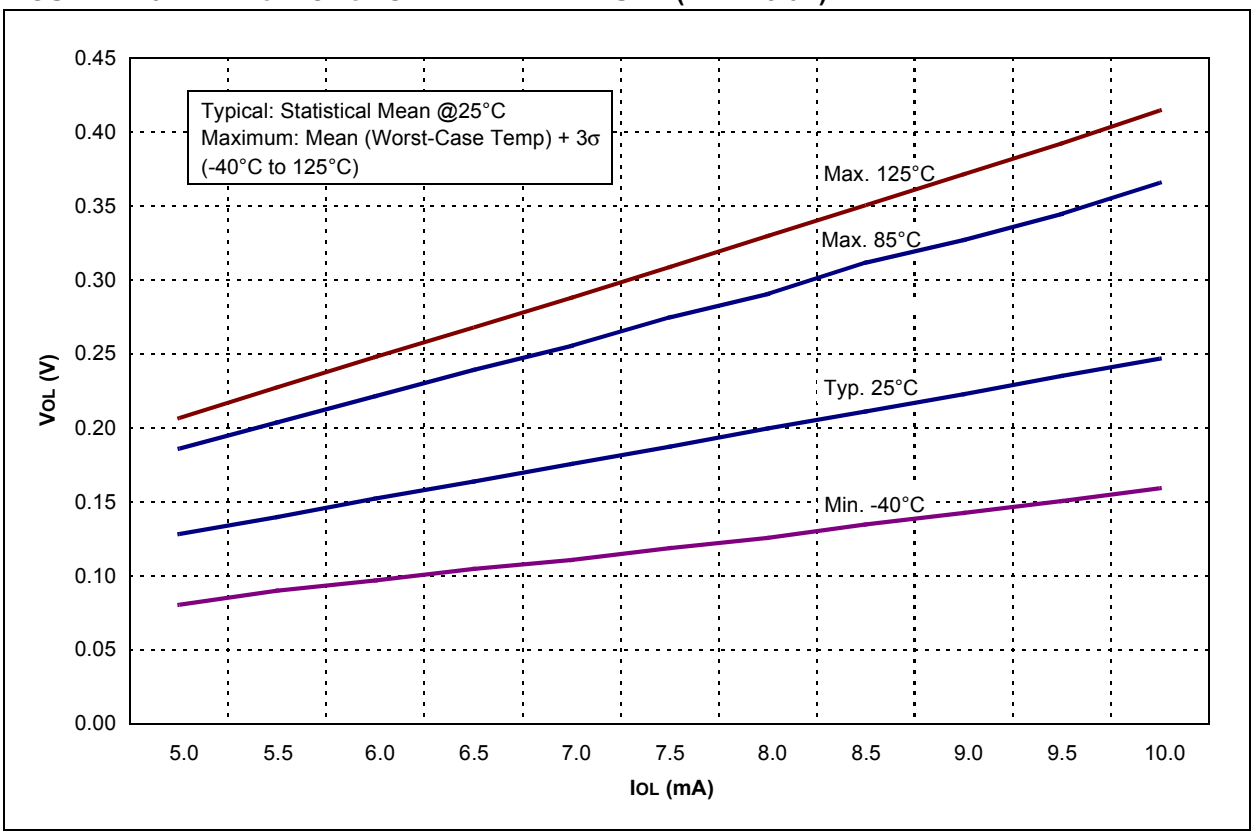
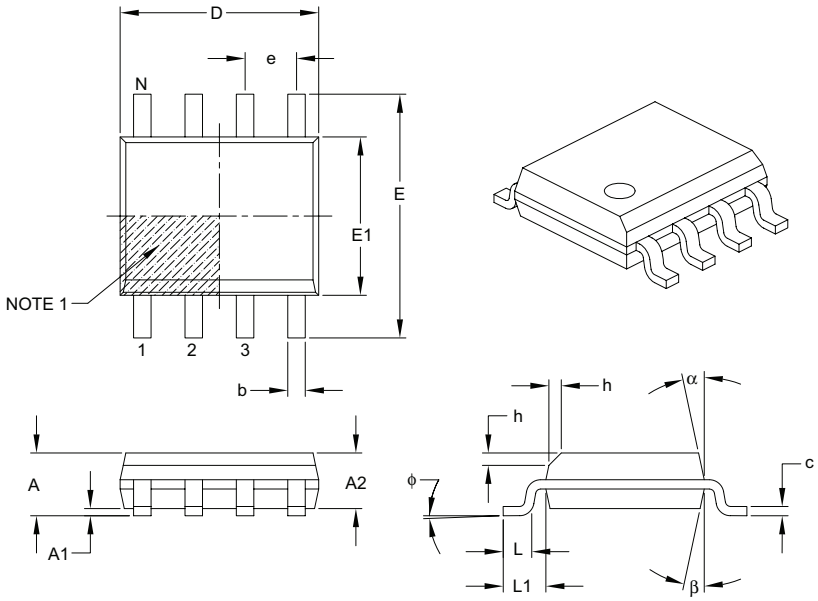


FIGURE 14-9: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)



8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B