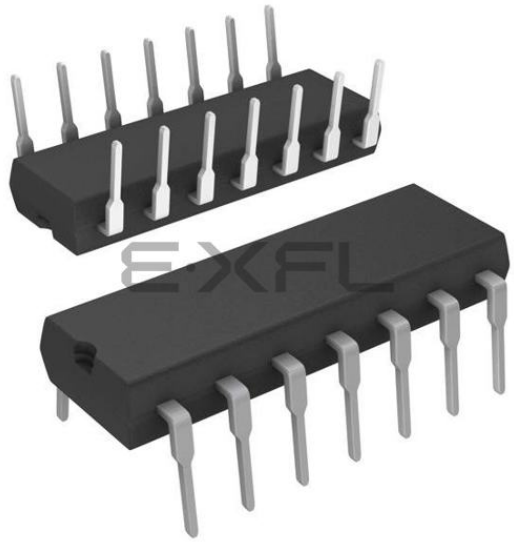

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	67 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f506-i-p

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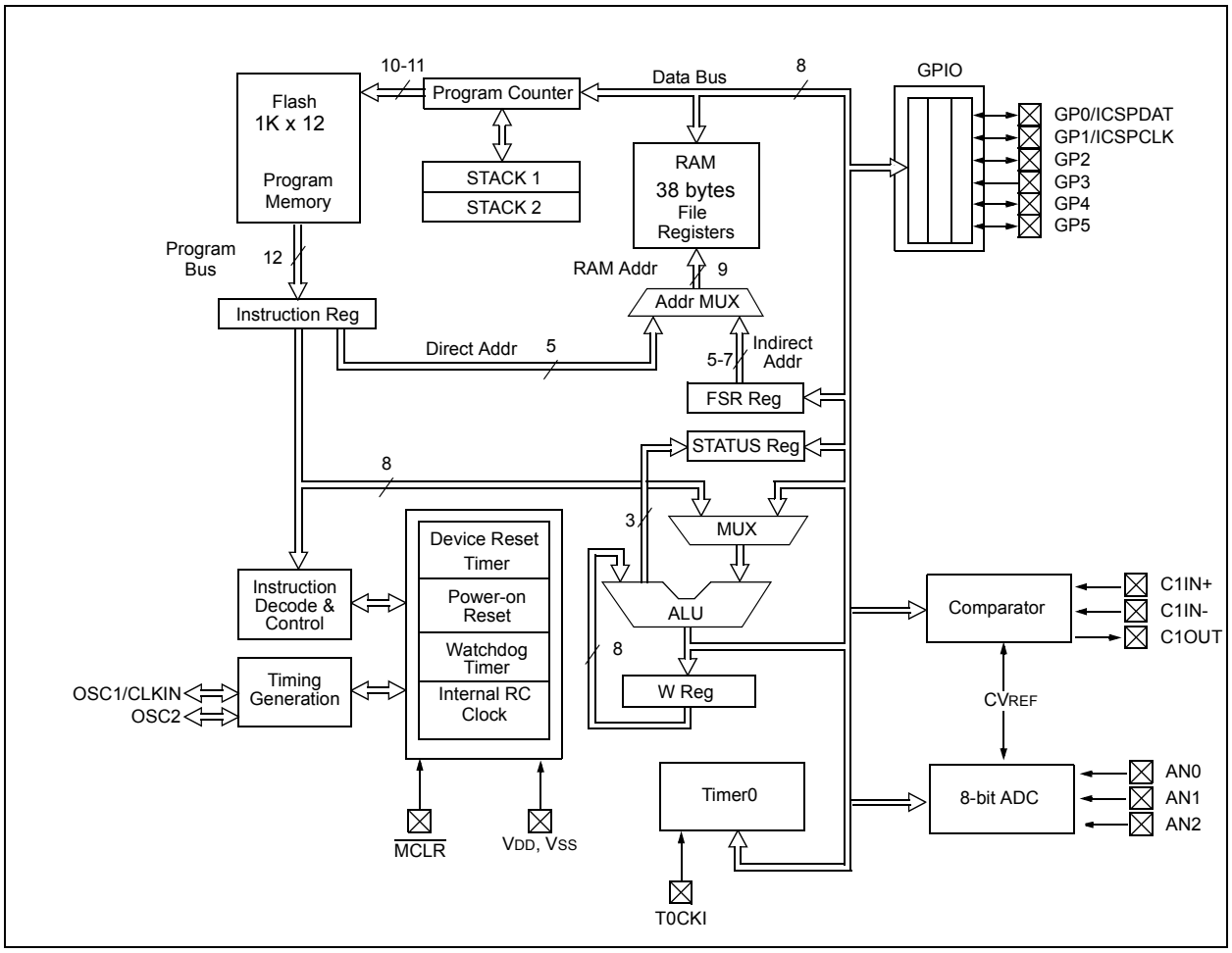
NOTES:

FIGURE 3-1: PIC12F510 SERIES BLOCK DIAGRAM



REGISTER 4-2: STATUS: STATUS REGISTER (PIC16F506)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
RBWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **RBWUF**: PORTB Reset bit
1 = Reset due to wake-up from Sleep on pin change
0 = After power-up or other Reset

bit 6 **CWUF**: Comparator Reset bit
1 = Reset due to wake-up from Sleep on comparator change
0 = After power-up or other Reset

bit 5 **PA0**: Program Page Preselect bit
1 = Page 1 (200h-3FFh)
0 = Page 0 (000h-1FFh)
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.

bit 4 **$\overline{TO}$**: Time-Out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$**: Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit Carry/$\overline{\text{Borrow}}$ bit (for ADDWF and SUBWF instructions)
ADDWF:
1 = A carry from the 4th low-order bit of the result occurred
0 = A carry from the 4th low-order bit of the result did not occur
SUBWF:
1 = A borrow from the 4th low-order bit of the result did not occur
0 = A borrow from the 4th low-order bit of the result occurred

bit 0 **C**: Carry/$\overline{\text{Borrow}}$ bit (for ADDWF, SUBWF and RRF, RLF instructions)

ADDWF:	SUBWF:	RRF or RLF:
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSb or MSb, respectively
0 = A carry did not occur	0 = A borrow occurred	

REGISTER 4-4: OPTION_REG: OPTION REGISTER (PIC16F506)

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{RBWU}}$:** Enable Wake-up On Pin Change bit (RB0, RB1, RB3, RB4)
1 = Disabled
0 = Enabled

bit 6 **$\overline{\text{RBPU}}$:** Enable Weak Pull-Ups bit (RB0, RB1, RB3, RB4)
1 = Disabled
0 = Enabled

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

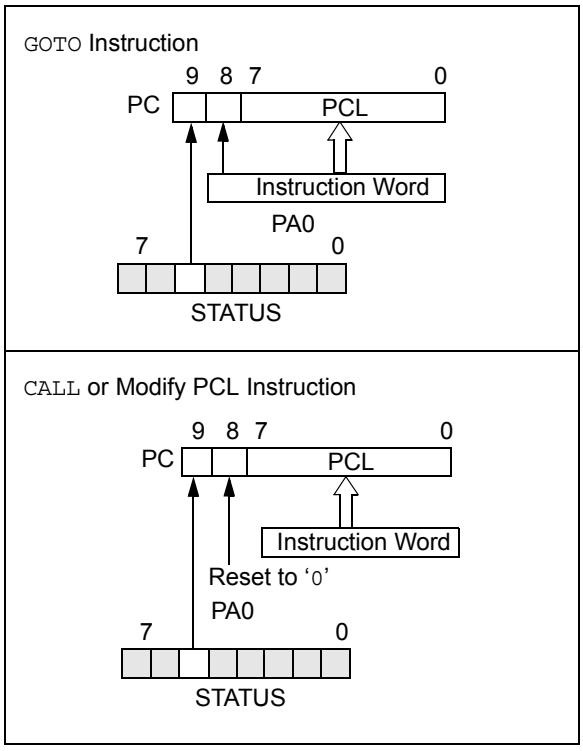
For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The Program Counter (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-4).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-4).

Instructions where the PCL is the destination or modify PCL instructions include MOVWF PC, ADDWF PC and BSF PC,5.

Note:	Because PC<8> is cleared in the CALL instruction or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-4: LOADING OF PC BRANCH INSTRUCTIONS



4.6.1 EFFECTS OF RESET

The PC is set upon a Reset, which means that the PC addresses the last location in the last page (i.e., the oscillator calibration instruction). After executing MOVLW XX, the PC will roll over to location 00h and begin executing user code.

The STATUS register page preselect bits are cleared upon a Reset, which means that page 0 is preselected.

Therefore, upon a Reset, a GOTO instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.7 Stack

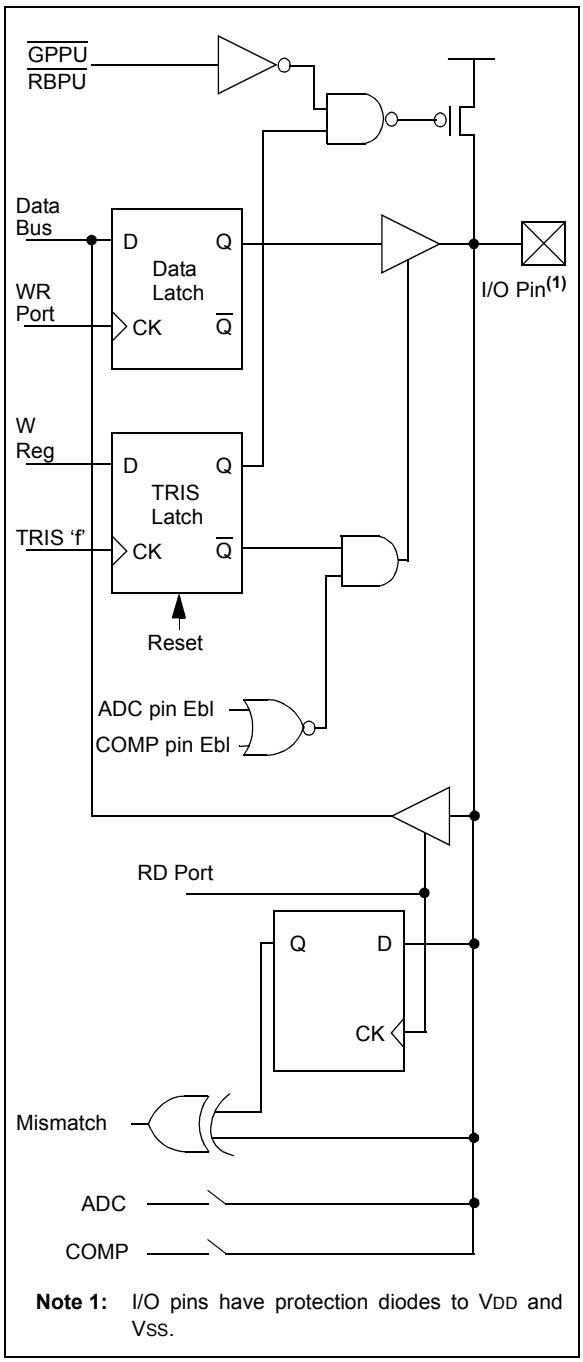
The PIC12F510/16F506 devices have a two-deep, 12-bit wide hardware PUSH/POP stack.

A CALL instruction will PUSH the current value of Stack 1 into Stack 2 and then PUSH the current PC value, incremented by one, into Stack Level 1. If more than two sequential CALLs are executed, only the most recent two return addresses are stored.

A RETLW instruction will POP the contents of Stack Level 1 into the PC and then copy Stack Level 2 contents into Stack Level 1. If more than two sequential RETLWs are executed, the stack will be filled with the address previously stored in Stack Level 2.

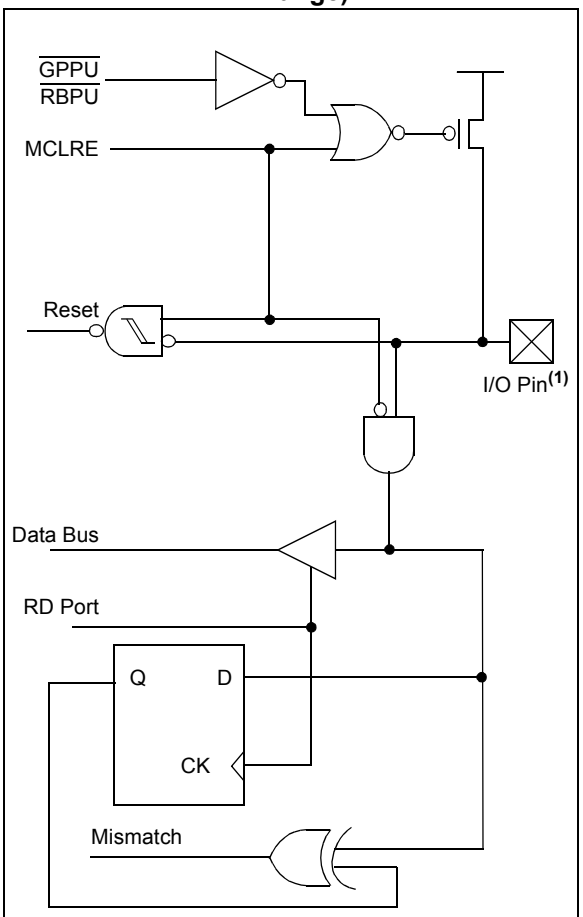
Note 1:	The W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.
2:	There are no Status bits to indicate stack overflows or stack underflow conditions.
3:	There are no instruction mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL and RETLW instructions.

FIGURE 5-2: BLOCK DIAGRAM OF GP0/RB0 AND GP1/RB1



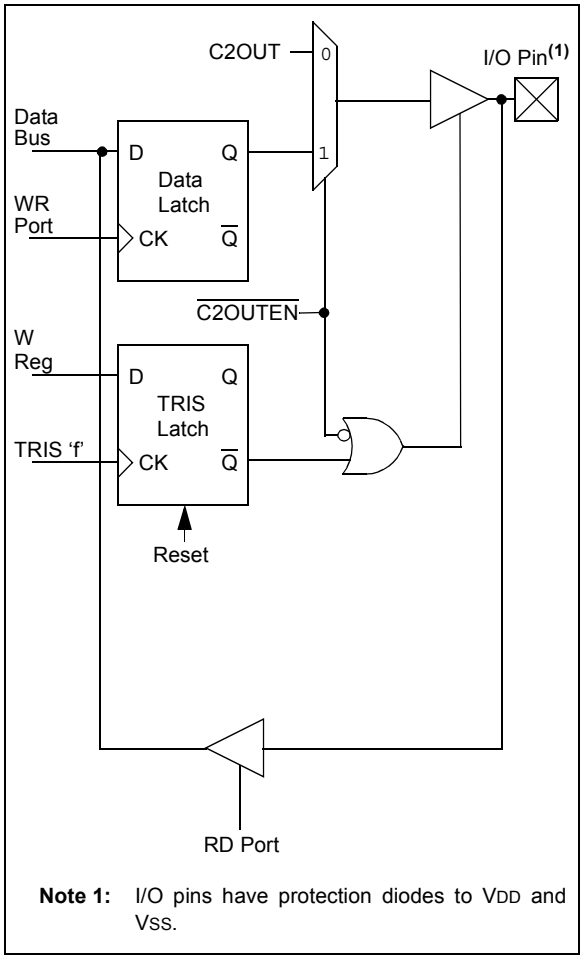
Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 5-3: BLOCK DIAGRAM OF GP3/RB3 (With Weak Pull-up And Wake-up On Change)



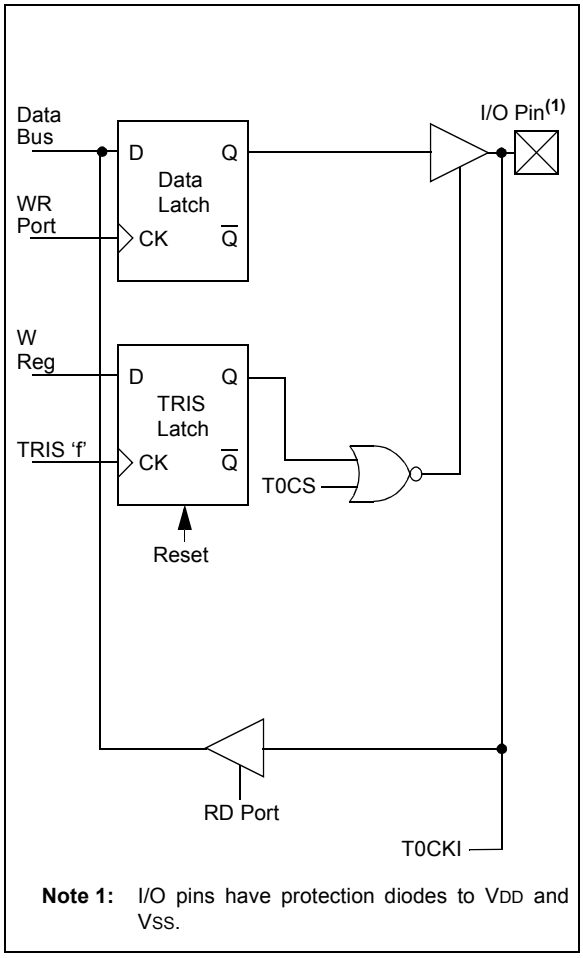
Note 1: GP3/MCLR pin has a protection diode to VSS only.

FIGURE 5-12: BLOCK DIAGRAM OF RC4



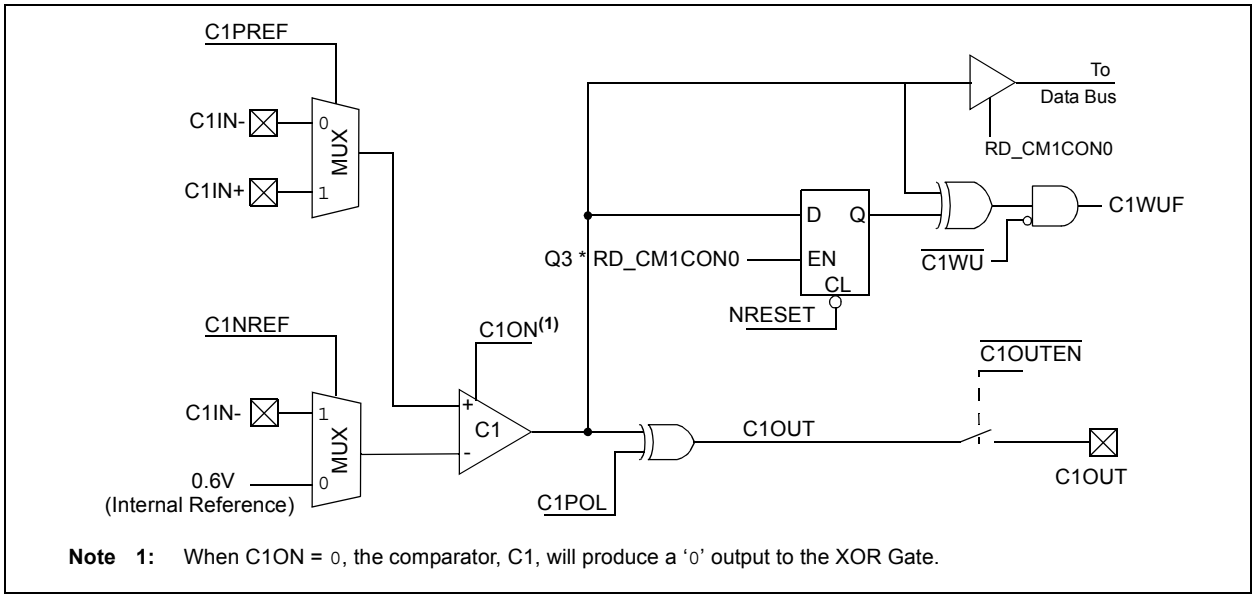
Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 5-13: BLOCK DIAGRAM OF RC5



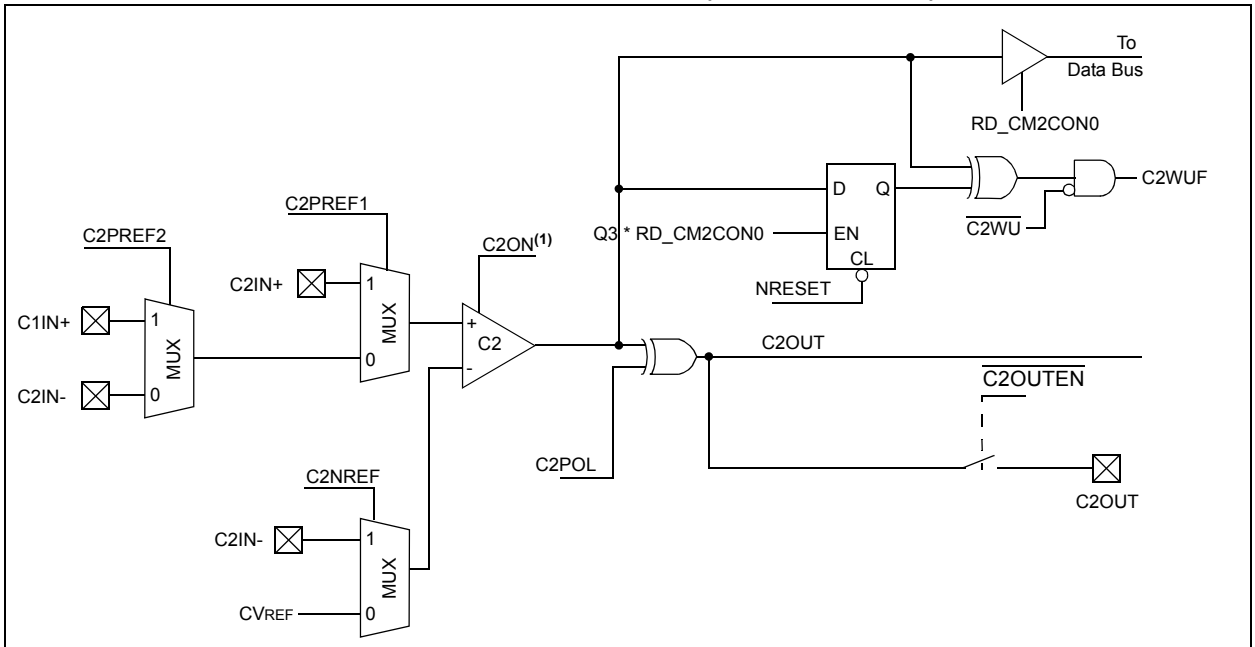
Note 1: I/O pins have protection diodes to VDD and VSS.

FIGURE 7-1: COMPARATOR 1 BLOCK DIAGRAM FOR PIC12F510/16F506



Note 1: When C1ON = 0, the comparator, C1, will produce a '0' output to the XOR Gate.

FIGURE 7-2: COMPARATOR 2 BLOCK DIAGRAM (PIC16F506 ONLY)



Note 1: When C2ON = 0, the comparator, C2, will produce a '0' output to the XOR Gate.

FIGURE 7-4: ANALOG INPUT MODE

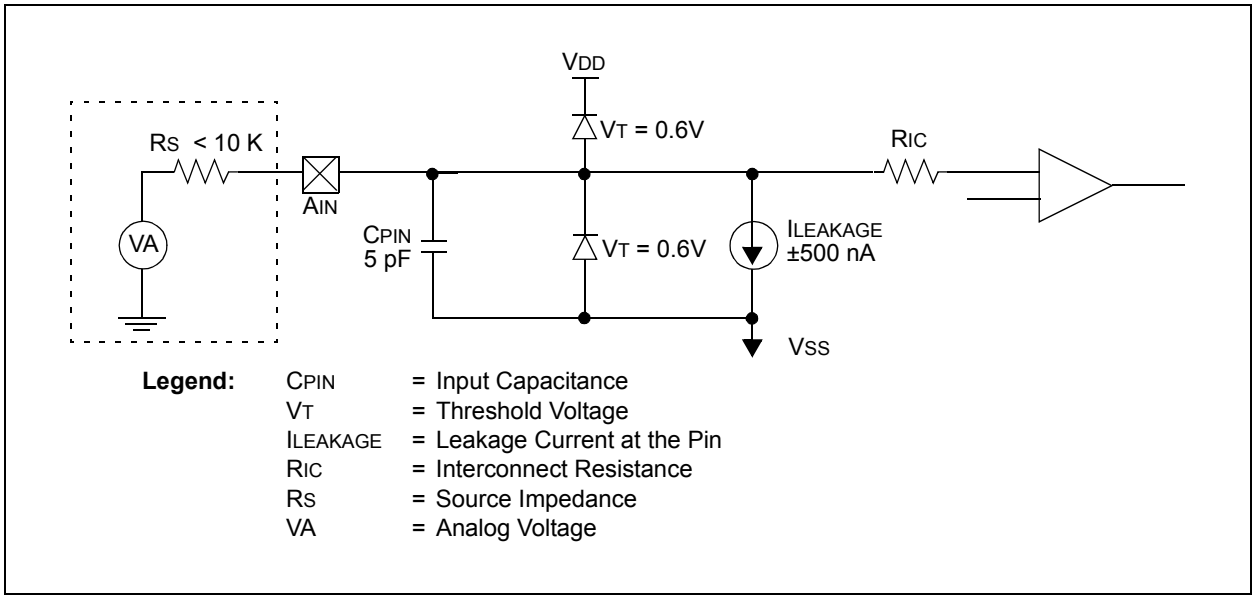


TABLE 7-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Add	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other Resets
03h	STATUS	GPWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	qq0q quuu
07h	CM1CON0(1)	C1OUT	$\overline{C1OUTEN}$	C1POL	$\overline{C1T0CS}$	C1ON	C1NREF	C1PREF	$\overline{C1WU}$	1111 1111	uuuu uuuu
08h	CM1CON0(2)	C1OUT	$\overline{C1OUTEN}$	C1POL	$\overline{C1T0CS}$	C1ON	C1NREF	C1PREF	$\overline{C1WU}$	1111 1111	uuuu uuuu
0Bh	CM2CON0(2)	C2OUT	$\overline{C2OUTEN}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{C2WU}$	1111 1111	uuuu uuuu
N/A	TRISB(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISC(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISGPIO(1)	—	—	I/O Control Register						--11 1111	--11 1111

Legend: x = Unknown, u = Unchanged, – = Unimplemented, read as '0', q = Depends on condition.
Note 1: PIC12F510 only.
2: PIC16F506 only.

9.1.5 SLEEP

This ADC does not have a dedicated ADC clock, and therefore, no conversion in Sleep is possible. If a conversion is underway and a Sleep command is executed, the GO/$\overline{\text{DONE}}$ and ADON bit will be cleared. This will stop any conversion in process and power-down the ADC module to conserve power. Due to the nature of the conversion process, the ADRES may contain a partial conversion. At least 1 bit must have been converted prior to Sleep to have partial conversion data in ADRES. The ADCS and CHS bits are reset to their default condition; ANS<1:0> = 11 and CHS<1:0> = 11.

- For accurate conversions, TAD must meet the following:
- 500 ns < TAD < 50 µs
- TAD = 1/(FOSC/divisor)

Shaded areas indicate TAD out of range for accurate conversions. If analog input is desired at these frequencies, use INTOSC/4 for the ADC clock source.

TABLE 9-2: TAD FOR ADCS SETTINGS WITH VARIOUS OSCILLATORS

Source	ADCS <1:0>	Divisor	20(1) MHz	16(1) MHz	8 MHz	4 MHz	1 MHz	500 kHz	350 kHz	200 kHz	100 kHz	32 kHz
INTOSC	11	4	—	—	.5 µs	1 µs	—	—	—	—	—	—
FOSC	10	4	.2 µs	.25 µs	.5 µs	1 µs	4 µs	8 µs	11 µs	20 µs	40 µs	125 µs
FOSC	01	8	.4 µs	.5 µs	1 µs	2 µs	8 µs	16 µs	23 µs	40 µs	80 µs	250 µs
FOSC	00	16	.8 µs	1 µs	2 µs	4 µs	16 µs	32 µs	46 µs	80 µs	160 µs	500 µs

Note 1: When operating with external oscillator frequencies of 16 MHz or higher, better ADC performance will result from selection of a suitable FOSC divisor value from Table 9-2 than from use of the INTOSC/4 option for the ADC clock.

TABLE 9-3: EFFECTS OF SLEEP ON ADCON0

	ANS1	ANS0	ADCS1	ADCS0	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
Entering Sleep	Unchanged	Unchanged	1	1	1	1	0	0
Wake or Reset	1	1	1	1	1	1	0	0

FIGURE 10-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

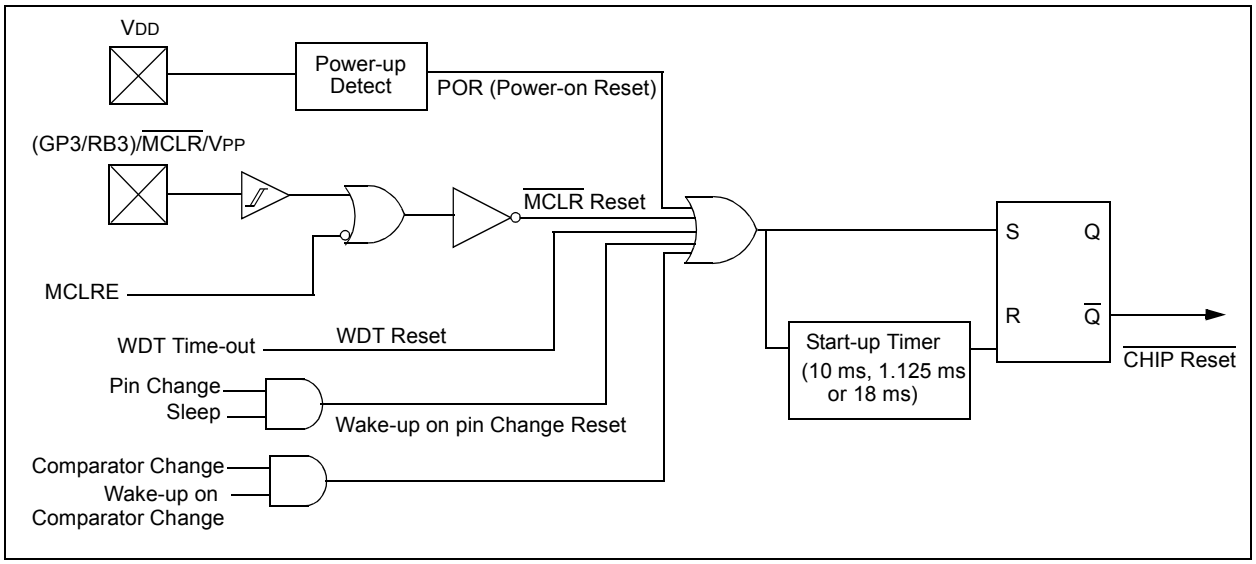


FIGURE 10-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR PULLED LOW)

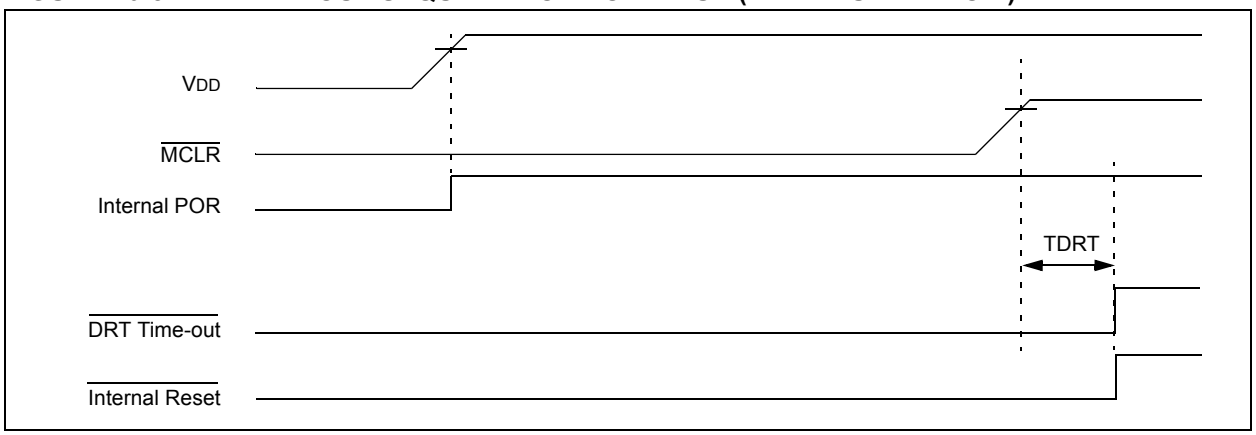
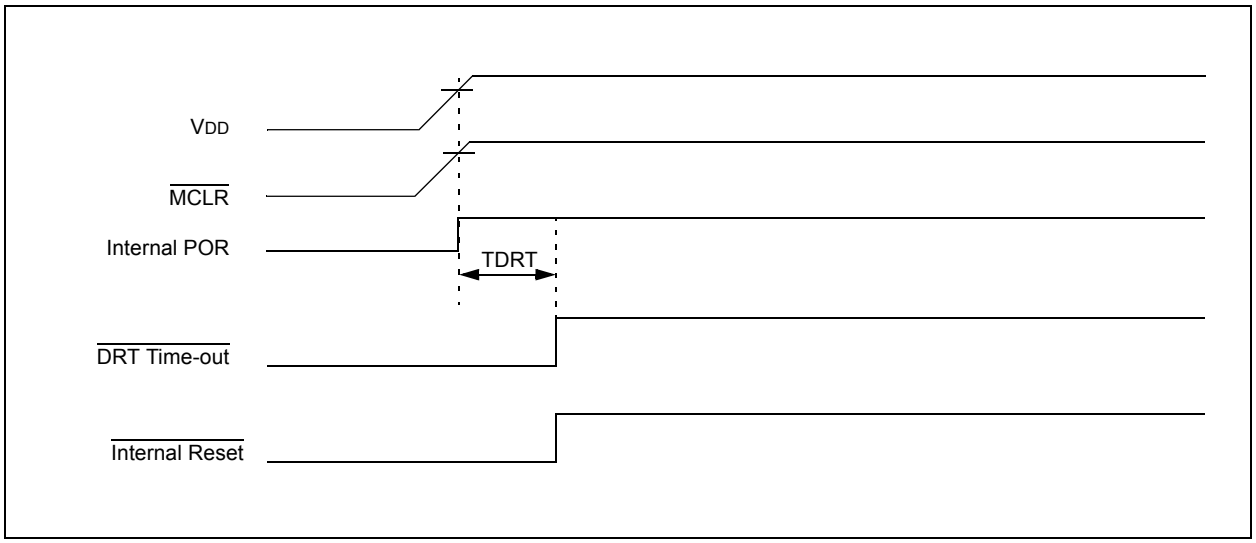


FIGURE 10-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME



10.5 Device Reset Timer (DRT)

On the PIC12F510/16F506 devices, the DRT runs any time the device is powered up. DRT runs from Reset and varies based on oscillator selection and Reset type (see Table 10-6).

The DRT operates from a free running on-chip oscillator that is separate from INTOSC. The processor is kept in Reset as long as the DRT is active. The DRT delay allows VDD to rise above VDD minimum and for the oscillator to stabilize.

Oscillator circuits, based on crystals or ceramic resonators, require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the devices in a Reset for a set period, as stated in Table 10-6, after $\overline{MCLR}$ has reached a logic high (VIH $\overline{MCLR}$) level. Programming (GP3/RB3)/$\overline{MCLR}$/VPP as $\overline{MCLR}$ and using an external RC network connected to the $\overline{MCLR}$ input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the (GP3/RB3)/$\overline{MCLR}$/VPP pin as a general purpose input.

The DRT delays will vary from chip-to-chip due to VDD, temperature and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out from Sleep. This is particularly important for applications using the WDT to wake from Sleep mode automatically.

Reset sources are POR, $\overline{MCLR}$, WDT time-out, Wake-up on Pin Change and Wake-up on Comparator Change. See **Section 10.9.2 "Wake-up from Sleep Reset", Notes 1, 2 and 3**.

10.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator that does not require any external components. This RC oscillator is separate from the external RC oscillator of the (GP5/RB5)/OSC1/CLKIN pin and the internal 4/8 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset generates a device Reset.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see **Section 10.1 "Configuration Bits"**). Refer to the PIC12F510/16F506 Programming Specifications to determine how to access the Configuration Word.

TABLE 10-6: TYPICAL DRT PERIODS

Oscillator Configuration	POR Reset	Subsequent Resets
LP	18 ms	18 ms
XT	18 ms	18 ms
HS(1)	18 ms	18 ms
EC(1)	1.125 ms	10 µs
INTOSC	1.125 ms	10 µs
EXTRC	1.125 ms	10 µs

Note 1: PIC16F506 only

Note:	It is the responsibility of the application designer to ensure the use of the 1.125 ms nominal DRT will result in acceptable operation. Refer to Electrical Specifications for VDD rise time and stability requirements for this mode of operation.

10.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a divisor ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

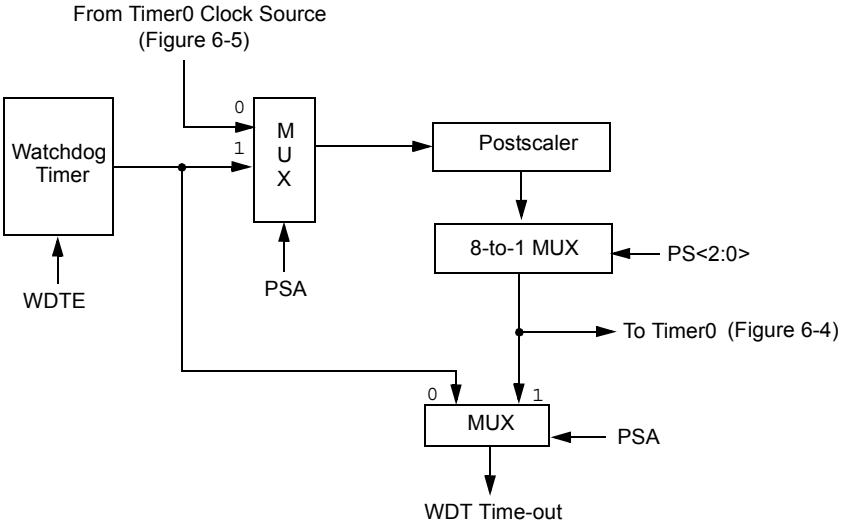
Under worst-case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

10.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

FIGURE 10-11: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

TABLE 10-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	OPTION(1)	$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION(2)	$\overline{RBWU}$	$\overline{RBPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded boxes = Not used by Watchdog Timer. – = unimplemented, read as '0', u = unchanged.

Note 1: PIC12F510 only.

2: PIC16F506 only.

10.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (TO, PD, GPWUF/RBWUF)

The $\overline{TO}$, $\overline{PD}$ and (GPWUF/RBWUF) bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) Reset.

TABLE 10-8: $\overline{TO}$/$\overline{PD}$/(GPWUF/RBWUF) STATUS AFTER RESET

CWUF	GPWUF/ RBWUF	$\overline{TO}$	$\overline{PD}$	Reset Caused By
0	0	0	0	WDT wake-up from Sleep
0	0	0	u	WDT time-out (not from Sleep)
0	0	1	0	$\overline{MCLR}$ wake-up from Sleep
0	0	1	1	Power-up
0	0	u	u	$\overline{MCLR}$ not during Sleep
0	1	1	0	Wake-up from Sleep on pin change
1	0	1	0	Wake-up from Sleep on comparator change

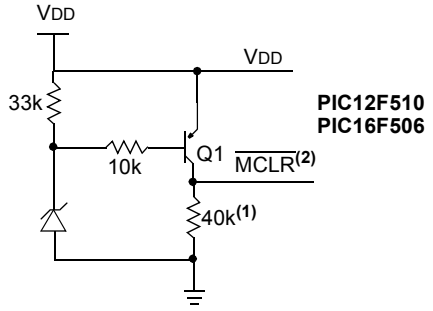
Legend: u = unchanged

10.8 Reset on Brown-out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

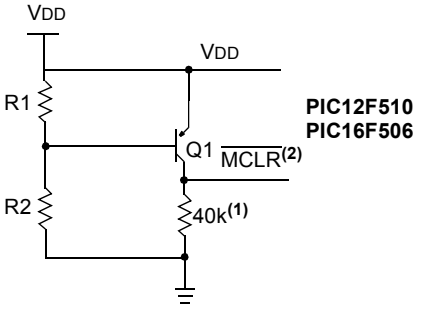
To reset PIC12F510/16F506 devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 10-12 and Figure 10-13.

FIGURE 10-12: BROWN-OUT PROTECTION CIRCUIT 1



Note 1: This circuit will activate Reset when V_{DD} goes below Vz + 0.7V (where Vz = Zener voltage).
2: Pin must be configured as $\overline{MCLR}$.

FIGURE 10-13: BROWN-OUT PROTECTION CIRCUIT 2

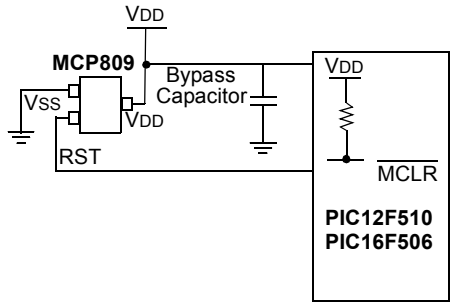


Note 1: This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

2: Pin must be configured as $\overline{MCLR}$.

FIGURE 10-14: BROWN-OUT PROTECTION CIRCUIT 3



Note: This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. There are 7 different trip point selections to accommodate 5V to 3V systems.

13.2 DC Characteristics: PIC12F510/16F506 (Extended)

DC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 40°C ≤ TA ≤ +125°C (extended)				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	See **Figure 14-1**
D002	VDR	**RAM Data Retention Voltage(2)**	—	1.5*	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See **Section 10.4 "Power-on Reset (POR)"** for details
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See **Section 10.4 "Power-on Reset (POR)"** for details
D010	IDD	**Supply Current(3,4)**	— —	175 0.625	275 1.1	µA mA	FOSC = 4 MHz, VDD = 2.0V FOSC = 4 MHz, VDD = 5.0V
			— —	250 1.0	450 1.5	µA mA	FOSC = 8 MHz, VDD = 2.0V FOSC = 8 MHz, VDD = 5.0V
			—	1.4	2.0	mA	FOSC = 20 MHz, VDD = 5.0V
			— —	11 38	16 54	µA µA	FOSC = 32 kHz, VDD = 2.0V FOSC = 32 kHz, VDD = 5.0V
D020	IPD	**Power-down Current(5)**	— —	0.1 0.35	9.0 15.0	µA µA	VDD = 2.0V VDD = 5.0V
D022	IWDT	**WDT Current(5)**	— —	1.0 7.0	18 22	µA µA	VDD = 2.0V VDD = 5.0V
D023	ICMP	**Comparator Current(5)**	— —	15 55	25 75	µA µA	VDD = 2.0V (per comparator) VDD = 5.0V (per comparator)
D022	ICVREF	**CVREF Current(5)**	— —	30 75	65 135	µA µA	VDD = 2.0V (high range) VDD = 5.0V (high range)
D023	IFVR	**Internal 0.6V Fixed Voltage Reference Current(5)**	— —	85 175	130 220	µA µA	VDD = 2.0V (0.6V reference and 1 comparator enabled) VDD = 5.0V (0.6V reference and 1 comparator enabled)
D024	ΔIAD	**A/D Conversion Current(5)**	—	120	150	µA	2.0V
			—	200	250	µA	5.0V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

4: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

5: For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

6: Does not include current through REXT. The current through the resistor can be estimated by the formula: I = VDD/2REXT (mA) with REXT in kΩ.

FIGURE 14-4: COMPARATOR IPD vs. VDD (COMPARATOR ENABLED)

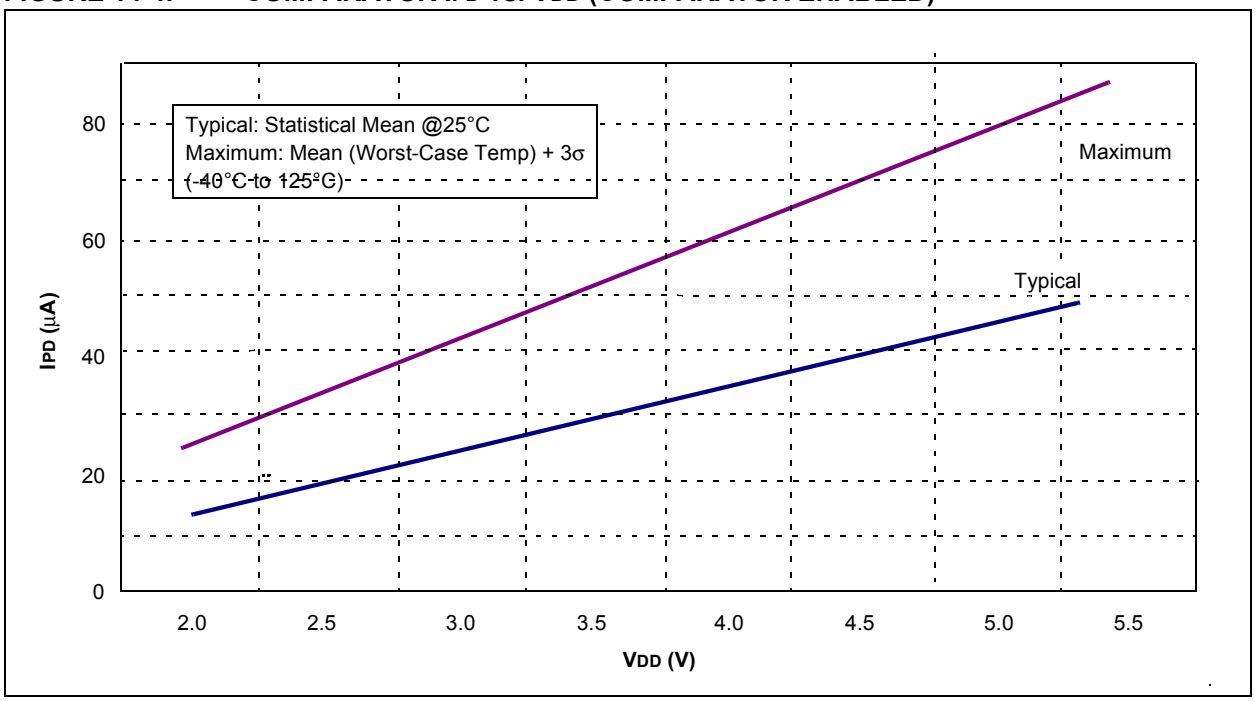


FIGURE 14-5: TYPICAL WDT IPD vs. VDD

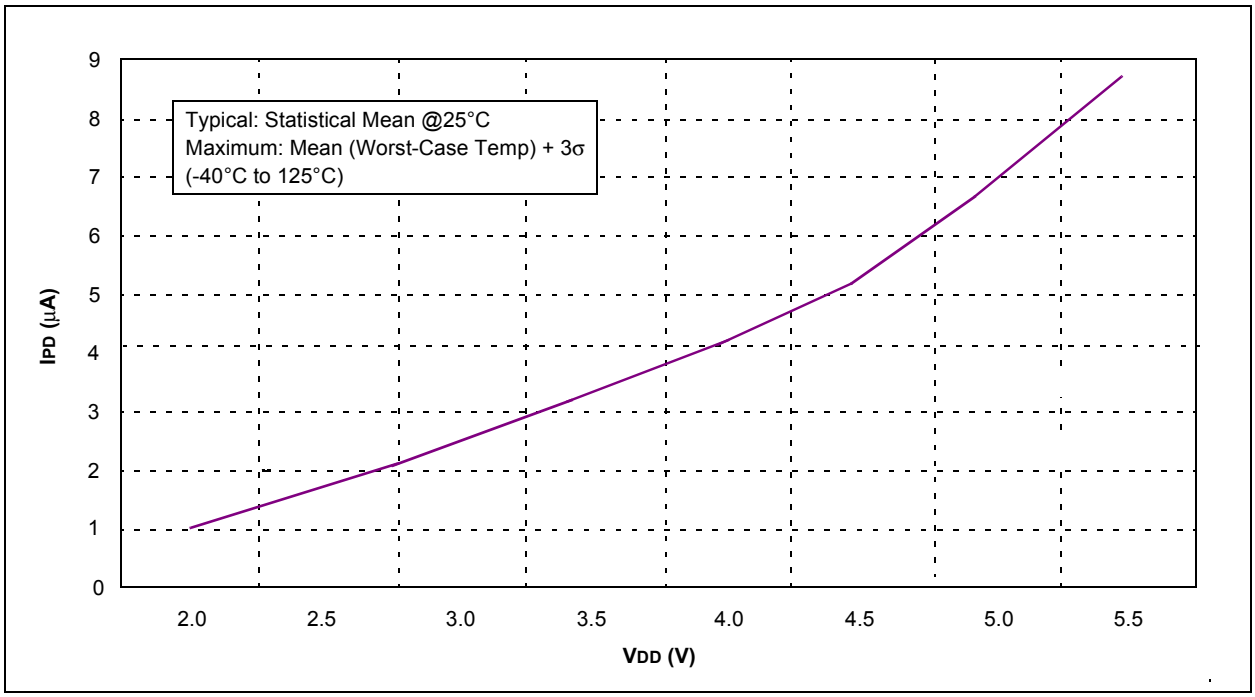
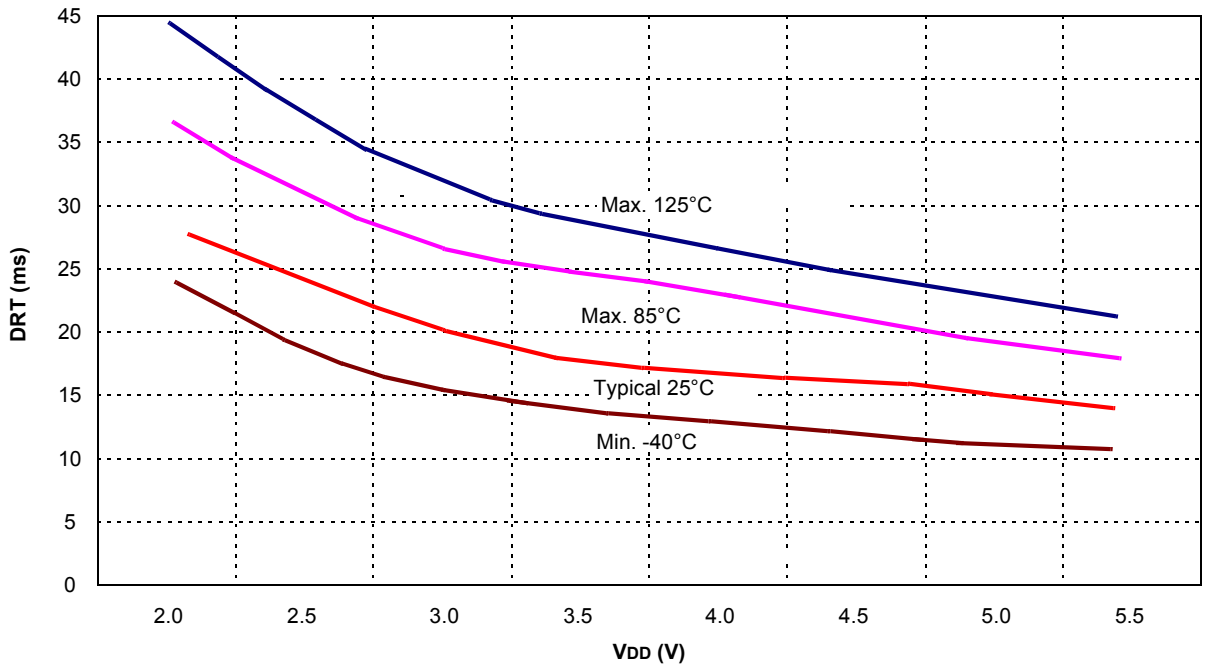


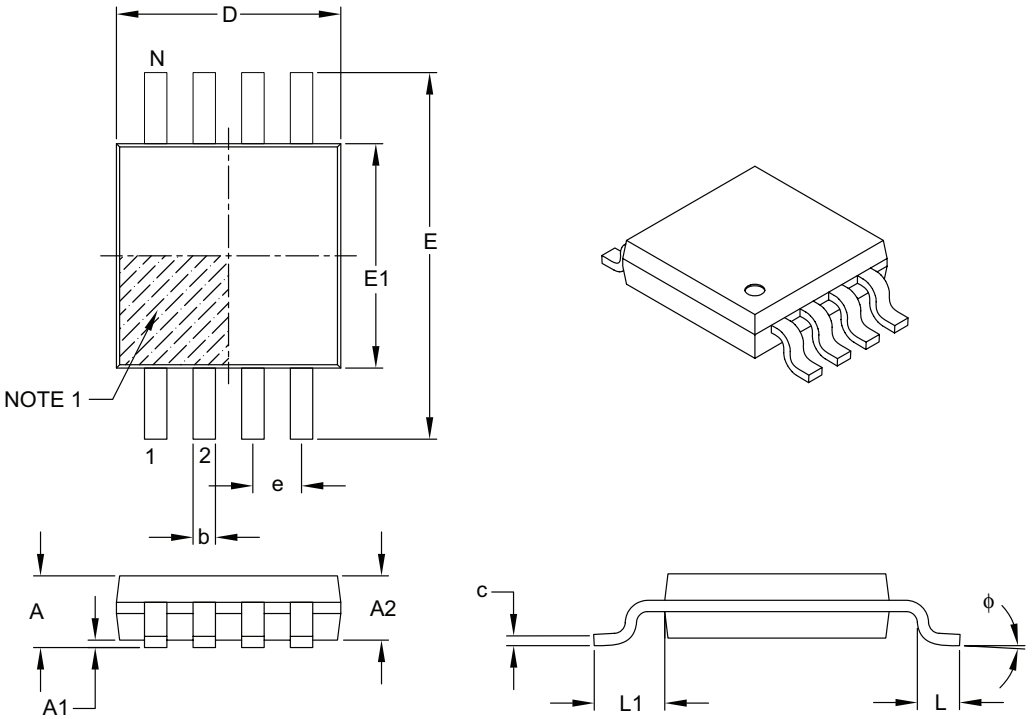
FIGURE 14-14: DEVICE RESET TIMER (HS, XT AND LP) vs. VDD



Note: See Table 13-7 if another clock mode is selected.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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