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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 11 |
| Program Memory Size | 1.5KB (1K x 12) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 67 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | A/D 4x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 14-SOIC (0.154", 3.90mm Width) |
| Supplier Device Package | 14-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f506-i-sl |

# PIC12F510/16F506

## 8/14-Pin, 8-Bit Flash Microcontroller

### Devices Included In This Data Sheet:

- PIC16F506
- PIC12F510

### High-Performance RISC CPU:

- Only 33 Single-Word Instructions to Learn
- All Single-Cycle Instructions except for Program Branches, which are Two-Cycle
- 12-Bit Wide Instructions
- Two-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- 8-Bit Wide Data Path
- 10 Special Function Hardware Registers (PIC12F510)
- 13 Special Function Hardware Registers (PIC16F506)
- Operating Speed:
  - DC – 8 MHz Crystal Oscillator (PIC12F510)
  - DC – 500 ns instruction cycle (PIC12F510)
  - DC – 20 MHz Crystal Oscillator (PIC16F506)
  - DC – 200 ns instruction cycle (PIC16F506)

### Special Microcontroller Features:

- 4 or 8 MHz Selectable Precision Internal Oscillator:
  - Factory calibrated to ±1%
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debugging (ICD) Support
- Power-on Reset (POR)
- Device Reset Timer (DRT):
  - Short DRT (1.125 ms, typical) for INTOSC, EXTRC and EC
  - DRT (18 ms, typical) for HS, XT and LP
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed $\overline{\text{MCLR}}$ Input Pin
- Selectable Internal Weak Pull-Ups on I/O Pins
- Power-Saving Sleep mode
- Wake-up from Sleep on Pin Change
- Wake-up from Sleep on Comparator Change
- Selectable Oscillator Options:
  - INTOSC: 4/8 MHz precision Internal oscillator
  - EXTRC: External low-cost RC oscillator
  - XT: Standard crystal/resonator
  - LP: Power-saving, low-frequency crystal
  - HS: High-speed crystal/resonator (PIC16F506 only)
  - EC: High-speed external clock input (PIC16F506 only)
- Analog-to-Digital (A/D) Converter:
  - 8-bit resolution
  - 4-input channels (1 channel is dedicated to conversion of the internal 0.6V absolute voltage reference)
- High Current Sink/Source for Direct LED Drive
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

### Low-Power Features/CMOS Technology:

- Operating Current:
  - < 175 μA @ 2V, 4 MHz, typical
- Standby Current:
  - 100 nA @ 2V, typical
- Low-Power, High-Speed Flash Technology:
  - 100,000 cycle Flash endurance
  - > 40-year retention
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
- Wide Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

### Peripheral Features (PIC12F510):

- 6 I/O Pins:
  - 5 I/O pins with individual direction control
  - 1 input only pin
- 1 Analog Comparator with Absolute Reference

### Peripheral Features (PIC16F506):

- 12 I/O Pins:
  - 11 I/O pins with individual direction control
  - 1 input only pin
- 2 Analog Comparators with Absolute Reference and Programmable Reference

**NOTES:**

## 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC12F510/16F506 devices can be attributed to a number of architectural features commonly found in RISC microprocessors. The PIC12F510/16F506 devices use a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200 ns @ 20 MHz, 1 µs @ 4 MHz) except for program branches.

Table 3-1 lists program memory (Flash) and data memory (RAM) for the PIC12F510/16F506 devices.

**TABLE 3-1: PIC12F510/16F506 MEMORY**

| Device | Memory | |
|---|---|---|
| | Program | Data |
| PIC12F510 | 1024 x 12 | 38 x 8 |
| PIC16F506 | 1024 x 12 | 67 x 8 |

The PIC12F510/16F506 devices can directly or indirectly address its register files and data memory. All Special Function Registers (SFRs), including the PC, are mapped in the data memory. The PIC12F510/16F506 devices have a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any addressing mode. This symmetrical nature and lack of “special optimal situations” make programming with the PIC12F510/16F506 devices simple, yet efficient. In addition, the learning curve is reduced significantly.

The PIC12F510/16F506 devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two’s complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single-operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the `SUBWF` and `ADDWF` instructions for examples.

A simplified block diagram is shown in Figure 3-1 for PIC12F510 with the corresponding device pins described in Table 3-2. A simplified block diagram for PIC16F506 is shown in Figure 3-2 with the corresponding device pins described in Table 3-3.

**REGISTER 4-2: STATUS: STATUS REGISTER (PIC16F506)**

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| RBWUF | CWUF | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **RBWUF**: PORTB Reset bit
1 = Reset due to wake-up from Sleep on pin change
0 = After power-up or other Reset

bit 6 **CWUF**: Comparator Reset bit
1 = Reset due to wake-up from Sleep on comparator change
0 = After power-up or other Reset

bit 5 **PA0**: Program Page Preselect bit
1 = Page 1 (200h-3FFh)
0 = Page 0 (000h-1FFh)
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.

bit 4 **$\overline{TO}$**: Time-Out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$**: Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit Carry/$\overline{\text{Borrow}}$ bit (for ADDWF and SUBWF instructions)
ADDWF:
1 = A carry from the 4th low-order bit of the result occurred
0 = A carry from the 4th low-order bit of the result did not occur
SUBWF:
1 = A borrow from the 4th low-order bit of the result did not occur
0 = A borrow from the 4th low-order bit of the result occurred

bit 0 **C**: Carry/$\overline{\text{Borrow}}$ bit (for ADDWF, SUBWF and RRF, RLF instructions)

| ADDWF: | SUBWF: | RRF or RLF: |
|---|---|---|
| 1 = A carry occurred | 1 = A borrow did not occur | Load bit with LSb or MSb, respectively |
| 0 = A carry did not occur | 0 = A borrow occurred | |

## 4.8 Indirect Data Addressing: INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

### 4.8.1 INDIRECT ADDRESSING EXAMPLE

- Register file 07 contains the value 10h
- Register file 08 contains the value 0Ah
- Load the value 07 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 08)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-1.

**EXAMPLE 4-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING**

```
        MOVLW   0x10     ;initialize pointer
        MOVWF   FSR      ;to RAM
NEXT    CLRF    INDF     ;clear INDF register
        INCF    FSR,F    ;inc pointer
        BTFSC   FSR,4    ;all done?
        GOTO    NEXT     ;NO, clear next
CONTINUE
            :            ;YES, continue
            :
```

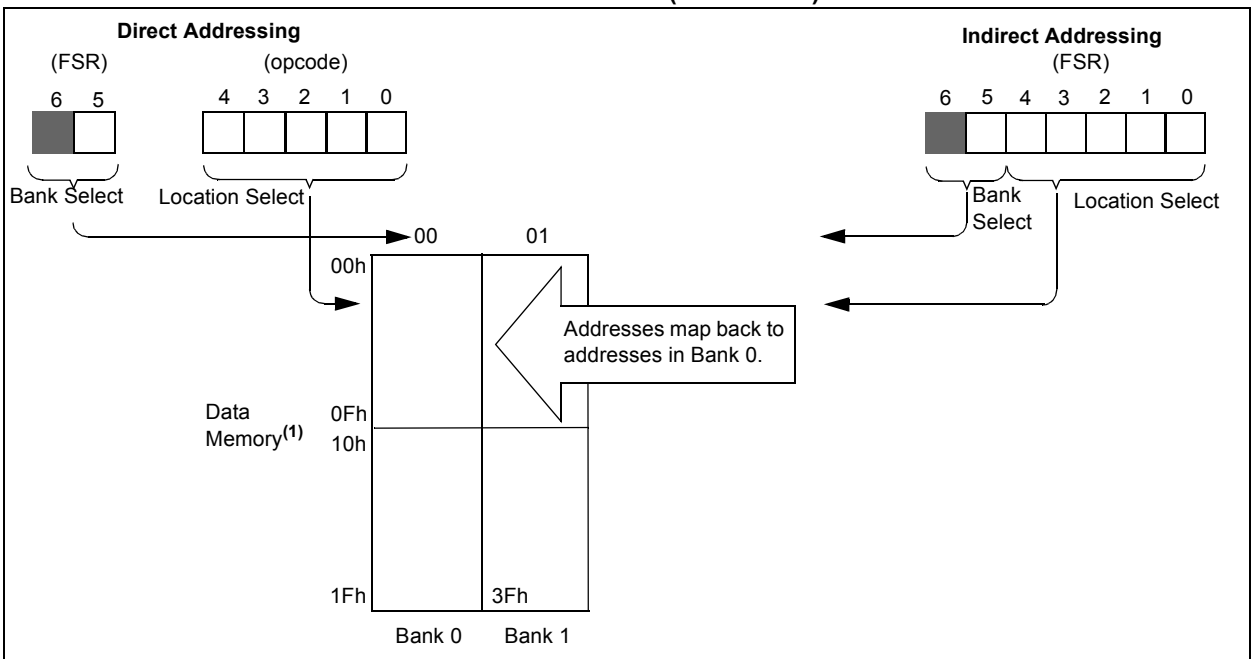
The FSR is a 5-bit wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

**PIC16F506** – Uses FSR<6:5>. Selects from Bank 0 to Bank 3. FSR<7> is unimplemented, read as '1'.

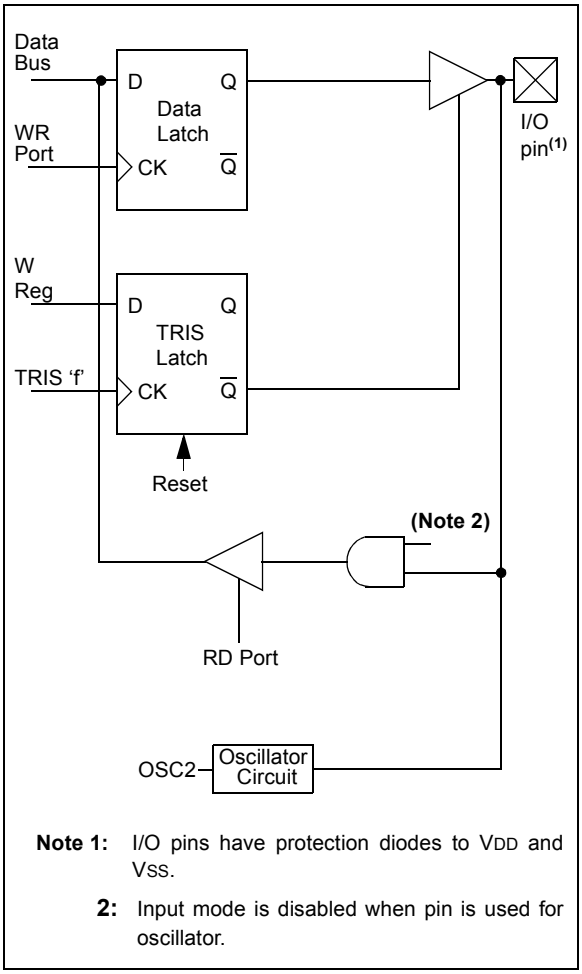
**PIC12F510** – Uses FSR<5>. Selects from Bank 0 to Bank 1. FSR<7:6> are unimplemented, read as '11'.

**FIGURE 4-5: DIRECT/INDIRECT ADDRESSING (PIC12F510)**




**Note 1:** For register map detail, see Figure 4-2.
**2:** Grey boxes are unimplemented and read as '1'.

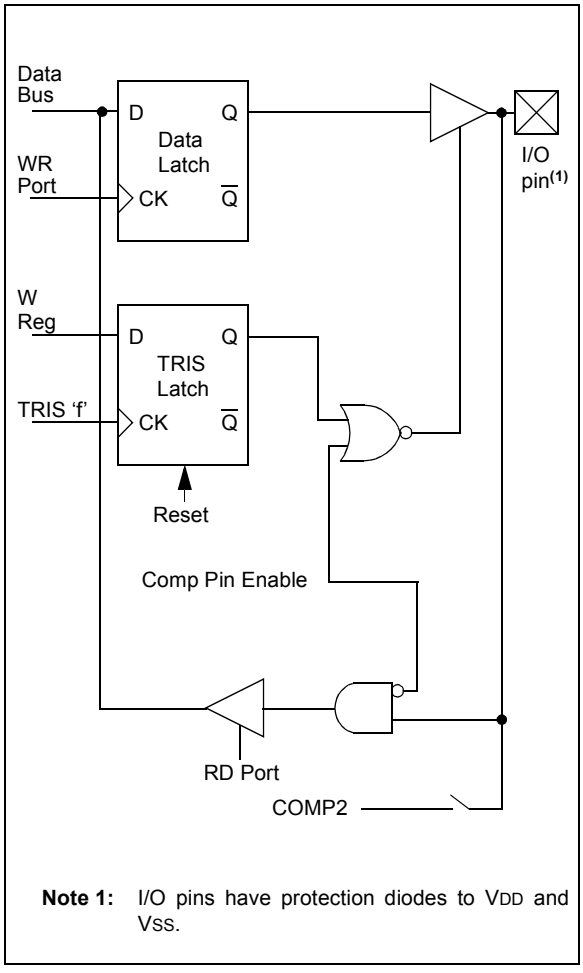
**FIGURE 5-8: BLOCK DIAGRAM OF RB5/GP5**




**Note 1:** I/O pins have protection diodes to VDD and VSS.

**2:** Input mode is disabled when pin is used for oscillator.

**FIGURE 5-9: BLOCK DIAGRAM OF RC0/RC1**




**Note 1:** I/O pins have protection diodes to VDD and VSS.

**TABLE 5-1: SUMMARY OF PORT REGISTERS**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | TRISGPIO(1) | — | — | I/O Control Register | | | | | | --11 1111 | --11 1111 |
| N/A | TRISB(2) | — | — | I/O Control Register | | | | | | --11 1111 | --11 1111 |
| N/A | TRISC(2) | — | — | I/O Control Register | | | | | | --11 1111 | --11 1111 |
| N/A | OPTION(1) | $\overline{GPWU}$ | $\overline{GPPU}$ | T0CS | TOSE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| N/A | OPTION(2) | $\overline{RBWU}$ | $\overline{RBPU}$ | T0CS | TOSE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 03h | STATUS(1) | GPWUF | CWUF | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | qq0q quuu(3) |
| 03h | STATUS(2) | RBWUF | CWUF | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | qq0q quuu(3) |
| 06h | GPIO(1) | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx | --uu uuuu |
| 06h | PORTB(2) | — | — | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | --xx xxxx | --uu uuuu |
| 07h | PORTC(2) | — | — | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | --xx xxxx | --uu uuuu |

**Legend:** – = unimplemented read as '0', x = unknown, u = unchanged, q = depends on condition.

**Note 1:** PIC12F510 only.

**2:** PIC16F506 only.

**3:** If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

**TABLE 5-2: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)**

| Priority | RB0 | RB1 | RB2 | RB3 | RB4 | RB5 |
|---|---|---|---|---|---|---|
| 1 | AN0/C1IN+ | AN1/C1IN- | AN2 | Input/$\overline{MCLR}$ | OSC2/CLKOUT | OSC1/CLKIN |
| 2 | TRISB | TRISB | C1OUT | — | TRISB | TRISB |
| 3 | — | — | TRISB | — | — | — |

**TABLE 5-3: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)**

| Priority | RC0 | RC1 | RC2 | RC3 | RC4 | RC5 |
|---|---|---|---|---|---|---|
| 1 | C2IN+ | C2IN- | $CV_{REF}$ | TRISC | C2OUT | T0CKI |
| 2 | TRISC | TRISC | TRISC | — | TRISC | TRISC |

**TABLE 5-4: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC12F510)**

| Priority | GP0 | GP1 | GP2 | GP3 | GP4 | GP5 |
|---|---|---|---|---|---|---|
| 1 | AN0/C1IN+ | AN1/C1IN- | AN2 | Input/$\overline{MCLR}$ | OSC2 | OSC1/CLKIN |
| 2 | TRISIO | TRISIO | C1OUT | — | TRISIO | TRISIO |
| 3 | — | — | T0CKI | — | — | — |
| 4 | — | — | TRISIO | — | — | — |

**TABLE 5-6: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC16F506 PORTB)(1), (2)**

| | RB0 | RB0 | RB0 | RB1 | RB1 | RB2 | RB2 | RB3 | RB4 | RB5 |
|---|---|---|---|---|---|---|---|---|---|---|
| **CM1CON0** | | | | | | | | | | |
| C1ON | — | 0 | 1 | 0 | 1 | 0 | 1 | — | — | — |
| C1PREF | — | — | 0 | — | — | — | — | — | — | — |
| C1NREF | — | — | — | — | 0 | — | — | — | — | — |
| $\overline{\text{C1T0CS}}$ | — | — | — | — | — | — | — | — | — | — |
| $\overline{\text{C1OUTEN}}$ | — | — | — | — | — | — | 1 | — | — | — |
| **CM2CON0** | | | | | | | | | | |
| C2ON | 1 | — | — | — | — | — | — | — | — | — |
| C2PREF1 | 0 | — | — | — | — | — | — | — | — | — |
| C2PREF2 | 1 | — | — | — | — | — | — | — | — | — |
| C2NREF | — | — | — | — | — | — | — | — | — | — |
| $\overline{\text{C2OUTEN}}$ | — | — | — | — | — | — | — | — | — | — |
| **OPTION** | | | | | | | | | | |
| T0CS | — | — | — | — | — | — | — | — | — | — |
| **ADCON0** | | | | | | | | | | |
| ANS<1:0> | 00, 01 | 00, 01 | 00, 01 | 00, 01, 10 | 00, 01, 10 | 00 | 00 | — | — | — |
| **CONFIG** | | | | | | | | | | |
| MCLRE | — | — | — | — | — | — | — | 0 | — | — |
| INTOSC | — | — | — | — | — | — | — | — | — | — |
| LP | — | — | — | — | — | — | — | — | Disabled | Disabled |
| EXTRC | — | — | — | — | — | — | — | — | — | Disabled |
| XT | — | — | — | — | — | — | — | — | Disabled | Disabled |
| EC | — | — | — | — | — | — | — | — | — | Disabled |
| HS | — | — | — | — | — | — | — | — | Disabled | Disabled |
| INTOSC CLKOUT | — | — | — | — | — | — | — | — | Disabled | Disabled |
| EXTRC CLOCKOUT | — | — | — | — | — | — | — | — | Disabled | Disabled |

**Note 1:** Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

**2:** Shaded cells indicate the bit status does not affect the pins digital functionality.

**TABLE 5-7: REQUIREMENTS FOR DIGITAL PIN OPERATION (PIC16F506 PORTC)(1), (2)**

| | RC0 | RC0 | RC1 | RC1 | RC2 | RC3 | RC4 | RC4 | RC5 | RC5 |
|---|---|---|---|---|---|---|---|---|---|---|
| **CM2CON0** | | | | | | | | | | |
| C2ON | 0 | 1 | 0 | 1 | — | — | 0 | 1 | — | — |
| C2PREF1 | — | 0 | — | — | — | — | — | — | — | — |
| C2PREF2 | — | 0 | — | — | — | — | — | — | — | — |
| C2NREF | — | — | — | 0 | — | — | — | — | — | — |
| $\overline{\text{C2OUTEN}}$ | — | — | — | — | — | — | — | 1 | — | — |
| **VRCON0** | | | | | | | | | | |
| VROE | — | — | — | — | 0 | — | — | — | — | — |
| **OPTION** | | | | | | | | | | |
| T0CS | — | — | — | — | — | — | — | — | 0 | — |

**Note 1:** Multiple column entries for a pin demonstrate the different permutations to arrive at digital functionality for the pin.

**2:** Shaded cells indicate the bit status does not affect the pins digital functionality.

**FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE**

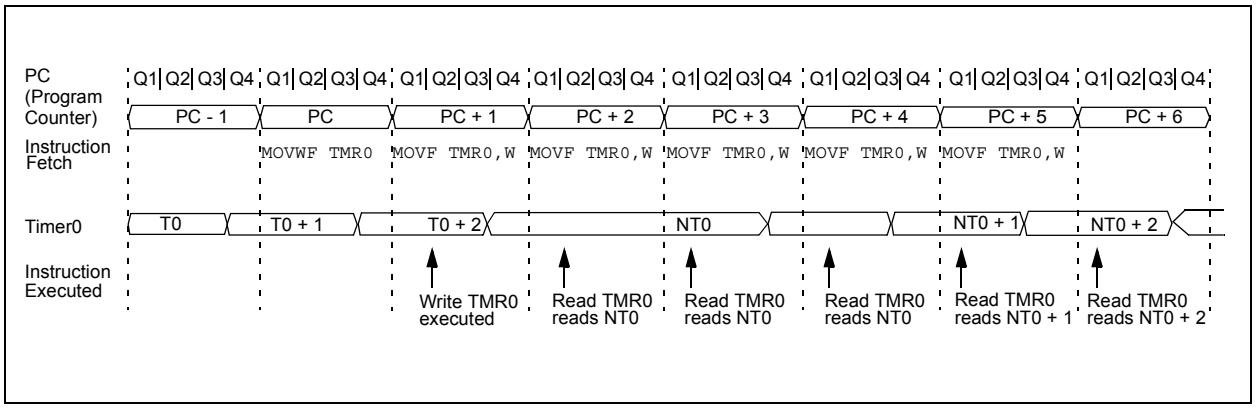



**FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2**

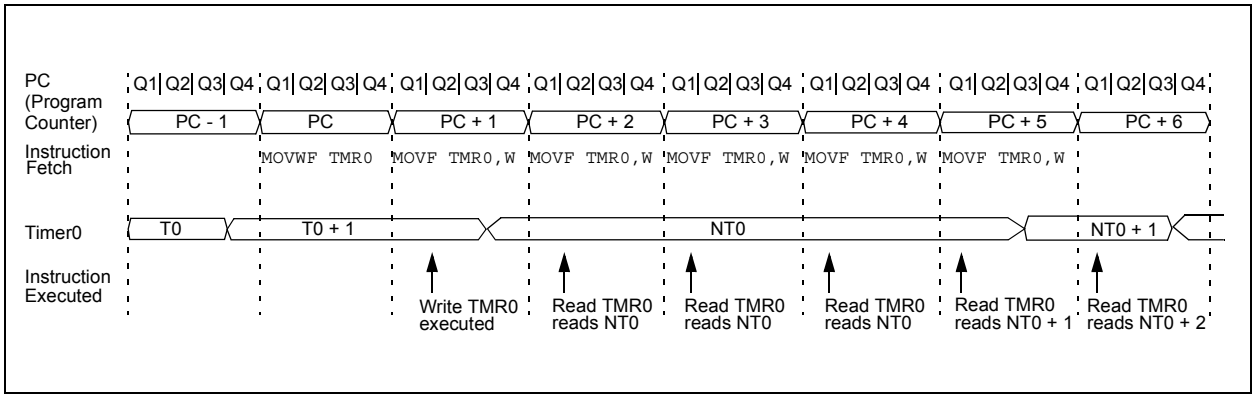



**TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01h | TMR0 | Timer0 – 8-bit Real-Time Clock/Counter | | | | | | | | xxxx xxxx | uuuu uuuu |
| 07h | CM1CON0(2) | C1OUT | $\overline{\text{C1OUTEN}}$ | C1POL | $\overline{\text{C1T0CS}}$ | C1ON | C1NREF | C1PREF | $\overline{\text{C1WU}}$ | 1111 1111 | uuuu uuuu |
| 08h | CM1CON0(3) | C1OUT | $\overline{\text{C1OUTEN}}$ | C1POL | $\overline{\text{C1T0CS}}$ | C1ON | C1NREF | C1PREF | $\overline{\text{C1WU}}$ | 1111 1111 | uuuu uuuu |
| N/A | OPTION | $\overline{\text{GPWU}}$ | $\overline{\text{GPPU}}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| N/A | TRISGPIO(1) | — | — | I/O Control Register | | | | | | ---- 1111 | --11 1111 |

**Legend:** Shaded cells not used by Timer0, – = unimplemented, x = unknown, u = unchanged.

**Note 1:** The TRIS of the T0CKI pin is overridden when T0CS = 1.

**2:** For PIC12F510.

**3:** For PIC16F506.

**REGISTER 7-2: CM1CON0: COMPARATOR C1 CONTROL REGISTER (PIC16F506)**

| R-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| C1OUT | $\overline{\text{C1OUTEN}}$ | C1POL | $\overline{\text{C1T0CS}}$ | C1ON | C1NREF | C1PREF | $\overline{\text{C1WU}}$ |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **C1OUT:** Comparator Output bit
1 = VIN+ > VIN-
0 = VIN+ < VIN-

bit 6 **$\overline{\text{C1OUTEN}}$:** Comparator Output Enable bit(1), (2)
1 = Output of comparator is NOT placed on the C1OUT pin
0 = Output of comparator is placed in the C1OUT pin

bit 5 **C1POL:** Comparator Output Polarity bit(2)
1 = Output of comparator is not inverted
0 = Output of comparator is inverted

bit 4 **$\overline{\text{C1T0CS}}$:** Comparator TMR0 Clock Source bit(2)
1 = TMR0 clock source selected by T0CS control bit
0 = Comparator output used as TMR0 clock source

bit 3 **C1ON:** Comparator Enable bit
1 = Comparator is on
0 = Comparator is off

bit 2 **C1NREF:** Comparator Negative Reference Select bit(2)
1 = C1IN- pin
0 = 0.6V internal reference

bit 1 **C1PREF:** Comparator Positive Reference Select bit(2)
1 = C1IN+ pin
0 = C1IN- pin

bit 0 **$\overline{\text{C1WU}}$:** Comparator Wake-up On Change Enable bit(2)
1 = Wake-up On Comparator Change is disabled
0 = Wake-up On Comparator Change is enabled

**Note 1:** Overrides T0CS bit for TRIS control of RB2.
**2:** When comparator is turned on, these control bits assert themselves. Otherwise, the other registers have precedence.

## 9.0 ANALOG-TO-DIGITAL (A/D) CONVERTER

The A/D Converter allows conversion of an analog signal into an 8-bit digital signal.

### 9.1 Clock Divisors

The ADC has 4 clock source settings ADCS<1:0>. There are 3 divisor values 16, 8 and 4. The fourth setting is INTOSC with a divisor of 4. These settings will allow a proper conversion when using an external oscillator at speeds from 20 MHz to 350 kHz. Using an external oscillator at a frequency below 350 kHz (TAD > 50 μs) requires the ADC oscillator setting to be INTOSC/4 for valid ADC results.

The ADC requires 13 TAD periods to complete a conversion. The divisor values do not affect the number of TAD periods required to perform a conversion. The divisor values determine the length of the TAD period.

When the ADCS<1:0> bits are changed while an ADC conversion is in process, the new ADC clock source will not be selected until the next conversion is started. This clock source selection will be lost when the device enters Sleep.

#### 9.1.1 VOLTAGE REFERENCE

There is no external voltage reference for the ADC. The ADC reference voltage will always be VDD.

#### 9.1.2 ANALOG MODE SELECTION

The ANS<1:0> bits are used to configure pins for analog input. Upon any Reset, ANS<1:0> defaults to 11. This configures pins AN0, AN1 and AN2 as analog inputs. Pins configured as analog inputs are not available for digital output. Users should not change the ANS bits while a conversion is in process. ANS bits are active regardless of the condition of ADON.

#### 9.1.3 ADC CHANNEL SELECTION

The CHS bits are used to select the analog channel to be sampled by the ADC. The CHS<1:0> bits can be changed at any time without adversely effecting a conversion. To acquire an analog signal the CHS<1:0> selection must match one of the pin(s) selected by the ANS<1:0> bits. When the ADC is on (ADON = 1) and a channel is selected that is also being used by the comparator, then both the comparator and the ADC will see the analog voltage on the pin.

| **Note:** | It is the users responsibility to ensure that use of the ADC and comparator simultaneously on the same pin, does not adversely affect the signal being monitored or adversely effect device operation. |
|---|---|

When the CHS<1:0> bits are changed during an ADC conversion, the new channel will not be selected until the current conversion is completed. This allows the current conversion to complete with valid results. All channel selection information will be lost when the device enters Sleep.

**TABLE 9-1: CHANNEL SELECT (ADCS) BITS AFTER AN EVENT**

| Event | ADCS<1:0> |
|---|---|
| $\overline{\text{MCLR}}$ | 11 |
| Conversion completed | CS<1:0> |
| Conversion terminated | CS<1:0> |
| Power-on | 11 |
| Wake from Sleep | 11 |

#### 9.1.4 THE GO/$\overline{\text{DONE}}$ BIT

The GO/$\overline{\text{DONE}}$ bit is used to determine the status of a conversion, to start a conversion and to manually halt a conversion in process. Setting the GO/$\overline{\text{DONE}}$ bit starts a conversion. When the conversion is complete, the ADC module clears the GO/$\overline{\text{DONE}}$ bit. A conversion can be terminated by manually clearing the GO/$\overline{\text{DONE}}$ bit while a conversion is in process. Manual termination of a conversion may result in a partially converted result in ADRES.

The GO/$\overline{\text{DONE}}$ bit is cleared when the device enters Sleep, stopping the current conversion. The ADC does not have a dedicated oscillator, it runs off of the instruction clock. Therefore, no conversion can occur in sleep.

The GO/$\overline{\text{DONE}}$ bit cannot be set when ADON is clear.

### 9.1.6 ANALOG CONVERSION RESULT REGISTER

The ADRES register contains the results of the last conversion. These results are present during the sampling period of the next analog conversion process. After the sampling period is over, ADRES is cleared (= 0). A 'leading one' is then right shifted into the ADRES to serve as an internal conversion complete bit. As each bit weight, starting with the MSB, is converted, the leading one is shifted right and the converted bit is stuffed into ADRES. After a total of 9 right shifts of the 'leading one' have taken place, the conversion is complete; the 'leading one' has been shifted out and the GO/$\overline{\text{DONE}}$ bit is cleared.

If the GO/$\overline{\text{DONE}}$ bit is cleared in software during a conversion, the conversion stops. The data in ADRES is the partial conversion result. This data is valid for the bit weights that have been converted. The position of the 'leading one' determines the number of bits that have been converted. The bits that were not converted before the GO/$\overline{\text{DONE}}$ was cleared are unrecoverable.

**REGISTER 9-1: ADCON0: A/D CONTROL REGISTER (PIC12F510)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ANS1 | ANS0 | ADCS1 | ADCS0 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **ANS<1:0>:** ADC Analog Input Pin Select bits[1), (2)]
- 00 = No pins configured for analog input
- 01 = AN2 configured as an analog input
- 10 = AN2 and AN0 configured as analog inputs
- 11 = AN2, AN1 and AN0 configured as analog inputs

bit 5-4 **ADCS<1:0>:** ADC Conversion Clock Select bits
- 00 = FOSC/16
- 01 = FOSC/8
- 10 = FOSC/4
- 11 = INTOSC/4

bit 3-2 **CHS<1:0>:** ADC Channel Select bits
- 00 = Channel AN0
- 01 = Channel AN1
- 10 = Channel AN2
- 11 = 0.6V absolute voltage reference

bit 1 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit[(4)]
- 1 = ADC conversion in progress. Setting this bit starts an ADC conversion cycle. This bit is automatically cleared by hardware when the ADC is done converting.
- 0 = ADC conversion completed/not in progress. Manually clearing this bit while a conversion is in process terminates the current conversion.

bit 0 **ADON:** ADC Enable bit
- 1 = ADC module is operating
- 0 = ADC module is shut-off and consumes no power

**Note 1:** When the ANS bits are set, the channels selected will automatically be forced into Analog mode, regardless of the pin function previously defined. The only exception to this is the comparator, where the analog input to the comparator and the ADC will be active at the same time. It is the users responsibility to ensure that the ADC loading on the comparator input does not affect their application.

**2:** The ANS<1:0> bits are active regardless of the condition of ADON.

**3:** CHS<1:0> bits default to 11 after any Reset.

**4:** If the ADON bit is clear, the GO/$\overline{\text{DONE}}$ bit cannot be set.

## 10.3 Reset

The device differentiates between various kinds of Reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Time-out Reset during normal operation
- WDT Time-out Reset during Sleep
- Wake-up from Sleep Reset on pin change
- Wake-up from Sleep Reset on comparator change

Some registers are not reset in any way, they are unknown on POR and unchanged in any other Reset. Most other registers are reset to "Reset state" on Power-on Reset (POR), $\overline{\text{MCLR}}$, WDT or Wake-up from Sleep Reset on pin change or wake-up from Sleep Reset on comparator change. The exceptions are $\overline{\text{TO}}$, $\overline{\text{PD}}$, CWUF and RBWUF/GPWUF bits. They are set or cleared differently in different Reset situations. These bits are used in software to determine the nature of Reset. See Table 10-4 for a full description of Reset states of all registers.

**TABLE 10-3: RESET CONDITIONS FOR REGISTERS – PIC12F510**

| Register | Address | Power-on Reset | $\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up On Pin Change, Wake-up on Comparator Change |
|---|---|---|---|
| W | — | qqqq qqqu(1) | qqqq qqqu(1) |
| INDF | 00h | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h | xxxx xxxx | uuuu uuuu |
| PCL | 02h | 1111 1111 | 1111 1111 |
| STATUS | 03h | 0001 1xxx | qq0q quuu(2) |
| FSR | 04h | 110x xxxx | 11uu uuuu |
| OSCCAL | 05h | 1111 111- | uuuu uuu- |
| GPIO | 06h | --xx xxxx | --uu uuuu |
| CM1CON0 | 07h | 1111 1111 | uuuu uuuu |
| ADCON0 | 08h | 1111 1100 | uu11 1100 |
| ADRES | 09h | xxxx xxxx | uuuu uuuu |
| OPTION | — | 1111 1111 | 1111 1111 |
| TRISIO | — | --11 1111 | --11 1111 |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition.

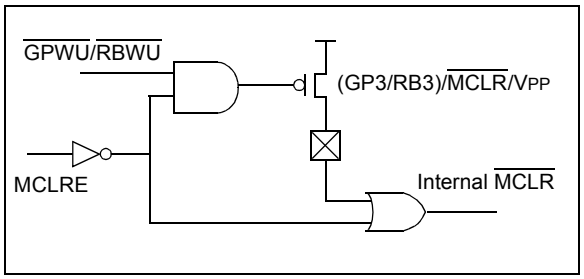
**Note 1:** Bits <7:2> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.

**2:** See Table 10-5 for Reset value for specific conditions.

### 10.3.1 MCLR ENABLE

This Configuration bit, when unprogrammed (left in the '1' state), enables the external MCLR function. When programmed, the MCLR function is tied to the internal VDD and the pin is assigned to be a I/O. See Figure 10-6.

**FIGURE 10-6: MCLR SELECT**




## 10.4 Power-on Reset (POR)

The PIC12F510/16F506 devices incorporate an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. The POR is active regardless of the state of the MCLR enable bit. An internal weak pull-up resistor is implemented using a transistor (refer to Table 13-3 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create an external Power-on Reset. A maximum rise time for VDD is specified. See **Section 13.0 "Electrical Characteristics"** for details.

When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the devices must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 10-7.

The Power-on Reset circuit and the Device Reset Timer (see **Section 10.5 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects MCLR, internal or external, to be high. After the time-out period, it will reset the Reset latch and thus end the on-chip Reset signal.

A power-up example where MCLR is held low is shown in Figure 10-8. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of Reset TDRT msec after MCLR goes high.

In Figure 10-9, the on-chip Power-on Reset feature is being used (MCLR and VDD are tied together or the pin is programmed to be (GP3/RB3). The VDD is stable before the Start-up timer times out and there is no problem in getting a proper Reset. However, Figure 10-10 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that MCLR is high and when MCLR and VDD actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 10-9).

| | |
|---|---|
| **Note:** | When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met. |

For additional information, refer to Application Notes AN522, *"Power-Up Considerations"* (DS00522) and AN607, *"Power-up Trouble Shooting"* (DS00607).

## 10.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (TO, PD, GPWUF/RBWUF)

The $\overline{TO}$, $\overline{PD}$ and (GPWUF/RBWUF) bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) Reset.

**TABLE 10-8: $\overline{TO}$/$\overline{PD}$/(GPWUF/RBWUF) STATUS AFTER RESET**

| CWUF | GPWUF/ RBWUF | $\overline{TO}$ | $\overline{PD}$ | Reset Caused By |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | WDT wake-up from Sleep |
| 0 | 0 | 0 | u | WDT time-out (not from Sleep) |
| 0 | 0 | 1 | 0 | $\overline{MCLR}$ wake-up from Sleep |
| 0 | 0 | 1 | 1 | Power-up |
| 0 | 0 | u | u | $\overline{MCLR}$ not during Sleep |
| 0 | 1 | 1 | 0 | Wake-up from Sleep on pin change |
| 1 | 0 | 1 | 0 | Wake-up from Sleep on comparator change |

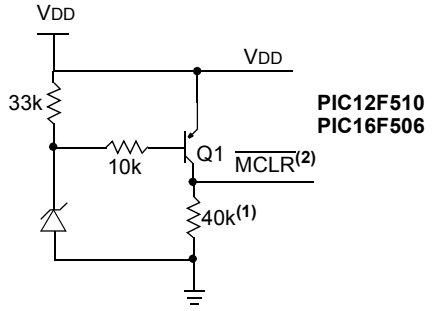
**Legend:** u = unchanged

## 10.8 Reset on Brown-out

A brown-out is a condition where device power ($V_{DD}$) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

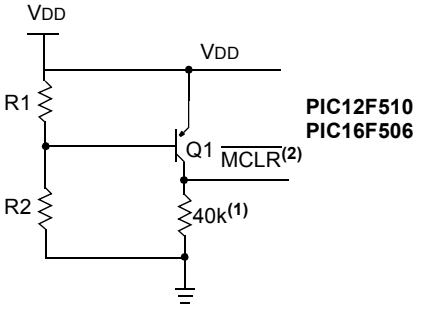
To reset PIC12F510/16F506 devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 10-12 and Figure 10-13.

**FIGURE 10-12: BROWN-OUT PROTECTION CIRCUIT 1**




**Note 1:** This circuit will activate Reset when $V_{DD}$ goes below Vz + 0.7V (where Vz = Zener voltage).
**2:** Pin must be configured as $\overline{MCLR}$.

**FIGURE 10-13: BROWN-OUT PROTECTION CIRCUIT 2**

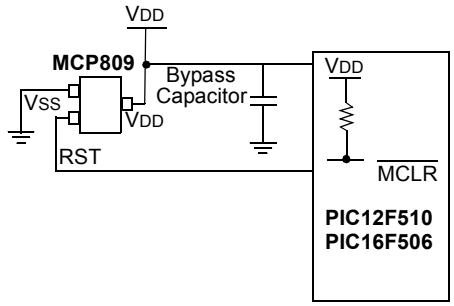



**Note 1:** This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when $V_{DD}$ is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

**2:** Pin must be configured as $\overline{MCLR}$.

**FIGURE 10-14: BROWN-OUT PROTECTION CIRCUIT 3**




**Note:** This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. There are 7 different trip point selections to accommodate 5V to 3V systems.

| DECF | Decrement f |
|---|---|
| Syntax: | [ *label* ] DECF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) – 1 → (dest) |
| Status Affected: | Z |
| Description: | Decrement register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’. |

| DECFSZ | Decrement f, Skip if 0 |
|---|---|
| Syntax: | [ *label* ] DECFSZ f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) – 1 → d; skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register ‘f’ are decremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.<br>If the result is ‘0’, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction. |

| GOTO | Unconditional Branch |
|---|---|
| Syntax: | [ *label* ] GOTO k |
| Operands: | $0 \le k \le 511$ |
| Operation: | k → PC<8:0>;<br>STATUS <6:5> → PC<10:9> |
| Status Affected: | None |
| Description: | GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS <6:5>. GOTO is a two-cycle instruction. |

| INCF | Increment f |
|---|---|
| Syntax: | [ *label* ] INCF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) + 1 → (dest) |
| Status Affected: | Z |
| Description: | The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. |

| INCFSZ | Increment f, Skip if 0 |
|---|---|
| Syntax: | [ *label* ] INCFSZ f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) + 1 → (dest), skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.<br>If the result is ‘0’, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction. |

| IORLW | Inclusive OR literal with W |
|---|---|
| Syntax: | [ *label* ] IORLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | (W) .OR. (k) → (W) |
| Status Affected: | Z |
| Description: | The contents of the W register are OR’ed with the eight-bit literal ‘k’. The result is placed in the W register. |

## 13.2 DC Characteristics: PIC12F510/16F506 (Extended)

| DC Characteristics | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 2.0 | | 5.5 | V | See **Figure 14-1** |
| D002 | VDR | **RAM Data Retention Voltage(2)** | — | 1.5* | — | V | Device in Sleep mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See **Section 10.4 "Power-on Reset (POR)"** for details |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See **Section 10.4 "Power-on Reset (POR)"** for details |
| D010 | IDD | **Supply Current(3,4)** | —<br>— | 175<br>0.625 | 275<br>1.1 | µA<br>mA | FOSC = 4 MHz, VDD = 2.0V<br>FOSC = 4 MHz, VDD = 5.0V |
| | | | —<br>— | 250<br>1.0 | 450<br>1.5 | µA<br>mA | FOSC = 8 MHz, VDD = 2.0V<br>FOSC = 8 MHz, VDD = 5.0V |
| | | | — | 1.4 | 2.0 | mA | FOSC = 20 MHz, VDD = 5.0V |
| | | | —<br>— | 11<br>38 | 16<br>54 | µA<br>µA | FOSC = 32 kHz, VDD = 2.0V<br>FOSC = 32 kHz, VDD = 5.0V |
| D020 | IPD | **Power-down Current(5)** | —<br>— | 0.1<br>0.35 | 9.0<br>15.0 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D022 | IWDT | **WDT Current(5)** | —<br>— | 1.0<br>7.0 | 18<br>22 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D023 | ICMP | **Comparator Current(5)** | —<br>— | 15<br>55 | 25<br>75 | µA<br>µA | VDD = 2.0V (per comparator)<br>VDD = 5.0V (per comparator) |
| D022 | ICVREF | **CVREF Current(5)** | —<br>— | 30<br>75 | 65<br>135 | µA<br>µA | VDD = 2.0V (high range)<br>VDD = 5.0V (high range) |
| D023 | IFVR | **Internal 0.6V Fixed Voltage Reference Current(5)** | —<br>— | 85<br>175 | 130<br>220 | µA<br>µA | VDD = 2.0V (0.6V reference and 1 comparator enabled)<br>VDD = 5.0V (0.6V reference and 1 comparator enabled) |
| D024 | ΔIAD | **A/D Conversion Current(5)** | — | 120 | 150 | µA | 2.0V |
| | | | — | 200 | 250 | µA | 5.0V |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

**4:** The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

**5:** For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

**6:** Does not include current through REXT. The current through the resistor can be estimated by the formula: I = VDD/2REXT (mA) with REXT in kΩ.

**TABLE 13-6: TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(2), (3) | — | — | 100* | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)(2) | 50 | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | 20 | — | — | ns |
| 20 | TioR | Port output rise time(2), (3) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2), (3) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

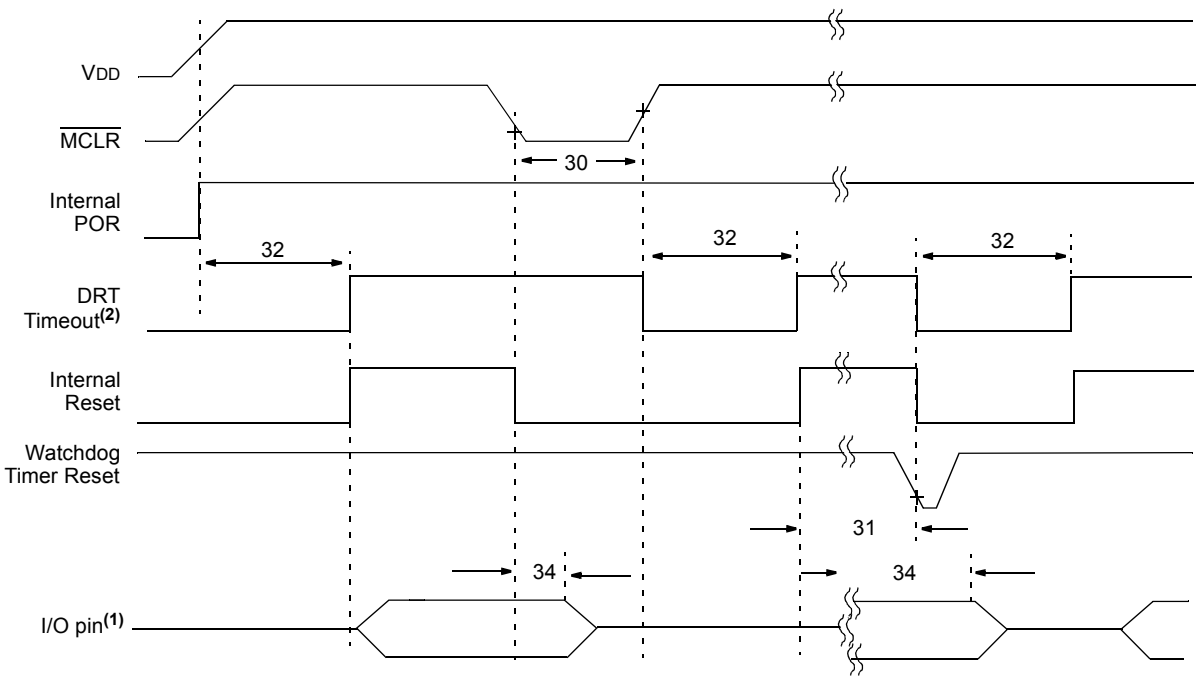
** These parameters are design targets and are not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** Measurements are taken in EXTRC mode.

**3:** See Figure 13-5 for loading conditions.

**FIGURE 13-8: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER TIMING**



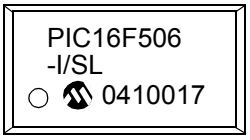

**Note 1:** I/O pins must be taken out of High-Impedance mode by enabling the output drivers in software.

**2:** Runs in MCLR or WDT Reset only in XT, LP and HS modes.

### 15.2 Package Marking Information (Cont'd)

14-Lead SOIC (3.90 mm)

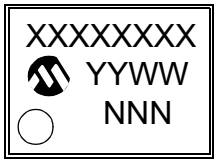

Example



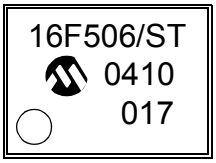

8-Lead MSOP


Example


14-Lead TSSOP (4.4 mm)




Example



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