Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	67 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f506t-i-sl

2.0 PIC12F510/16F506 DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC12F510/16F506 Product Identification System at the back of this data sheet to specify the correct part number.

2.1 Quick Turn Programming (QTP) Devices

Microchip offers a QTP programming service for factory production orders. This service is made available for users who choose not to program medium-to-high quantity units and whose code patterns have stabilized. The devices are identical to the Flash devices, but with all Flash locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.2 Serialized Quick Turn Programming^{SM} (SQTP^{SM}) Devices

Microchip offers a unique programming service, where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry code, password or ID number.

TABLE 3-3: PIN DESCRIPTIONS – PIC16F506

Name	Function	Input Type	Output Type	Description
RB0/AN0/C1IN+/ICSPDAT	RB0	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	AN0	AN	—	ADC channel input.
	C1IN+	AN	—	Comparator 1 input.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming data pin.
RB1/AN1/C1IN-/ICSPCLK	RB1	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	AN1	AN	—	ADC channel input.
	C1IN-	AN	—	Comparator 1 input.
	ICSPCLK	ST	—	In-Circuit Serial Programming clock pin.
RB2/AN2/C1OUT	RB2	TTL	CMOS	Bidirectional I/O port.
	AN2	AN	—	ADC channel input.
	C1OUT	—	CMOS	Comparator 1 output.
RB3/$\overline{\text{MCLR}}$/VPP	RB3	TTL	—	Standard TTL input. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	$\overline{\text{MCLR}}$ input – weak pull-up always enabled in this mode.
	VPP	HV	—	Programming voltage input.
RB4/OSC2/CLKOUT	RB4	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	OSC2	—	XTAL	XTAL oscillator output pin.
	CLKOUT	—	CMOS	EXTRC/INTOSC CLKOUT pin (FOSC/4).
RB5/OSC1/CLKIN	RB5	TTL	CMOS	Bidirectional I/O port.
	OSC1	XTAL	—	XTAL oscillator input pin.
	CLKIN	ST	—	EXTRC/EC Schmitt Trigger input.
RC0/C2IN+	RC0	TTL	CMOS	Bidirectional I/O port.
	C2IN+	AN	—	Comparator 2 input.
RC1/C2IN-	RC1	TTL	CMOS	Bidirectional I/O port.
	C2IN-	AN	—	Comparator 2 input.
RC2/CVREF	RC2	TTL	CMOS	Bidirectional I/O port.
	CVREF	—	AN	Programmable Voltage Reference output.
RC3	RC3	TTL	CMOS	Bidirectional I/O port.
RC4/C2OUT	RC4	TTL	CMOS	Bidirectional I/O port.
	C2OUT	—	CMOS	Comparator 2 output.
RC5/T0CKI	RC5	TTL	CMOS	Bidirectional I/O port.
	T0CKI	ST	—	Timer0 clock input.
VDD	VDD	P	—	Positive supply for logic and I/O pins.
VSS	VSS	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog Voltage, HV = High Voltage

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (see Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY – PIC12F510

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset
N/A	TRIS	I/O Control Registers (TRISGPIO)								`--11 1111`
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT Prescaler								`1111 1111`
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								`xxxx xxxx`
01h	TMR0	Timer0 Module Register								`xxxx xxxx`
02h[(1)]	PCL	Low Order 8 bits of PC								`1111 1111`
03h	STATUS	GPWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	`0001 1xxx`
04h	FSR	Indirect Data Memory Address Pointer								`110x xxxx`
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	`1111 111-`
06h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	`--xx xxxx`
07h	CM1CON0	C1OUT	$\overline{C1OUTEN}$	C1POL	$\overline{C1T0CS}$	C1ON	C1NREF	C1PREF	$\overline{C1WU}$	`1111 1111`
08h	ADCON0	ANS1	ANS0	ADCS1	ADCS0	CHS1	CHS0	GO/$\overline{DONE}$	ADON	`1111 1100`
09h	ADRES	ADC Conversion Result								`xxxx xxxx`

Legend: `x` = unknown, `u` = unchanged, – = unimplemented, read as ‘`0`’ (if applicable). Shaded cells = unimplemented or unused.

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.6 “Program Counter”** for an explanation of how to access these bits.

TABLE 4-2: SPECIAL FUNCTION REGISTER SUMMARY – PIC16F506

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset
N/A	TRIS	I/O Control Registers (TRISB, TRISC)								`--11 1111`
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT Prescaler								`1111 1111`
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								`xxxx xxxx`
01h	TMR0	Timer0 Module Register								`xxxx xxxx`
02h(1)	PCL	Low Order 8 bits of PC								`1111 1111`
03h	STATUS	RBWUF	CWUF	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	`0001 1xxx`
04h	FSR	Indirect Data Memory Address Pointer								`100x xxxx`
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	`1111 111-`
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	`--xx xxxx`
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	`--xx xxxx`
08h	CM1CON0	C1OUT	$\overline{C1OUTEN}$	C1POL	$\overline{C1T0CS}$	C1ON	C1NREF	C1PREF	$\overline{C1WU}$	`1111 1111`
09h	ADCON0	ANS1	ANS0	ADCS1	ADCS0	CHS1	CHS0	GO/$\overline{DONE}$	ADON	`1111 1100`
0Ah	ADRES	ADC Conversion Result								`xxxx xxxx`
0Bh	CM2CON0	C2OUT	$\overline{C2OUTEN}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{C2WU}$	`1111 1111`
0Ch	VRCON	VREN	VROE	VRR	—(2)	VR3	VR2	VR1	VR0	`0011 1111`

Legend: `x` = unknown, `u` = unchanged, – = unimplemented, read as '`0`' (if applicable). Shaded cells = unimplemented or unused.

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.6 "Program Counter"** for an explanation of how to access these bits.

2: Unimplemented bit VRCON<4> read as '`1`'.

4.3 STATUS Register

This register contains the arithmetic status of the ALU, the Reset status and the page preselect bit.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS`, will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

Therefore, it is recommended that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register. These instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions which do affect Status bits, see **Section 11.0 "Instruction Set Summary"**.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRISGPIO(1)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISB(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISC(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	OPTION(1)	$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION(2)	$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	T0CS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS(1)	GPWUF	CWUF	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	qq0q quuu(3)
03h	STATUS(2)	RBWUF	CWUF	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	qq0q quuu(3)
06h	GPIO(1)	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
06h	PORTB(2)	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC(2)	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: – = unimplemented read as '0', x = unknown, u = unchanged, q = depends on condition.
Note 1: PIC12F510 only.
2: PIC16F506 only.
3: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

TABLE 5-2: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)

Priority	RB0	RB1	RB2	RB3	RB4	RB5
1	AN0/C1IN+	AN1/C1IN-	AN2	Input/$\overline{\text{MCLR}}$	OSC2/CLKOUT	OSC1/CLKIN
2	TRISB	TRISB	C1OUT	—	TRISB	TRISB
3	—	—	TRISB	—	—	—

TABLE 5-3: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC16F506)

Priority	RC0	RC1	RC2	RC3	RC4	RC5
1	C2IN+	C2IN-	CVREF	TRISC	C2OUT	T0CKI
2	TRISC	TRISC	TRISC	—	TRISC	TRISC

TABLE 5-4: I/O PIN FUNCTION ORDER OF PRECEDENCE (PIC12F510)

Priority	GP0	GP1	GP2	GP3	GP4	GP5
1	AN0/C1IN+	AN1/C1IN-	AN2	Input/$\overline{\text{MCLR}}$	OSC2	OSC1/CLKIN
2	TRISIO	TRISIO	C1OUT	—	TRISIO	TRISIO
3	—	—	T0CKI	—	—	—
4	—	—	TRISIO	—	—	—

FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

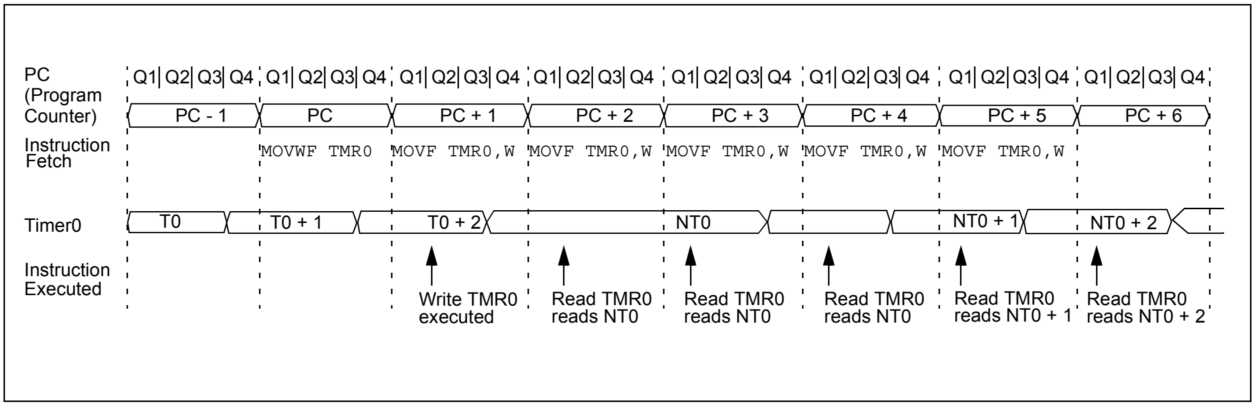


FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

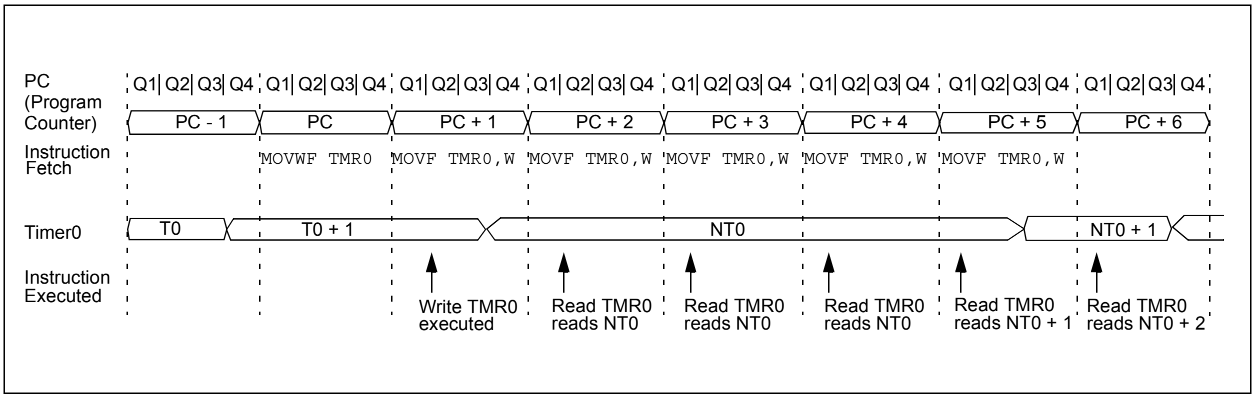


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
01h	TMR0	Timer0 – 8-bit Real-Time Clock/Counter								xxxx xxxx	uuuu uuuu
07h	CM1CON0[2]	C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$	1111 1111	uuuu uuuu
08h	CM1CON0[3]	C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$	1111 1111	uuuu uuuu
N/A	OPTION	$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	TRISGPIO[1]	—	—	I/O Control Register						---- 1111	--11 1111

Legend: Shaded cells not used by Timer0, – = unimplemented, x = unknown, u = unchanged.
Note 1: The TRIS of the T0CKI pin is overridden when T0CS = 1.
2: For PIC12F510.
3: For PIC16F506.

6.1 Using Timer0 With An External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

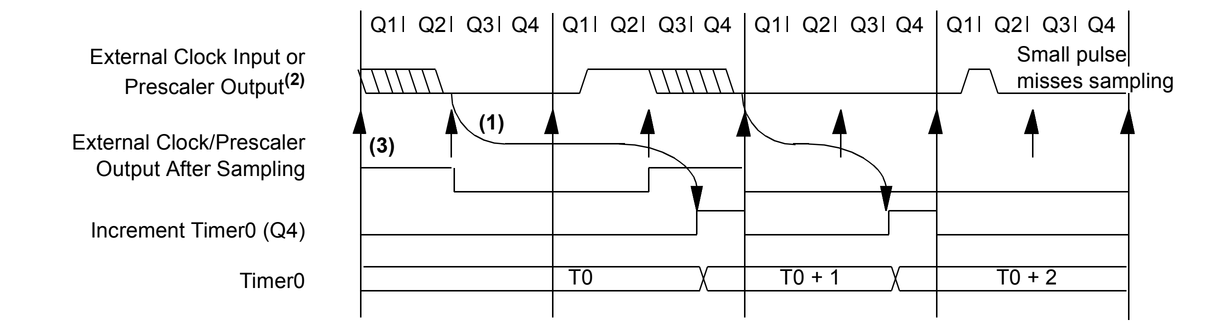
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of an external clock with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI or the comparator output to be high for at least 2TOSC (and a small RC delay of 2Tt0H) and low for at least 2TOSC (and a small RC delay of 2Tt0H). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI or the comparator output to have a period of at least 4TOSC (and a small RC delay of 4Tt0H) divided by the prescaler value. The only requirement on T0CKI or the comparator output high and low time is that they do not violate the minimum pulse width requirement of Tt0H. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3TOSC to 7TOSC. (Duration of Q = TOSC). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4TOSC max.

2: External clock if no prescaler selected; prescaler output otherwise.

3: The arrows indicate the points in time where sampling occurs.

6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (see Figure 10-12). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet.

Note:	The prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1, x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a Reset, the prescaler contains all ‘`0`’s.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0 → WDT)

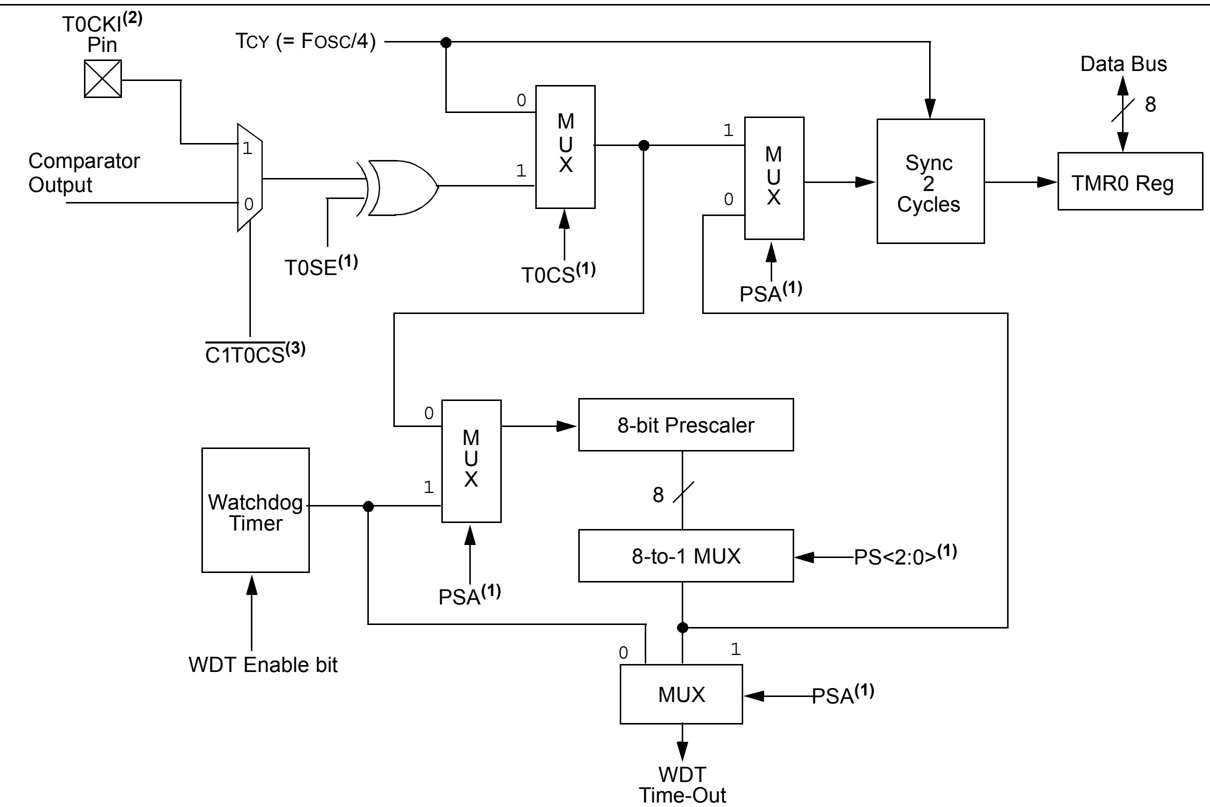
```
CLRWDT                  ;Clear WDT
CLRF   TMR0             ;Clear TMR0 & Prescaler
MOVLW  '00xx1111'b      ;These 3 lines (5, 6, 7)
OPTION                  ;are required only if
                        ;desired
CLRWDT                  ;PS<2:0> are 000 or 001
MOVLW  '00xx1xxx'b      ;Set Postscaler to
OPTION                  ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                  ;Clear WDT and
                        ;prescaler
MOVLW   'xxxx0xxx'      ;Select TMR0, new
                        ;prescale value and
                        ;clock source
OPTION
```

FIGURE 6-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

2: T0CKI is shared with pin GP2 on the PIC12F510 and shared with RC5 on the PIC16F506.

3: Bit $\overline{\text{C1T0CS}}$ is located in the CM1CON0 register.

REGISTER 7-2: CM1CON0: COMPARATOR C1 CONTROL REGISTER (PIC16F506)

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **C1OUT:** Comparator Output bit
1 = VIN+ > VIN-
0 = VIN+ < VIN-

bit 6 **$\overline{\text{C1OUTEN}}$:** Comparator Output Enable bit(1), (2)
1 = Output of comparator is NOT placed on the C1OUT pin
0 = Output of comparator is placed in the C1OUT pin

bit 5 **C1POL:** Comparator Output Polarity bit(2)
1 = Output of comparator is not inverted
0 = Output of comparator is inverted

bit 4 **$\overline{\text{C1T0CS}}$:** Comparator TMR0 Clock Source bit(2)
1 = TMR0 clock source selected by T0CS control bit
0 = Comparator output used as TMR0 clock source

bit 3 **C1ON:** Comparator Enable bit
1 = Comparator is on
0 = Comparator is off

bit 2 **C1NREF:** Comparator Negative Reference Select bit(2)
1 = C1IN- pin
0 = 0.6V internal reference

bit 1 **C1PREF:** Comparator Positive Reference Select bit(2)
1 = C1IN+ pin
0 = C1IN- pin

bit 0 **$\overline{\text{C1WU}}$:** Comparator Wake-up On Change Enable bit(2)
1 = Wake-up On Comparator Change is disabled
0 = Wake-up On Comparator Change is enabled

Note 1: Overrides T0CS bit for TRIS control of RB2.

2: When comparator is turned on, these control bits assert themselves. Otherwise, the other registers have precedence.

9.1.5 SLEEP

This ADC does not have a dedicated ADC clock, and therefore, no conversion in Sleep is possible. If a conversion is underway and a Sleep command is executed, the GO/$\overline{\text{DONE}}$ and ADON bit will be cleared. This will stop any conversion in process and power-down the ADC module to conserve power. Due to the nature of the conversion process, the ADRES may contain a partial conversion. At least 1 bit must have been converted prior to Sleep to have partial conversion data in ADRES. The ADCS and CHS bits are reset to their default condition; ANS<1:0> = `11` and CHS<1:0> = `11`.

- For accurate conversions, T_{AD} must meet the following:
- 500 ns < T_{AD} < 50 µs
- T_{AD} = `1`/(F_{OSC}/divisor)

Shaded areas indicate T_{AD} out of range for accurate conversions. If analog input is desired at these frequencies, use INTOSC/4 for the ADC clock source.

TABLE 9-2: T_{AD} FOR ADCS SETTINGS WITH VARIOUS OSCILLATORS

Source	ADCS <1:0>	Divisor	20[(1)] MHz	16[(1)] MHz	8 MHz	4 MHz	1 MHz	500 kHz	350 kHz	200 kHz	100 kHz	32 kHz
INTOSC	`11`	4	—	—	.5 µs	1 µs	—	—	—	—	—	—
FOSC	`10`	4	.2 µs	.25 µs	.5 µs	1 µs	4 µs	8 µs	11 µs	20 µs	40 µs	125 µs
FOSC	`01`	8	.4 µs	.5 µs	1 µs	2 µs	8 µs	16 µs	23 µs	40 µs	80 µs	250 µs
FOSC	`00`	16	.8 µs	1 µs	2 µs	4 µs	16 µs	32 µs	46 µs	80 µs	160 µs	500 µs

Note 1: When operating with external oscillator frequencies of 16 MHz or higher, better ADC performance will result from selection of a suitable F_{OSC} divisor value from Table 9-2 than from use of the INTOSC/4 option for the ADC clock.

TABLE 9-3: EFFECTS OF SLEEP ON ADCON0

	ANS1	ANS0	ADCS1	ADCS0	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
Entering Sleep	Unchanged	Unchanged	`1`	`1`	`1`	`1`	`0`	`0`
Wake or Reset	`1`	`1`	`1`	`1`	`1`	`1`	`0`	`0`

REGISTER 10-2: CONFIG: CONFIGURATION WORD REGISTER (PIC16F506)(1)

—	—	—	—	—	—	—	—
bit 15							bit 8

—	IOSCFS	MCLRE	$\overline{\text{CP}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 7							bit 0

bit 11-7 **Unimplemented**: Read as '1'

bit 6 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz INTOSC speed
0 = 4 MHz INTOSC speed

bit 5 **MCLRE:** Master Clear Enable bit
1 = RB3/$\overline{\text{MCLR}}$ pin functions as $\overline{\text{MCLR}}$
0 = RB3/$\overline{\text{MCLR}}$ pin functions as RB3, $\overline{\text{MCLR}}$ tied internally to V_{DD}

bit 4 **$\overline{\text{CP}}$:** Code Protection bit
1 = Code protection off
0 = Code protection on

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
000 = LP oscillator and 18 ms DRT
001 = XT oscillator and 18 ms DRT
010 = HS oscillator and 18 ms DRT
011 = EC oscillator with RB4 function on RB4/OSC2/CLKOUT and 1.125 ms DRT(2)
100 = INTOSC with RB4 function on RB4/OSC2/CLKOUT and 1.125 ms DRT(2)
101 = INTOSC with CLKOUT function on RB4/OSC2/CLKOUT and 1.125 ms DRT(2)
110 = EXTRC with RB4 function on RB4/OSC2/CLKOUT and 1.125 ms DRT (2)
111 = EXTRC with CLKOUT function on RB4/OSC2/CLKOUT and 1.125 ms DRT(2)

Note 1: Refer to the "*PIC16F506 Memory Programming Specification*" (DS41258) to determine how to access the Configuration Word.

2: It is the responsibility of the application designer to ensure the use of the 1.125 ms (nominal) DRT will result in acceptable operation. Refer to Electrical Specifications for V_{DD} rise time and stability requirements for this mode of operation.

10.5 Device Reset Timer (DRT)

On the PIC12F510/16F506 devices, the DRT runs any time the device is powered up. DRT runs from Reset and varies based on oscillator selection and Reset type (see Table 10-6).

The DRT operates from a free running on-chip oscillator that is separate from INTOSC. The processor is kept in Reset as long as the DRT is active. The DRT delay allows VDD to rise above VDD minimum and for the oscillator to stabilize.

Oscillator circuits, based on crystals or ceramic resonators, require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the devices in a Reset for a set period, as stated in Table 10-6, after $\overline{\text{MCLR}}$ has reached a logic high (VIH $\overline{\text{MCLR}}$) level. Programming (GP3/RB3)/$\overline{\text{MCLR}}$/VPP as $\overline{\text{MCLR}}$ and using an external RC network connected to the $\overline{\text{MCLR}}$ input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the (GP3/RB3)/$\overline{\text{MCLR}}$/VPP pin as a general purpose input.

The DRT delays will vary from chip-to-chip due to VDD, temperature and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out from Sleep. This is particularly important for applications using the WDT to wake from Sleep mode automatically.

Reset sources are POR, $\overline{\text{MCLR}}$, WDT time-out, Wake-up on Pin Change and Wake-up on Comparator Change. See **Section 10.9.2 "Wake-up from Sleep Reset", Notes 1, 2 and 3**.

TABLE 10-6: TYPICAL DRT PERIODS

Oscillator Configuration	POR Reset	Subsequent Resets
LP	18 ms	18 ms
XT	18 ms	18 ms
HS(1)	18 ms	18 ms
EC(1)	1.125 ms	10 μs
INTOSC	1.125 ms	10 μs
EXTRC	1.125 ms	10 μs

Note 1: PIC16F506 only

Note: It is the responsibility of the application designer to ensure the use of the 1.125 ms nominal DRT will result in acceptable operation. Refer to Electrical Specifications for VDD rise time and stability requirements for this mode of operation.

10.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator that does not require any external components. This RC oscillator is separate from the external RC oscillator of the (GP5/RB5)/OSC1/CLKIN pin and the internal 4/8 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a `SLEEP` instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset generates a device Reset.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see **Section 10.1 "Configuration Bits"**). Refer to the PIC12F510/16F506 Programming Specifications to determine how to access the Configuration Word.

10.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a divisor ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst-case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

10.6.2 WDT PROGRAMMING CONSIDERATIONS

The `CLRWDT` instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The `SLEEP` instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

10.12 In-Circuit Serial Programming™ (ICSP™)

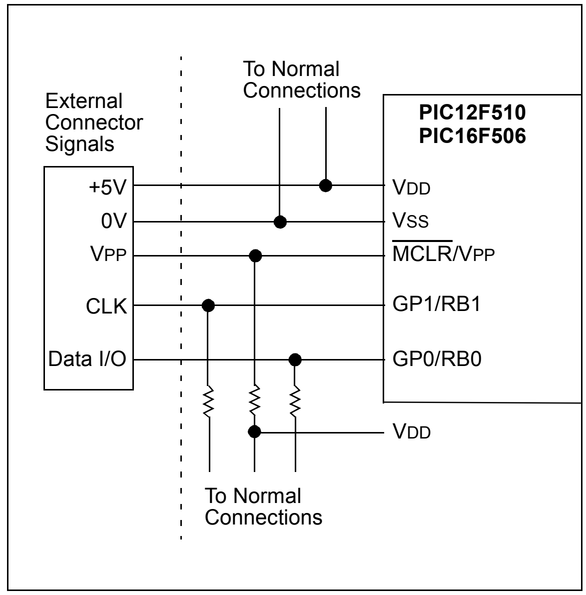
The PIC12F510/16F506 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The devices are placed into a Program/Verify mode by holding the GP1/RB1 and GP0/RB0 pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). GP1/RB1 becomes the programming clock and GP0/RB0 becomes the programming data. Both GP1/RB1 and GP0/RB0 are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is supplied to the device. Depending on the command and if the command was a Load or a Read, 14 bits of program data are then supplied to or from the device. For complete details of serial programming, please refer to the PIC12F510/16F506 Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 10-15.

FIGURE 10-15: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



12.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK™ Object Linker/
    MPLIB™ Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
  - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

12.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

13.1 DC Characteristics: PIC12F510/16F506 (Industrial)

DC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 40°C ≤ TA ≤ +85°C (industrial)				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	See **Figure 14-1**
D002	VDR	**RAM Data Retention Voltage(2)**	—	1.5*	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See **Section 10.4 "Power-on Reset (POR)"** for details
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See **Section 10.4 "Power-on Reset (POR)"** for details
D010	IDD	**Supply Current(3,4)**	— —	175 0.625	275 1.1	μA mA	FOSC = 4 MHz, VDD = 2.0V FOSC = 4 MHz, VDD = 5.0V
			— —	250 1.0	450 1.5	μA mA	FOSC = 8 MHz, VDD = 2.0V FOSC = 8 MHz, VDD = 5.0V
			—	1.4	2.0	mA	FOSC = 20 MHz, VDD = 5.0V
			— —	11 38	15 52	μA μA	FOSC = 32 kHz, VDD = 2.0V FOSC = 32 kHz, VDD = 5.0V
D020	IPD	**Power-down Current(5)**	— —	0.1 0.35	1.2 2.4	μA μA	VDD = 2.0V VDD = 5.0V
D022	IWDT	**WDT Current(5)**	— —	1.0 7.0	3.0 16.0	μA μA	VDD = 2.0V VDD = 5.0V
D023	ICMP	**Comparator Current(5)**	— —	15 55	22 67	μA μA	VDD = 2.0V (per comparator) VDD = 5.0V (per comparator)
D022	ICVREF	**CVREF Current(5)**	— —	30 75	60 125	μA μA	VDD = 2.0V (high range) VDD = 5.0V (high range)
D023	IFVR	**Internal 0.6V Fixed Voltage Reference Current(5)**	— —	85 175	120 205	μA μA	VDD = 2.0V (0.6V reference and 1 comparator enabled) VDD = 5.0V (0.6V reference and 1 comparator enabled)
D024	ΔIAD	**A/D Conversion Current(5)**	—	120	150	μA	2.0V
			—	200	250	μA	5.0V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

4: The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

5: For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

6: Does not include current through REXT. The current through the resistor can be estimated by the formula:
I = VDD/2REXT (mA) with REXT in kΩ.

FIGURE 14-4: COMPARATOR IPD vs. VDD (COMPARATOR ENABLED)

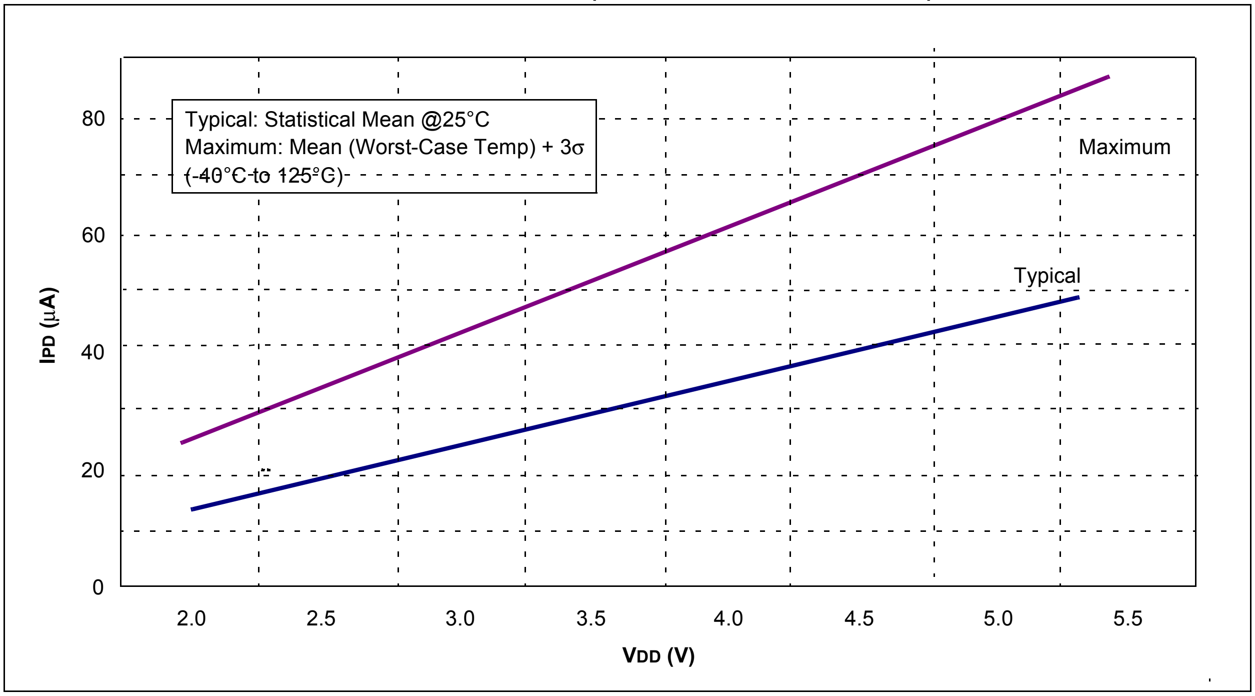


FIGURE 14-5: TYPICAL WDT IPD vs. VDD

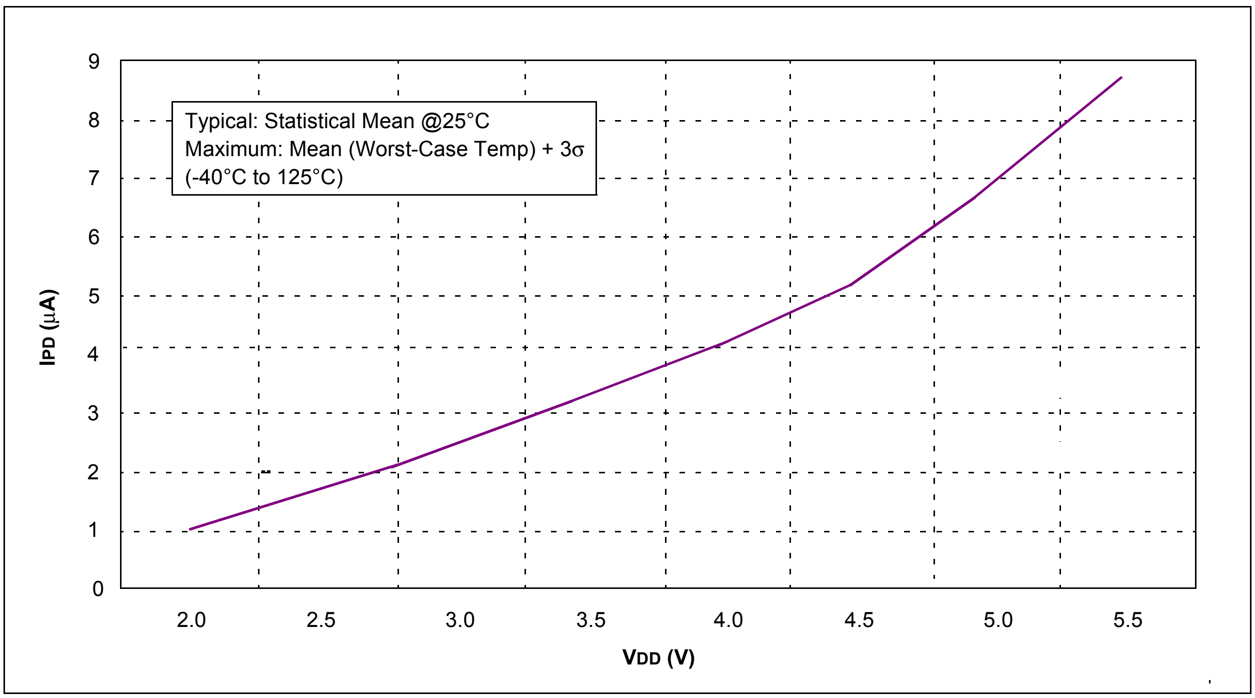


FIGURE 14-8: V_{OL} vs. I_{OL} OVER TEMPERATURE (V_{DD} = 3.0V)

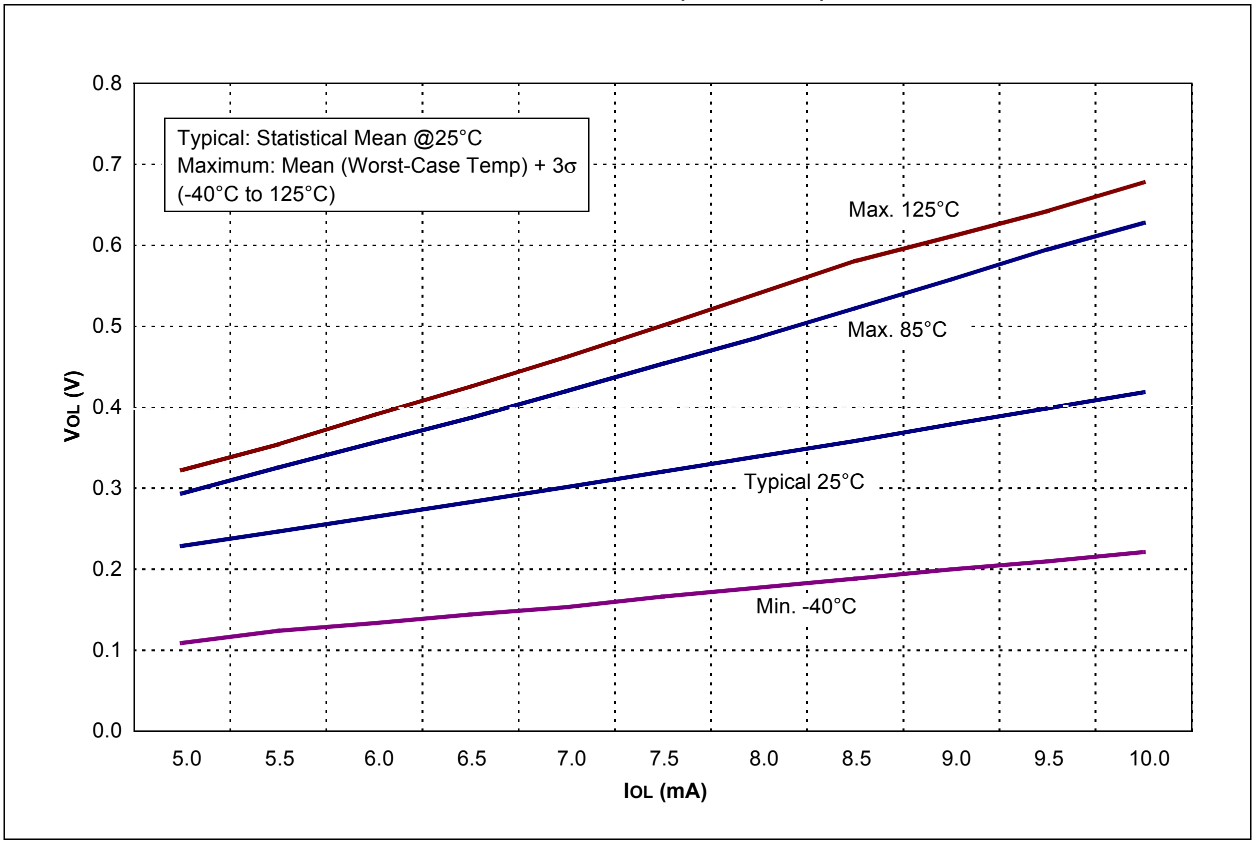


FIGURE 14-9: V_{OL} vs. I_{OL} OVER TEMPERATURE (V_{DD} = 5.0V)

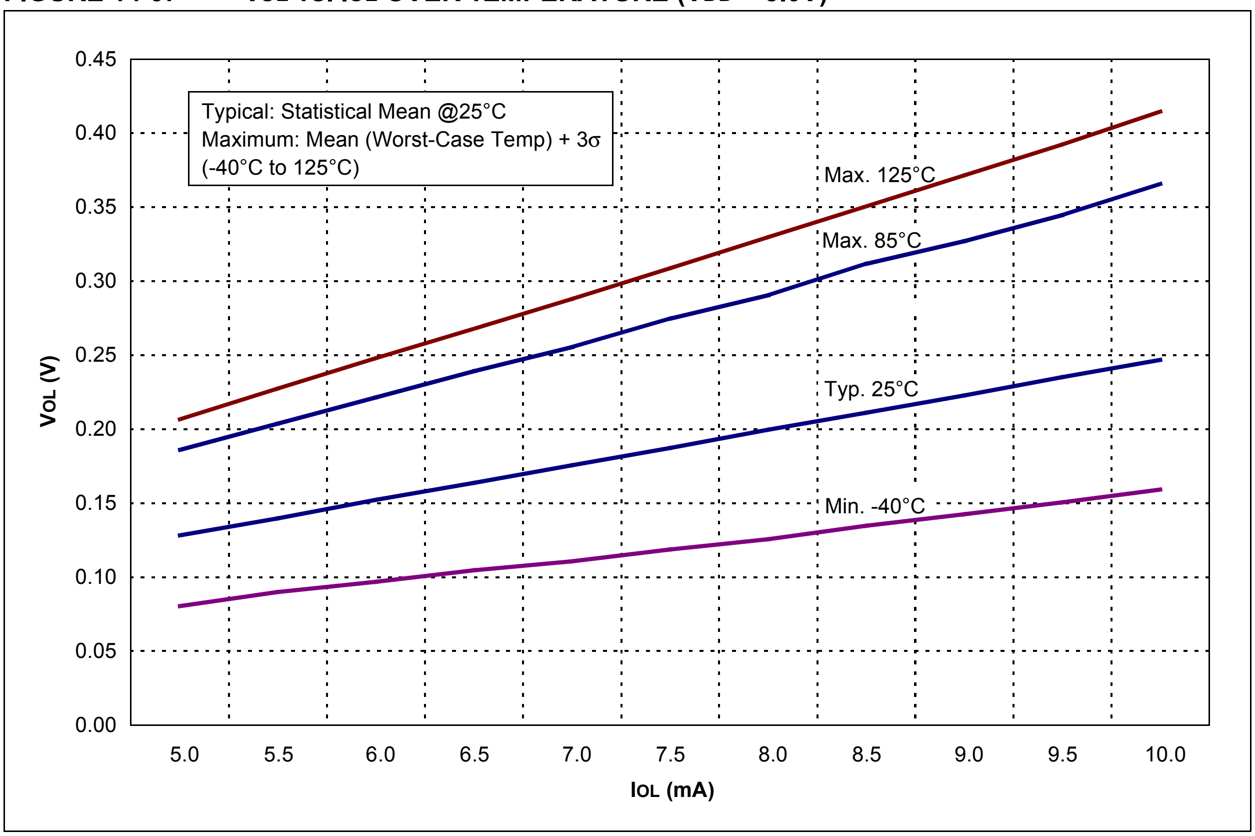


FIGURE 14-12: TTL INPUT THRESHOLD VIN vs. VDD

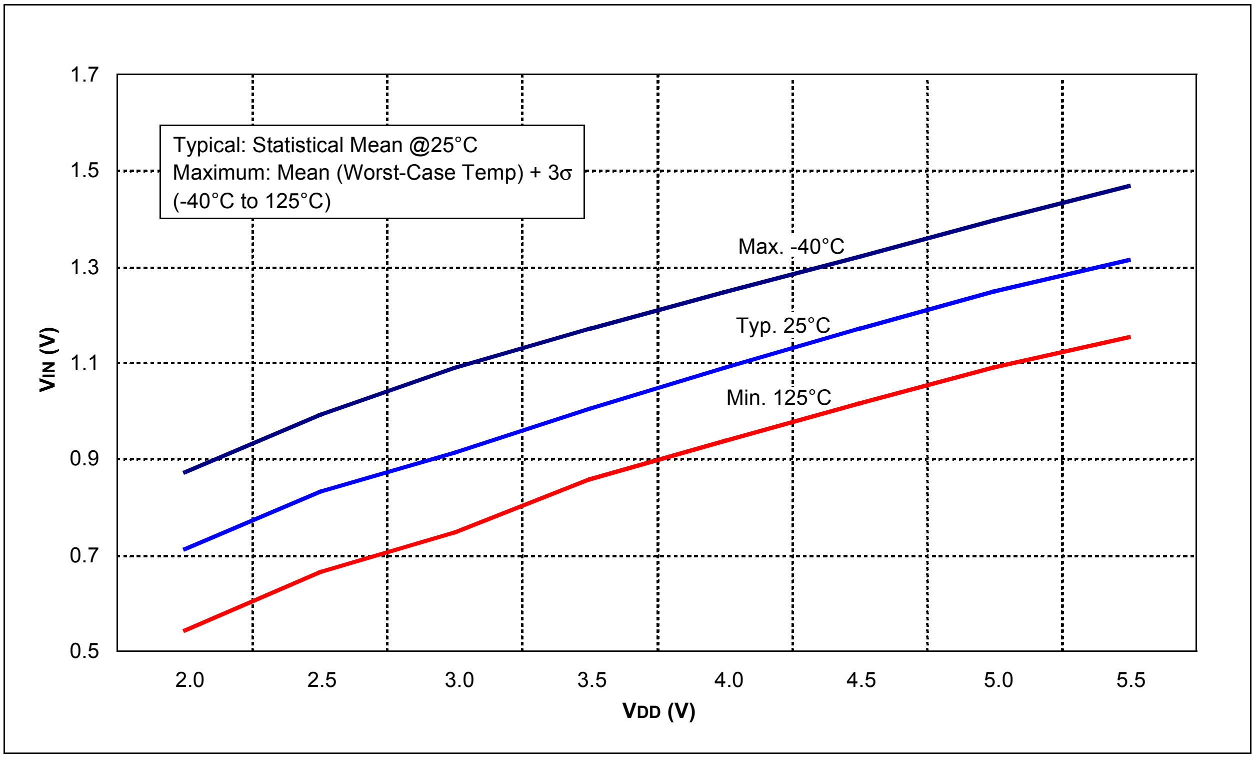
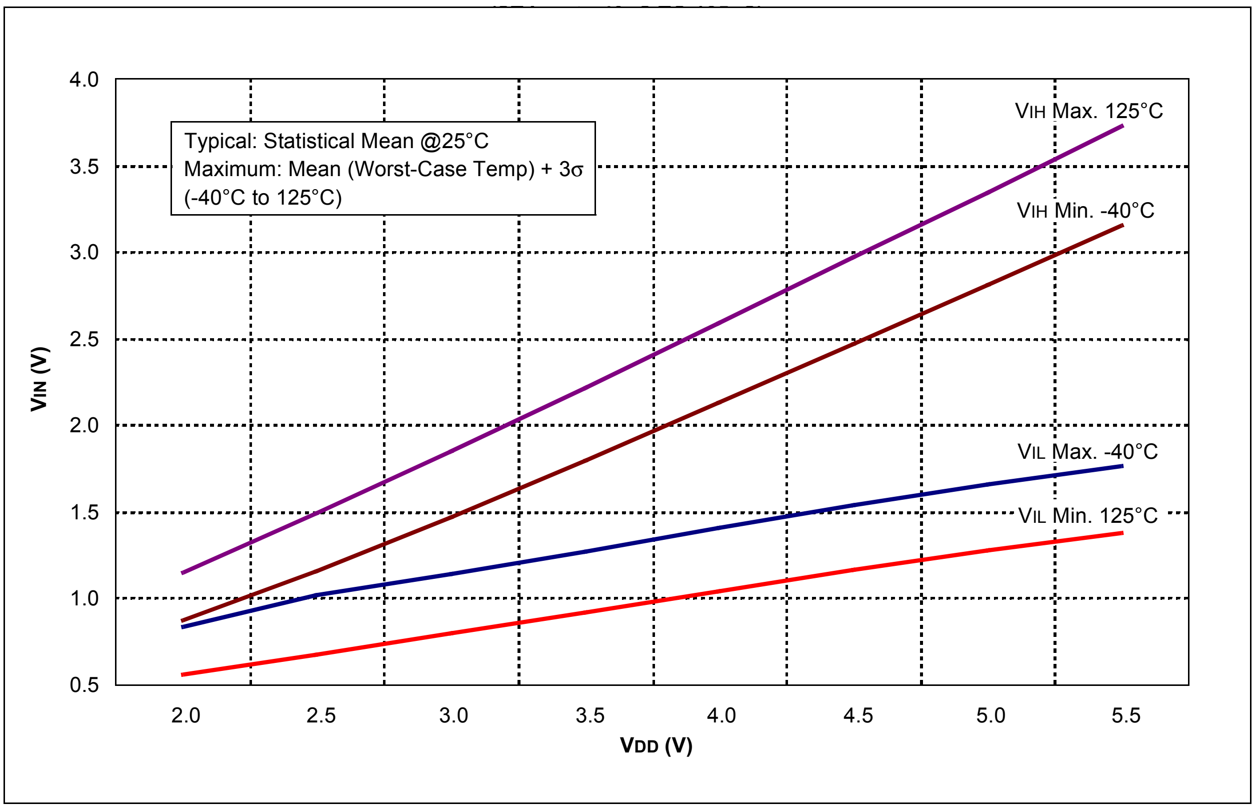
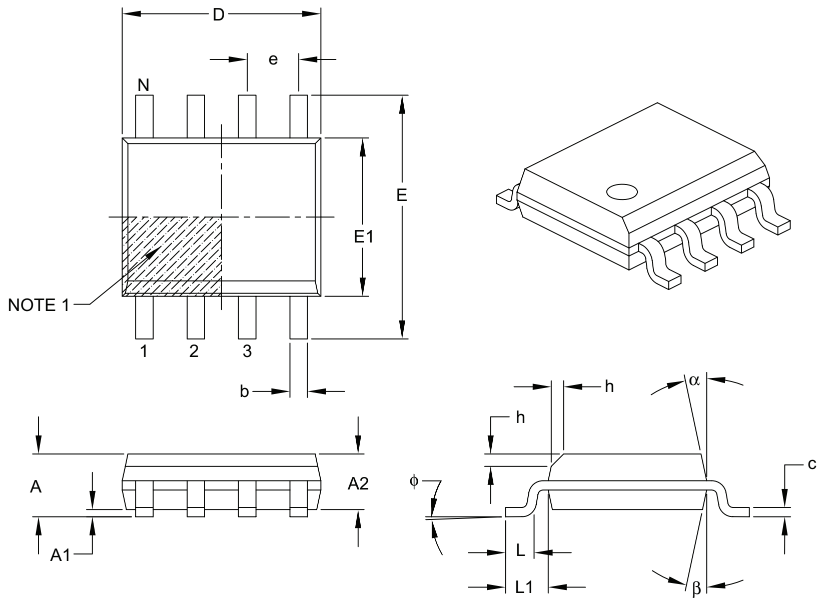


FIGURE 14-13: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD



8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



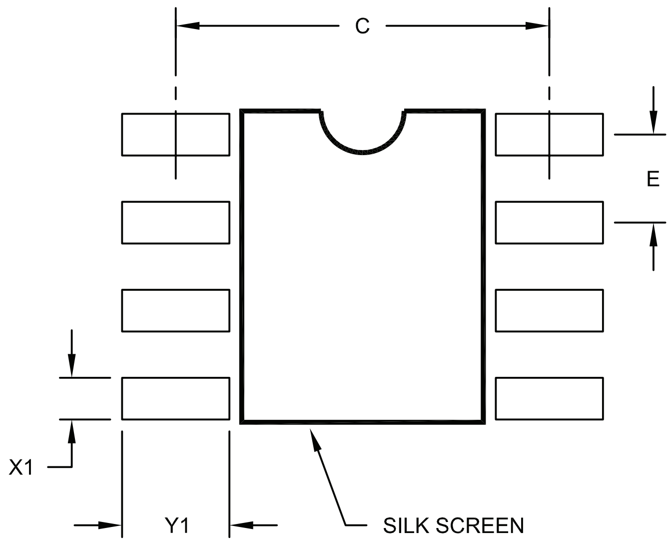
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A