



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	67 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f506t-i-st



PIC12F510/16F506

8/14-Pin, 8-Bit Flash Microcontroller

Devices Included In This Data Sheet:

- PIC16F506
- PIC12F510

High-Performance RISC CPU:

- Only 33 Single-Word Instructions to Learn
- All Single-Cycle Instructions except for Program Branches, which are Two-Cycle
- 12-Bit Wide Instructions
- Two-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- 8-Bit Wide Data Path
- 10 Special Function Hardware Registers (PIC12F510)
- 13 Special Function Hardware Registers (PIC16F506)
- Operating Speed:
 - DC – 8 MHz Crystal Oscillator (PIC12F510)
 - DC – 500 ns instruction cycle (PIC12F510)
 - DC – 20 MHz Crystal Oscillator (PIC16F506)
 - DC – 200 ns instruction cycle (PIC16F506)

Special Microcontroller Features:

- 4 or 8 MHz Selectable Precision Internal Oscillator:
 - Factory calibrated to $\pm 1\%$
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debugging (ICD) Support
- Power-on Reset (POR)
- Device Reset Timer (DRT):
 - Short DRT (1.125 ms, typical) for INTOSC, EXTRC and EC
 - DRT (18 ms, typical) for HS, XT and LP
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed $\overline{\text{MCLR}}$ Input Pin
- Selectable Internal Weak Pull-Ups on I/O Pins
- Power-Saving Sleep mode
- Wake-up from Sleep on Pin Change
- Wake-up from Sleep on Comparator Change

- Selectable Oscillator Options:
 - INTOSC: 4/8 MHz precision Internal oscillator
 - EXTRC: External low-cost RC oscillator
 - XT: Standard crystal/resonator
 - LP: Power-saving, low-frequency crystal
 - HS: High-speed crystal/resonator (PIC16F506 only)
 - EC: High-speed external clock input (PIC16F506 only)
- Analog-to-Digital (A/D) Converter:
 - 8-bit resolution
 - 4-input channels (1 channel is dedicated to conversion of the internal 0.6V absolute voltage reference)
- High Current Sink/Source for Direct LED Drive
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

Low-Power Features/CMOS Technology:

- Operating Current:
 - < 175 μA @ 2V, 4 MHz, typical
- Standby Current:
 - 100 nA @ 2V, typical
- Low-Power, High-Speed Flash Technology:
 - 100,000 cycle Flash endurance
 - > 40-year retention
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
- Wide Temperature Range:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +125°C

Peripheral Features (PIC12F510):

- 6 I/O Pins:
 - 5 I/O pins with individual direction control
 - 1 input only pin
- 1 Analog Comparator with Absolute Reference

Peripheral Features (PIC16F506):

- 12 I/O Pins:
 - 11 I/O pins with individual direction control
 - 1 input only pin
- 2 Analog Comparators with Absolute Reference and Programmable Reference

PIC12F510/16F506

NOTES:

PIC12F510/16F506

NOTES:

PIC12F510/16F506

REGISTER 4-4: OPTION_REG: OPTION REGISTER (PIC16F506)

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
<u>RBWU</u>	<u>RBPU</u>	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **RBWU**: Enable Wake-up On Pin Change bit (RB0, RB1, RB3, RB4)

1 = Disabled

0 = Enabled

bit 6 **RBPU**: Enable Weak Pull-Ups bit (RB0, RB1, RB3, RB4)

1 = Disabled

0 = Enabled

bit 5 **T0CS**: Timer0 Clock Source Select bit

1 = Transition on T0CKI pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: Timer0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin

0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit

1 = Prescaler assigned to the WDT

0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>**: Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

5.0 I/O PORT

As with any other register, the I/O register(s) can be written and read under program control. However, read instructions (e.g., `MOVF PORTB, W`) always read the I/O pins independent of the pin's Input/Output modes. On Reset, all I/O ports are defined as input (inputs are at high-impedance) since the I/O control registers are all set.

Note: On the PIC12F510, I/O PORTB is referenced as GPIO. On the PIC16F506, I/O PORTB is referenced as PORTB.

5.1 PORTB/GPIO

PORTB/GPIO is an 8-bit I/O register. Only the low-order 6 bits are used (RB/GP<5:0>). Bits 7 and 6 are unimplemented and read as '0's. Please note that RB3/GP3 is an input only pin. The Configuration Word can set several I/O's to alternate functions. When acting as alternate functions, the pins will read as '0' during a port read. Pins RB0/GP0, RB1/GP1, RB3/GP3 and RB4 (PIC16F506 only) can be configured with weak pull-up and also for wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If RB3/GP3/MCLR is configured as MCLR, weak pull-up is always on and wake-up on change for this pin is not enabled.

5.2 PORTC (PIC16F506 Only)

PORTC is an 8-bit I/O register. Only the low-order 6 bits are used (RC<5:0>). Bits 7 and 6 are unimplemented and read as '0's.

5.3 TRIS Registers

The Output Driver Control register is loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a High-Impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exception is RB3/GP3, which are input only, and the T0CKI pin, which may be controlled by the OPTION register. See Register 4-3.

Note: A read of the port reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high but the external system is holding it low, a read of the port will indicate that the pin is low.

Note: The TRIS registers are write-only and are set (output drivers disabled) upon Reset.

5.4 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All port pins, except RB3/GP3 which is input only, may be used for both input and output operations. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except RB3/GP3) can be programmed individually as input or output.

FIGURE 5-1: PIC12F510/16F506 EQUIVALENT CIRCUIT FOR PIN DRIVE⁽²⁾

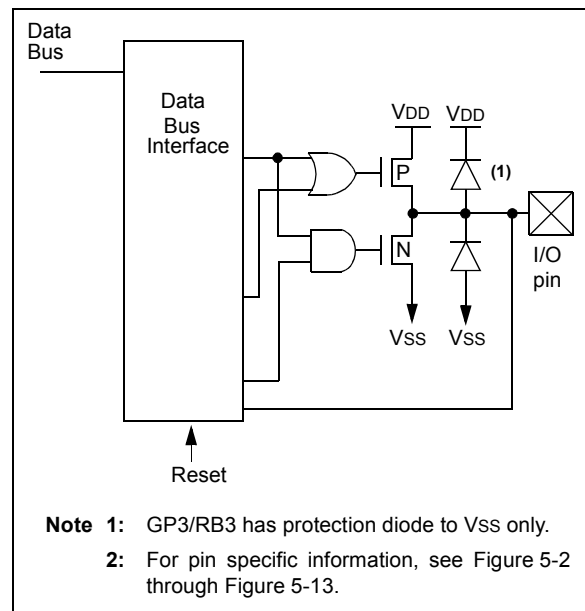


FIGURE 5-4: BLOCK DIAGRAM OF GP2

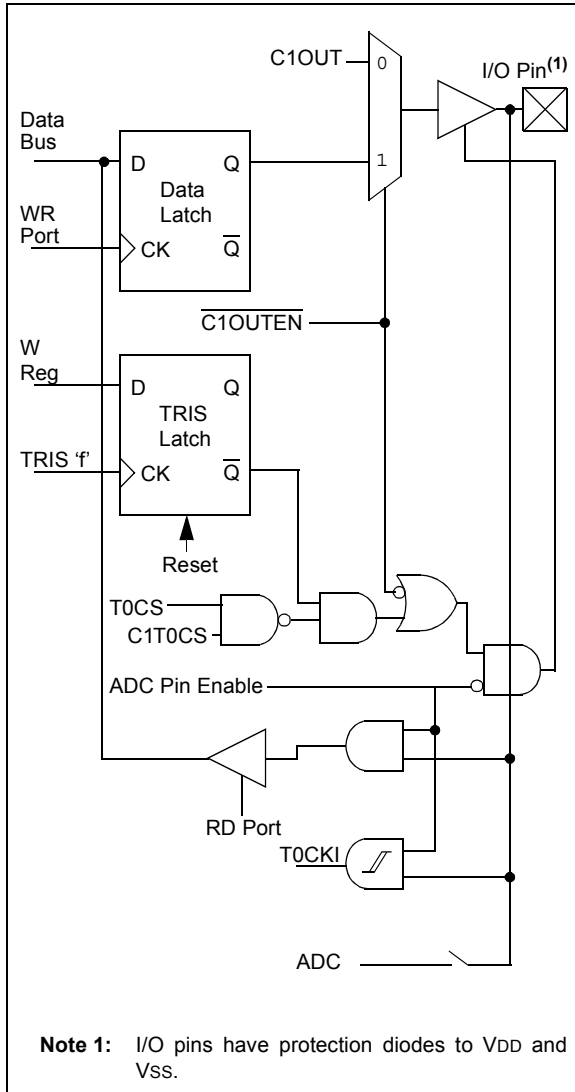


FIGURE 5-5: BLOCK DIAGRAM OF RB2

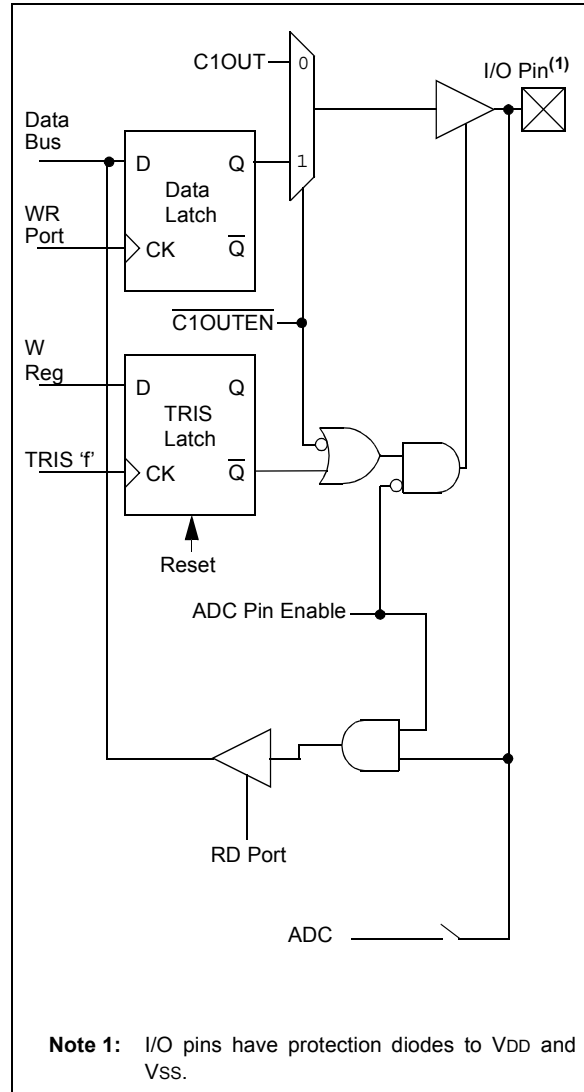
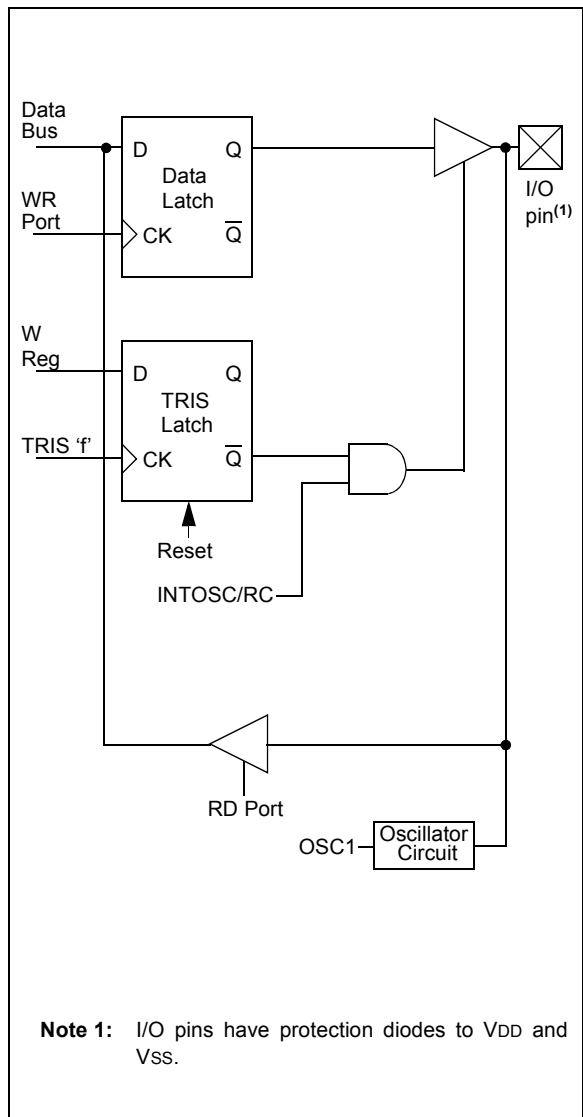


FIGURE 5-7: BLOCK DIAGRAM OF GP4



7.0 COMPARATOR(S)

The PIC12F510 contains one analog comparator module. The PIC16F506 contains two comparators and a comparator voltage reference.

REGISTER 7-1: CM1CON0: COMPARATOR C1 CONTROL REGISTER (PIC12F510)

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **C1OUT:** Comparator Output bit
 1 = $V_{IN+} > V_{IN-}$
 0 = $V_{IN+} < V_{IN-}$
- bit 6 **C1OUTEN:** Comparator Output Enable bit^{(1), (2)}
 1 = Output of comparator is NOT placed on the C1OUT pin
 0 = Output of comparator is placed in the C1OUT pin
- bit 5 **C1POL:** Comparator Output Polarity bit⁽²⁾
 1 = Output of comparator is not inverted
 0 = Output of comparator is inverted
- bit 4 **C1T0CS:** Comparator TMR0 Clock Source bit⁽²⁾
 1 = TMR0 clock source selected by T0CS control bit
 0 = Comparator output used as TMR0 clock source
- bit 3 **C1ON:** Comparator Enable bit
 1 = Comparator is on
 0 = Comparator is off
- bit 2 **C1NREF:** Comparator Negative Reference Select bit⁽²⁾
 1 = C1IN- pin
 0 = 0.6V internal reference
- bit 1 **C1PREF:** Comparator Positive Reference Select bit⁽²⁾
 1 = C1IN+ pin
 0 = C1IN- pin
- bit 0 **C1WU:** Comparator Wake-up On Change Enable bit⁽²⁾
 1 = Wake-up On Comparator Change is disabled
 0 = Wake-up On Comparator Change is enabled

Note 1: Overrides T0CS bit for TRIS control of RB2.

2: When comparator is turned on, these control bits assert themselves.

REGISTER 7-3: CM2CON0: COMPARATOR C2 CONTROL REGISTER (PIC16F506)

R-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
C2OUT	$\overline{\text{C2OUTEN}}$	C2POL	C2PREF2	C2ON	C2NREF	C2PREF1	$\overline{\text{C2WU}}$
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **C2OUT:** Comparator Output bit
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
- bit 6 **$\overline{\text{C2OUTEN}}$:** Comparator Output Enable bit^{(1), (2)}
1 = Output of comparator is NOT placed on the C2OUT pin
0 = Output of comparator is placed in the C2OUT pin
- bit 5 **C2POL:** Comparator Output Polarity bit⁽²⁾
1 = Output of comparator not inverted
0 = Output of comparator inverted
- bit 4 **C2PREF2:** Comparator Positive Reference Select bit⁽²⁾
1 = C1IN+ pin
0 = C2IN- pin
- bit 3 **C2ON:** Comparator Enable bit
1 = Comparator is on
0 = Comparator is off
- bit 2 **C2NREF:** Comparator Negative Reference Select bit⁽²⁾
1 = C2IN- pin
0 = V_{REF}
- bit 1 **C2PREF1:** Comparator Positive Reference Select bit⁽²⁾
1 = C2IN+ pin
0 = C2PREF2 controls analog input selection
- bit 0 **$\overline{\text{C2WU}}$:** Comparator Wake-up on Change Enable bit⁽²⁾
1 = Wake-up on Comparator change is disabled
0 = Wake-up on Comparator change is enabled.

Note 1: Overrides TOCS bit for TRIS control of RC4.

2: When comparator is turned on, these control bits assert themselves. Otherwise, the other registers have precedence.

PIC12F510/16F506

FIGURE 7-1: COMPARATOR 1 BLOCK DIAGRAM FOR PIC12F510/16F506

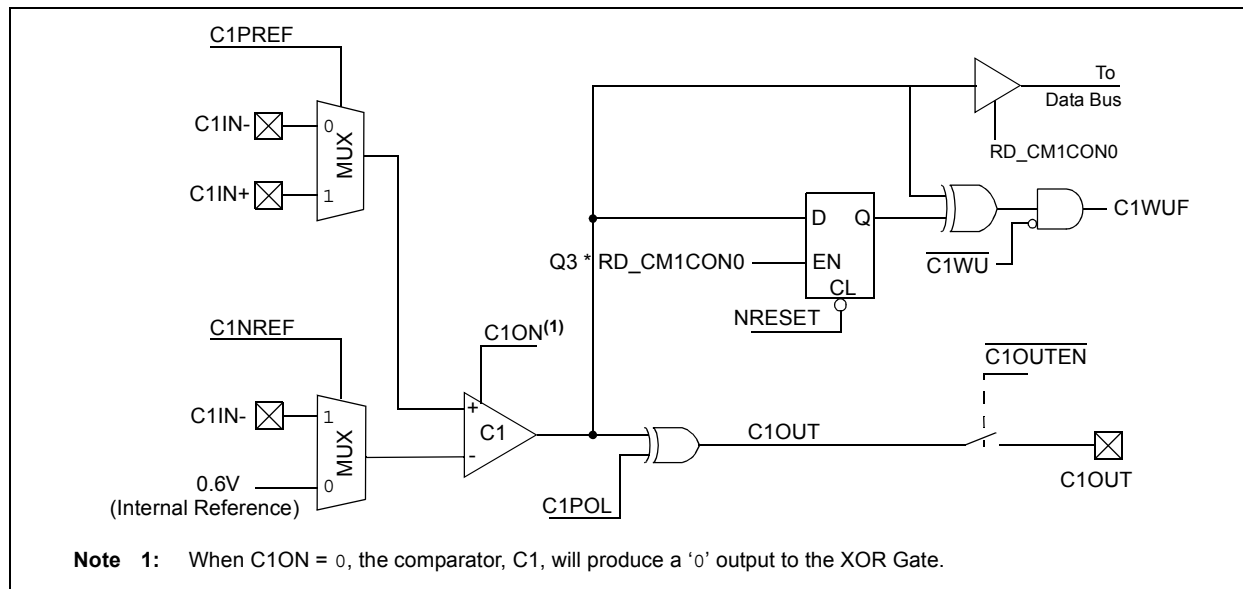
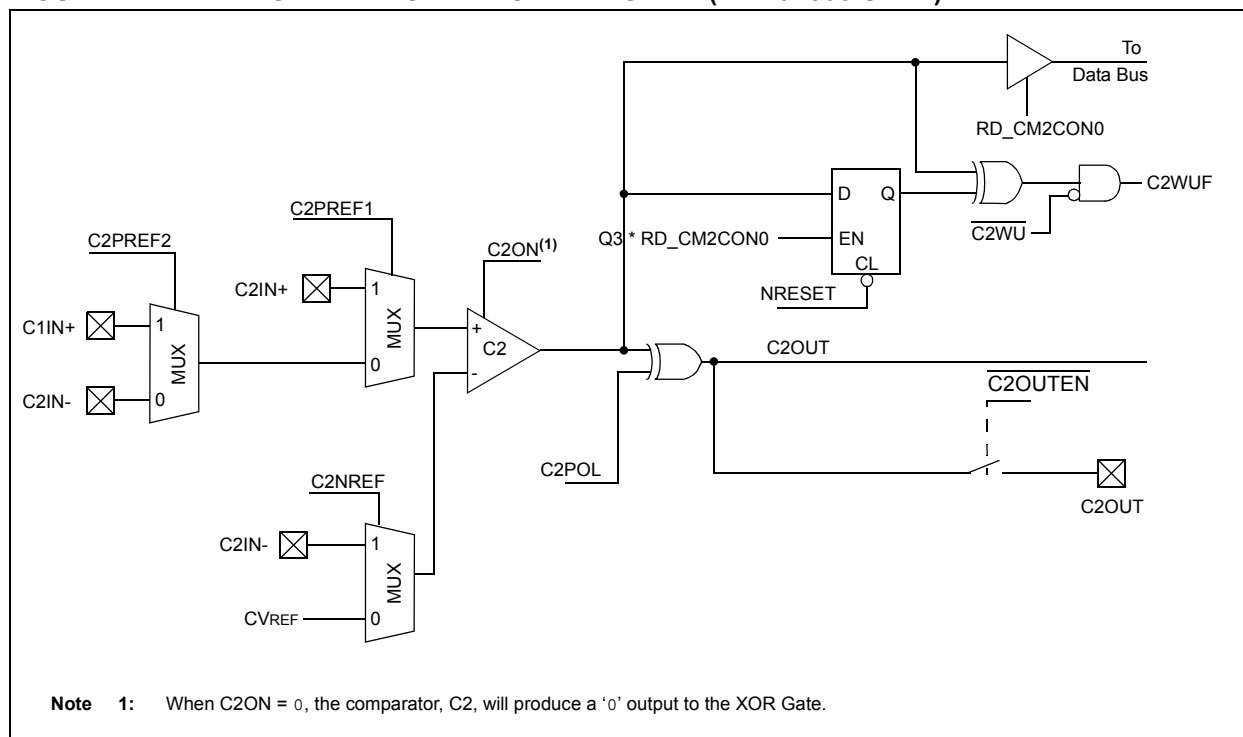


FIGURE 7-2: COMPARATOR 2 BLOCK DIAGRAM (PIC16F506 ONLY)



8.0 COMPARATOR VOLTAGE REFERENCE MODULE (PIC16F506 ONLY)

The comparator voltage reference module also allows the selection of an internally generated voltage reference for one of the C2 comparator inputs. The VRCON register (Register 8-1) controls the voltage reference module shown in Figure 8-1.

8.1 Configuring The Voltage Reference

The voltage reference can output 32 voltage levels; 16 in a high range and 16 in a low range.

Equation 8-1 determines the output voltages:

EQUATION 8-1:

$$\begin{aligned} VRR = 1 \text{ (low range): } CVREF &= (VR<3:0>/24) \times VDD \\ VRR = 0 \text{ (high range): } \\ CVREF &= (VDD/4) + (VR<3:0> \times VDD/32) \end{aligned}$$

8.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 8-1) keep CVREF from approaching VSS or VDD. The exception is when the module is disabled by clearing the VREN bit (VRCON<7>). When disabled, the reference voltage is VSS when VR<3:0> is '0000' and the VRR (VRCON<5>) bit is set. This allows the comparator to detect a zero-crossing and not consume the CVREF module current.

The voltage reference is VDD derived and, therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the comparator voltage reference can be found in **Section 13.2 "DC Characteristics: PIC12F510/16F506 (Extended)"**.

REGISTER 8-1: VRCON: VOLTAGE REFERENCE CONTROL REGISTER (PIC16F506 ONLY)

R/W-0	R/W-0	R/W-1	U-1	R/W-1	R/W-1	R/W-1	R/W-1
VREN	VROE	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0', except if denoted otherwise
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7	VREN: CVREF Enable bit 1 = CVREF is powered on 0 = CVREF is powered down, no current is drawn
bit 6	VROE: CVREF Output Enable bit ⁽¹⁾ 1 = CVREF output is enabled 0 = CVREF output is disabled
bit 5	VRR: CVREF Range Selection bit 1 = Low range 0 = High range
bit 4	Unimplemented: Read as '1'
bit 3-0	VR<3:0> CVREF Value Selection bit When VRR = 1: CVREF = (VR<3:0>/24)*VDD When VRR = 0: CVREF = VDD/4 + (VR<3:0>/32)*VDD

Note 1: When this bit is set, the TRIS for the CVREF pin is overridden and the analog voltage is placed on the CVREF pin.

2: CVREF controls for ratio metric reference applies to Comparator 2 on the PIC16F506 only.

10.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC12F510/16F506 microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These features are:

- Oscillator Selection
- Reset:
 - Power-on Reset (POR)
 - Device Reset Timer (DRT)
 - Wake-up from Sleep on Pin Change
- Watchdog Timer (WDT)
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™ (ICSP™)
- Clock Out

The PIC12F510/16F506 devices have a Watchdog Timer, which can be shut off only through Configuration bit WDTE. It runs off of its own RC oscillator for added reliability. If using HS (PIC16F506), XT or LP selectable oscillator options, there is always a delay, provided by the Device Reset Timer (DRT), intended to keep the chip in Reset until the crystal oscillator is stable. If using INTOSC, EXTRC or EC there is an 1.125 ms (nominal) delay only on VDD power-up. With this timer on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through a change-on-input pin or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application, including an internal 4/8 MHz oscillator. The EXTRC oscillator option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options.

10.1 Configuration Bits

The PIC12F510/16F506 Configuration Words consist of 12 bits. Configuration bits can be programmed to select various device configurations. Three bits are for the selection of the oscillator type; (two bits on the PIC12F510), one bit is the Watchdog Timer enable bit, one bit is the MCLR enable bit and one bit is for code protection (Register 10-1, Register 10-2).

10.3 Reset

The device differentiates between various kinds of Reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Time-out Reset during normal operation
- WDT Time-out Reset during Sleep
- Wake-up from Sleep Reset on pin change
- Wake-up from Sleep Reset on comparator change

Some registers are not reset in any way, they are unknown on POR and unchanged in any other Reset. Most other registers are reset to “Reset state” on Power-on Reset (POR), $\overline{\text{MCLR}}$, WDT or Wake-up from Sleep Reset on pin change or wake-up from Sleep Reset on comparator change. The exceptions are TO , PD , CWUF and RBWUF/GPWUF bits. They are set or cleared differently in different Reset situations. These bits are used in software to determine the nature of Reset. See Table 10-4 for a full description of Reset states of all registers.

TABLE 10-3: RESET CONDITIONS FOR REGISTERS – PIC12F510

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up On Pin Change, Wake-up on Comparator Change
W	—	q q q q q q q u ⁽¹⁾	q q q q q q q u ⁽¹⁾
INDF	00h	x x x x x x x x	u u u u u u u u
TMR0	01h	x x x x x x x x	u u u u u u u u
PCL	02h	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
STATUS	03h	0 0 0 1 1 x x x	q q 0 q q u u u ⁽²⁾
FSR	04h	1 1 0 x x x x x	1 1 u u u u u u
OSCCAL	05h	1 1 1 1 1 1 1 -	u u u u u u u -
GPIO	06h	- - x x x x x x	- - u u u u u u
CM1CON0	07h	1 1 1 1 1 1 1 1	u u u u u u u u
ADCON0	08h	1 1 1 1 1 1 0 0	u u 1 1 1 1 0 0
ADRES	09h	x x x x x x x x	u u u u u u u u
OPTION	—	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
TRISIO	—	- - 1 1 1 1 1 1	- - 1 1 1 1 1 1

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as ‘0’, q = value depends on condition.

Note 1: Bits <7:2> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.

2: See Table 10-5 for Reset value for specific conditions.

PIC12F510/16F506

10.5 Device Reset Timer (DRT)

On the PIC12F510/16F506 devices, the DRT runs any time the device is powered up. DRT runs from Reset and varies based on oscillator selection and Reset type (see Table 10-6).

The DRT operates from a free running on-chip oscillator that is separate from INTOSC. The processor is kept in Reset as long as the DRT is active. The DRT delay allows VDD to rise above VDD minimum and for the oscillator to stabilize.

Oscillator circuits, based on crystals or ceramic resonators, require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the devices in a Reset for a set period, as stated in Table 10-6, after MCLR has reached a logic high (V_{IH} MCLR) level. Programming (GP3/RB3)/MCLR/VPP as MCLR and using an external RC network connected to the MCLR input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the (GP3/RB3)/MCLR/VPP pin as a general purpose input.

The DRT delays will vary from chip-to-chip due to VDD, temperature and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out from Sleep. This is particularly important for applications using the WDT to wake from Sleep mode automatically.

Reset sources are POR, MCLR, WDT time-out, Wake-up on Pin Change and Wake-up on Comparator Change. See **Section 10.9.2 “Wake-up from Sleep Reset”**, **Notes 1, 2 and 3**.

10.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator that does not require any external components. This RC oscillator is separate from the external RC oscillator of the (GP5/RB5)/OSC1/CLKIN pin and the internal 4/8 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset generates a device Reset.

The \overline{TO} bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see **Section 10.1 “Configuration Bits”**). Refer to the PIC12F510/16F506 Programming Specifications to determine how to access the Configuration Word.

TABLE 10-6: TYPICAL DRT PERIODS

Oscillator Configuration	POR Reset	Subsequent Resets
LP	18 ms	18 ms
XT	18 ms	18 ms
HS ⁽¹⁾	18 ms	18 ms
EC ⁽¹⁾	1.125 ms	10 μ s
INTOSC	1.125 ms	10 μ s
EXTRC	1.125 ms	10 μ s

Note 1: PIC16F506 only

Note: It is the responsibility of the application designer to ensure the use of the 1.125 ms nominal DRT will result in acceptable operation. Refer to Electrical Specifications for VDD rise time and stability requirements for this mode of operation.

10.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a divisor ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst-case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

10.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

PIC12F510/16F506

FIGURE 14-2: TYPICAL I_{PD} vs. V_{DD} (SLEEP MODE, ALL PERIPHERALS DISABLED)

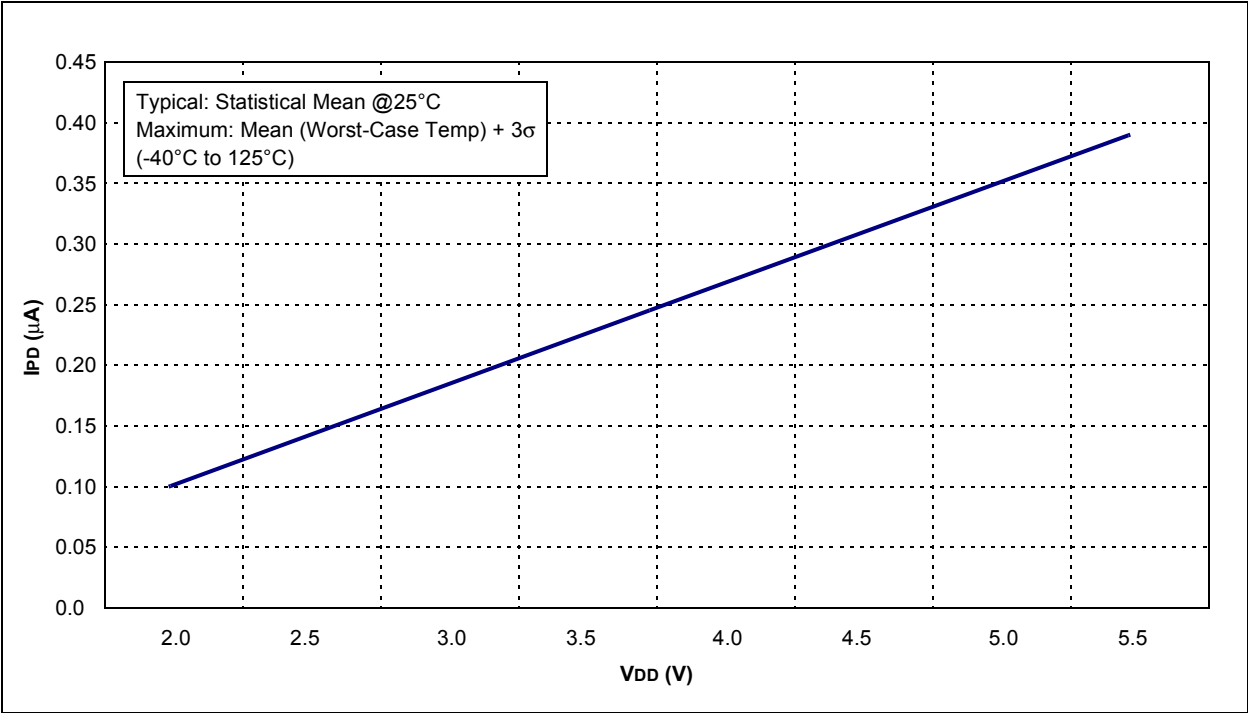
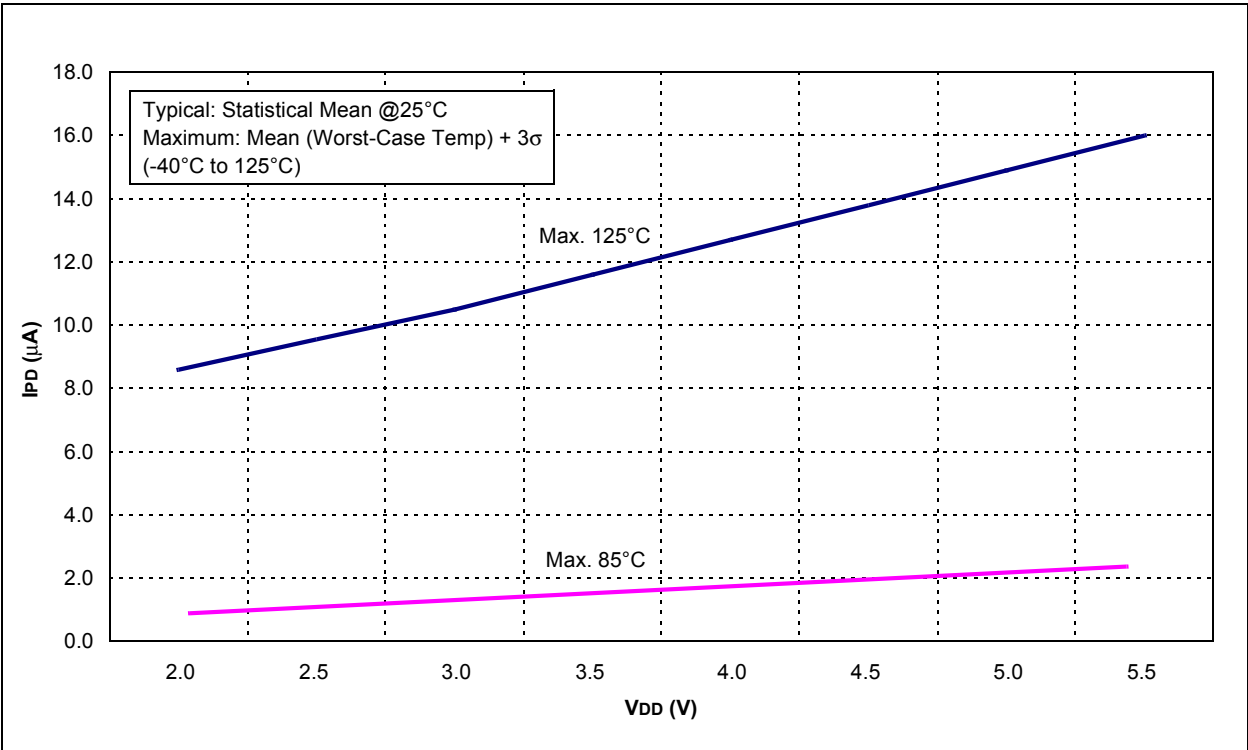


FIGURE 14-3: MAXIMUM I_{PD} vs. V_{DD} (SLEEP MODE, ALL PERIPHERALS DISABLED)



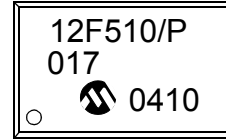
15.0 PACKAGING

15.1 Package Marking Information

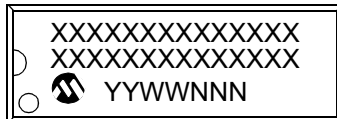
8-Lead PDIP



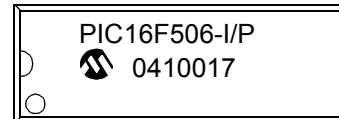
Example



14-Lead PDIP



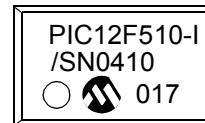
Example



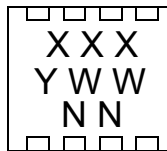
8-Lead SOIC (3.90 mm)



Example



8-Lead 2x3 DFN*



Example

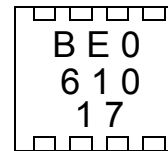


TABLE 15-1: 8-LEAD 2X3 DFN (MC) TOP MARKING

Part Number	Marking
PIC12F510(T)-I/MC	BS0
PIC12F510-E/MC	BT0

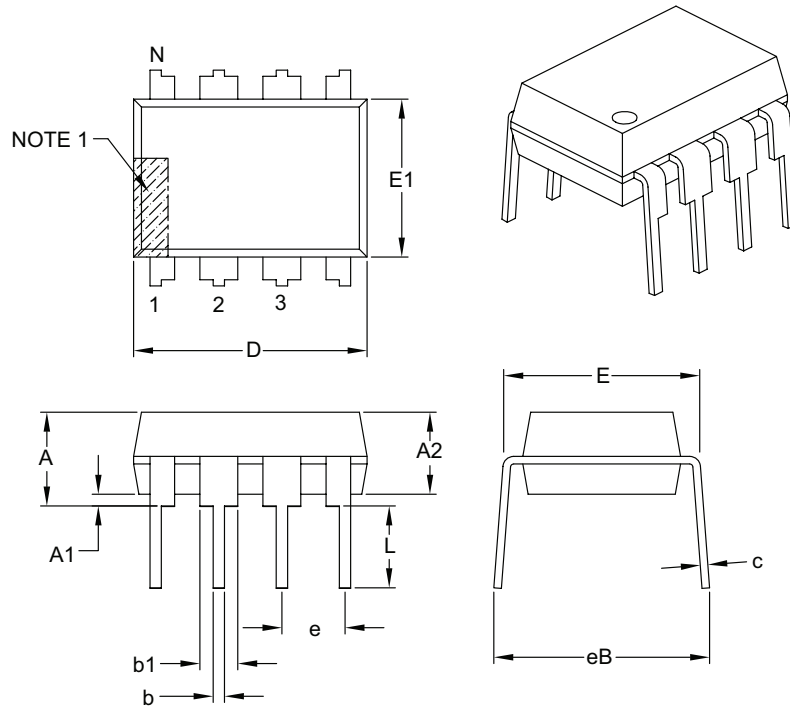
Legend:	XX...X Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard PIC® device marking consists of Microchip part number, year code, week code and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

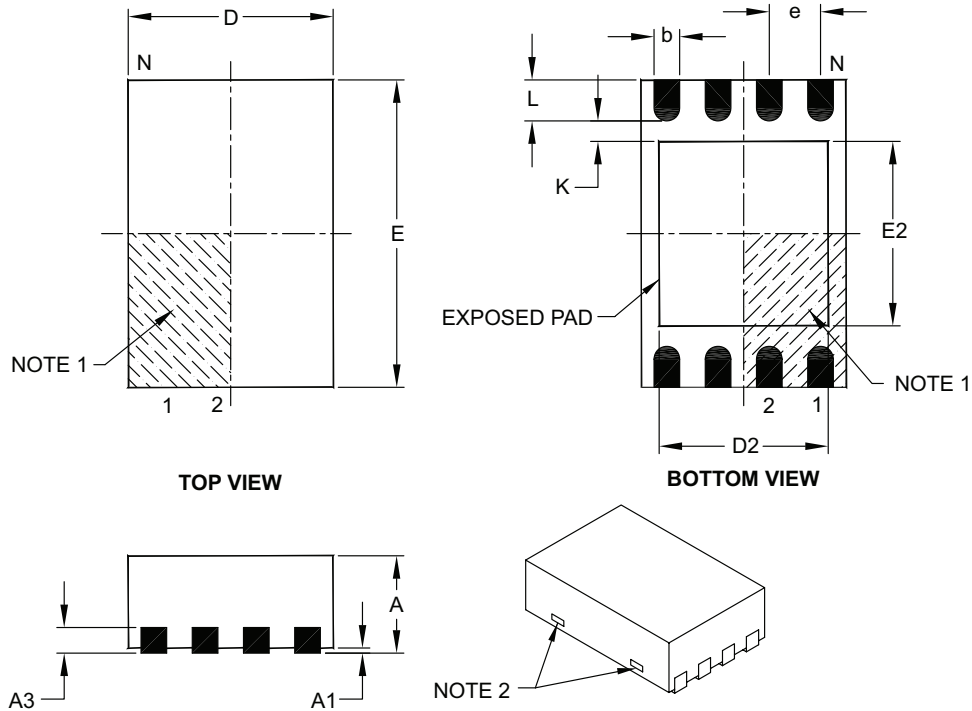
- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.30	–	1.75
Exposed Pad Width	E2	1.50	–	1.90
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

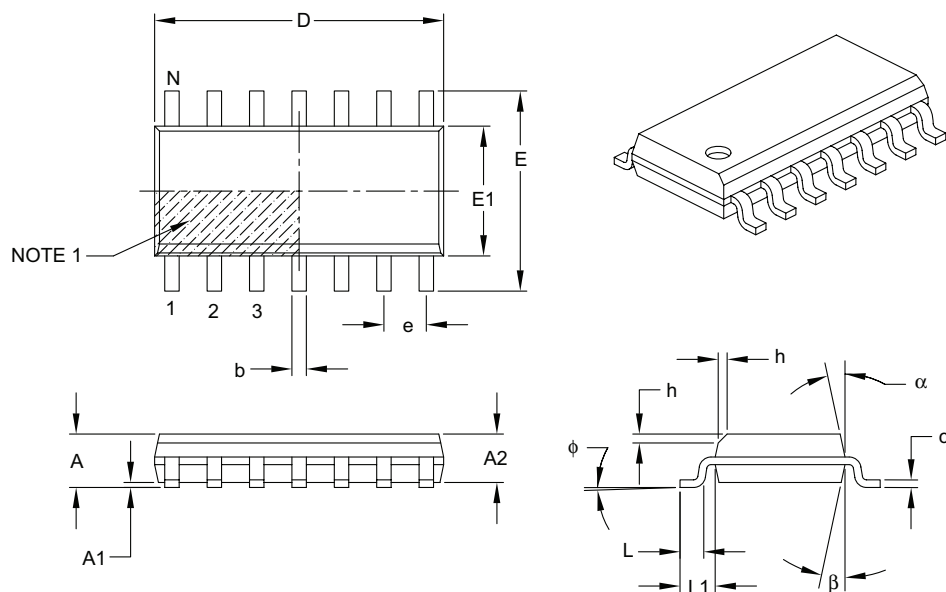
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123B

PIC12F510/16F506

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

PIC12F510/16F506

NOTES: