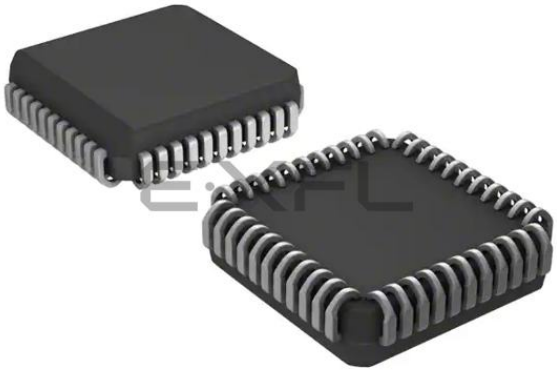

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| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8051 |
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| Peripherals | POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/p89cv51rb2fa-512 |

**Table 3. P89CV51RB2/RC2/RD2 Pin description** *...continued*

| Symbol | Pin | | Type | Description |
|---|---|---|---|---|
| | PLCC44 | TQFP44 | | |
| P0[6]/AD6 | 37 | 31 | I/O | **P0[6] —** Port 0 bit 6. |
| | | | I/O | **AD6 —** Address/data bit 6. |
| P0[7]/AD7 | 36 | 30 | I/O | **P0[7] —** Port 0 bit 7. |
| | | | I/O | **AD7 —** Address/data bit 7. |
| P1[0] to P1[7] | | | I/O with internal pull-up | **Port 1**: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 pins are pulled HIGH by the internal pull-ups when 1s are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled LOW will source current ($I_{IL}$) because of the internal pull-ups. P1[5], P1[6], P1[7] have high current drive of 16 mA. |
| P1[0]/T2 | 2 | 40 | I/O | **P1[0] —** Port 1 bit 0. |
| | | | I/O | **T2 —** External count input to timer/counter 2 or clock-out from timer/counter 2. |
| P1[1]/T2EX | 3 | 41 | I/O | **P1[1] —** Port 1 bit 1. |
| | | | I | **T2EX**: Timer/counter 2 capture/reload trigger and direction control. |
| P1[2]/ECI | 4 | 42 | I/O | **P1[2] —** Port 1 bit 2. |
| | | | I | **ECI —** External clock input. This signal is the external clock input for the PCA. |
| P1[3]/CEX0 | 5 | 43 | I/O | **P1[3] —** Port 1 bit 3. |
| | | | I/O | **CEX0 —** Capture/compare external I/O for PCA Module 0. Each capture/compare module connects to a Port 1 pin for external I/O. When not used by the PCA, this pin can handle standard I/O. |
| P1[4]/CEX1/ $\overline{SS}$ | 6 | 44 | I/O | **P1[4] —** Port 1 bit 4. |
| | | | I/O | **CEX1 —** Capture/compare external I/O for PCA Module 1. |
| | | | I | **$\overline{SS}$ —** Slave Select input for SPI. |
| P1[5]/CEX2/ MOSI | 7 | 1 | I/O | **P1[5] —** Port 1 bit 5. |
| | | | I/O | **CEX2 —** Capture/compare external I/O for PCA Module 2. |
| | | | I/O | **MOSI —** Master output/slave input for SPI. |
| P1[6]/CEX3/ MISO | 8 | 2 | I/O | **P1[6] —** Port 1 bit 6. |
| | | | I/O | **CEX3 —** Capture/compare external I/O for PCA Module 3. |
| | | | I/O | **MISO —** Master input/slave output for SPI. |
| P1[7]/CEX4/ SPICLK | 9 | 3 | I/O | **P1[7] —** Port 1 bit 7. |
| | | | I/O | **CEX4 —** Capture/compare external I/O for PCA Module 4. |
| | | | I/O | **SPICLK —** Serial clock input/output for SPI. |
| P2[0] to P2[7] | | | I/O with internal pull-up | **Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins are pulled HIGH by the internal pull-ups when 1s are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled LOW will source current ($I_{IL}$) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit address (MOVX @DPTR). In this application, it uses strong internal pull-ups when transitioning to 1s. |
| P2[0]/A8 | 24 | 18 | I/O | **P2[0] —** Port 2 bit 0. |
| | | | O | **A8 —** Address bit 8. |

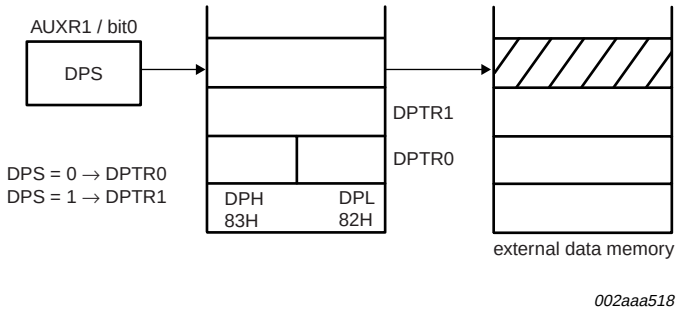



**Fig 5. Dual data pointer organization**

**Table 8. AUXR1 - Auxiliary function register 1 (address A2H) bit allocation**

*Not bit addressable; reset value 00H.*

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | - | ENBOOT | - | GF2 | 0 | - | DPS |

**Table 9. AUXR1 - Auxiliary function register 1 (address A2H) bit description**

| Bit | Symbol | Description |
|---|---|---|
| 7, 6, 4 | - | Reserved for future use. Should be set to 0 by user programs. |
| 5 | ENBOOT | Enable BOOTROM |
| 3 | GF2 | General purpose user-defined Flag. |
| 2 | 0 | This bit contains a hard-wired 0. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register. |
| 1 | - | Reserved for future use. Should be set to 0 by user programs. |
| 0 | DPS | Data Pointer Select. Chooses one of two data pointers for use by the program. See text for details. |

### 6.2.3 Reset

At initial power-up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins HIGH. Powering up the device without a valid reset could cause the MCU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash. A system reset will not affect the on-chip RAM while the device is running, however, the contents of the on-chip RAM during power-up are indeterminate.

When power is applied to the device, the RST pin must be held HIGH long enough for the oscillator to start-up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement an RC circuit by connecting the RST pin to $V_{DD}$ through a 10 µF capacitor and to $V_{SS}$ through an 8.2 kΩ resistor as shown in Figure 6.

During initial power-up the POF flag in the PCON register is set to indicate an initial power-up condition. The POF flag will remain active until cleared by software.

**Table 11. ISP Hex record formats** *…continued*

| Record type | Command/data function |
|---|---|
| 03 | Miscellaneous write functions<br>:nnxxxx03ffssddcc<br>Where:<br>nn = number of bytes in the record<br>xxxx = required field but value is a don't care<br>ff = subfunction code<br>ss = selection code<br>dd = data (if needed)<br>cc = checksum<br>Subfunction code = 0C (erase 4 kB blocks)<br>ff = 0C<br>ss = block code, as shown below:<br>block 0, 0 kB to 4 kB, 00H<br>block 1, 4 kB to 8 kB, 10H<br>block 2, 8 kB to 12 kB, 20H<br>block 3, 12 kB to 16 kB, 30H<br>block 4, 16 kB to 20 kB, 40H (only available on P89CV51RC2/RD2)<br>block 5, 20 kB to 24 kB, 50H (only available on P89CV51RC2/RD2)<br>block 6, 24 kB to 28 kB, 60H (only available on P89CV51RC2/RD2)<br>block 7, 28 kB to 32 kB, 70H (only available on P89CV51RC2/RD2)<br>block 8, 32 kB to 36 kB, 80H (only available on P89CV51RD2)<br>block 9, 36 kB to 40 kB, 90H (only available on P89CV51RD2)<br>block 10, 40 kB to 44 kB, A0H (only available on P89CV51RD2)<br>block 11, 44 kB to 48 kB, B0H (only available on P89CV51RD2)<br>block 12, 48 kB to 52 kB, C0H (only available on P89CV51RD2)<br>block 13, 52 kB to 56 kB, D0H (only available on P89CV51RD2)<br>block 14, 56 kB to 60 kB, E0H (only available on P89CV51RD2)<br>block 15, 60 kB to 64 kB, F0H (only available on P89CV51RD2)<br>Example:<br>:020000030C20CF (erase 4 kB block #2) |

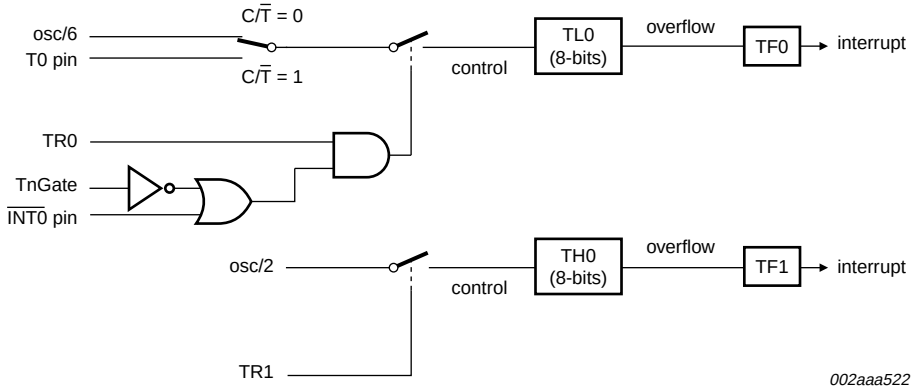



**Fig 10. Timer/counter 0 Mode 3 (two 8-bit counters)**

## 6.5 Timer 2

Timer 2 is a 16-bit timer/counter which can operate as either an event timer or an event counter, as selected by C/$\overline{T}$2 in the special function register T2CON. Timer 2 has four operating modes: Capture, Auto-reload (up or down counting), Clock-out, and Baud rate generator which are selected according to Table 18 using T2CON (Table 19 and Table 20) and T2MOD (Table 21 and Table 22).

**Table 18. Timer 2 operating mode**

| RCLK + TCLK | CP/$\overline{RL}$2 | TR2 | T2OE | Mode |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 16-bit auto reload |
| 0 | 1 | 1 | 0 | 16-bit capture |
| 0 | 0 | 1 | 1 | Programmable clock-out |
| 1 | X | 1 | 0 | Baud rate generator |
| X | X | 0 | X | off |

**Table 19. T2CON - Timer/Counter 2 control register (address C8H) bit allocation**

*Bit addressable; reset value: 00H.*

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/$\overline{T}$2 | CP/$\overline{RL}$2 |

**Table 20. T2CON - Timer/Counter 2 control register (address C8H) bit description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | TF2 | Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1 or when Timer 2 is in Clock-out mode. |
| 6 | EXF2 | Timer 2 external flag is set when Timer 2 is in capture, reload or baud rate mode, EXEN2 = 1 and a negative transition on T2EX occurs. If Timer 2 interrupt is enabled EXF2 = 1 causes the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. |
| 5 | RCLK | Receive clock flag. When set, causes the UART to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock. |

**Table 20. T2CON - Timer/Counter 2 control register (address C8H) bit description** *...continued*

| Bit | Symbol | Description |
|---|---|---|
| 4 | TCLK | Transmit clock flag. When set, causes the UART to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock. |
| 3 | EXEN2 | Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX. |
| 2 | TR2 | Start/stop control for Timer 2. A logic 1 enables the timer to run. |
| 1 | C/$\overline{T}$2 | Timer or counter select. (Timer 2)<br>0 = internal timer ($f_{osc}$ / 6)<br>1 = external event counter (falling edge triggered; external clock's maximum rate = $f_{osc}$ / 12) |
| 0 | CP/$\overline{RL}$2 | Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow. |

**Table 21. T2MOD - Timer 2 mode control register (address C9H) bit allocation**

*Not bit addressable; reset value: XX00 0000B.*

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | - | - | - | - | - | T2OE | DCEN |

**Table 22. T2MOD - Timer 2 mode control register (address C9H) bit description**

| Bit | Symbol | Description |
|---|---|---|
| 7 to 2 | - | Reserved for future use. Should be set to 0 by user programs. |
| 1 | T2OE | Timer 2 Output Enable bit. Used in programmable Clock-out mode only. |
| 0 | DCEN | Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter. |

### 6.5.1 Capture mode

In the Capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0 Timer 2 is a 16-bit timer or counter (as selected by C/$\overline{T}$2 in T2CON) which upon overflowing sets bit TF2, the Timer 2 overflow bit. The Capture mode is illustrated in Figure 11.

This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit ET2 in the IE register). If EXEN2 = 1, Timer 2 operates as described above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively.

In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt). The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt.

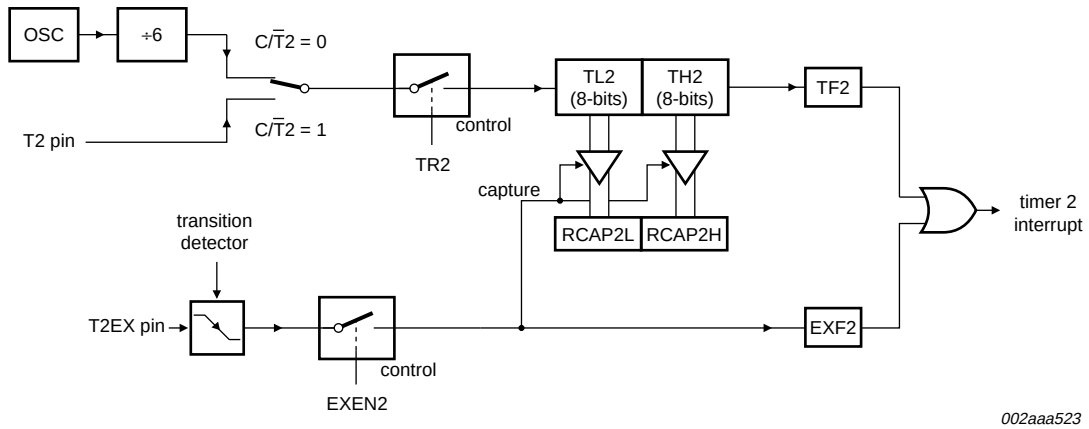



**Fig 11. Timer 2 in Capture mode**

There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2 pin transitions or $f_{osc}$ / 6 pulses. Since once loaded contents of RCAP2L and RCAP2H registers are not protected, once Timer 2 interrupt is signalled it has to be serviced before a new capture event on T2EX pin occurs. Otherwise, the next falling edge on T2EX pin will initiate reload of the current value from TL2 and TH2 to RCAP2L and RCAP2H and consequently corrupt their content related to the previously reported interrupt.

### 6.5.2 Auto-reload mode (up or down counter)

In the 16-bit auto-reload mode, Timer 2 can be configured as either a timer or counter (via C/T2 in T2CON), then programmed to count up or down. The counting direction is determined by bit DCEN (Down Counter Enable) which is located in the T2MOD register (see Table 21 and Table 22). When reset is applied, DCEN = 0 and Timer 2 will default to counting up. If the DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 12 shows Timer 2 counting up automatically (DCEN = 0).

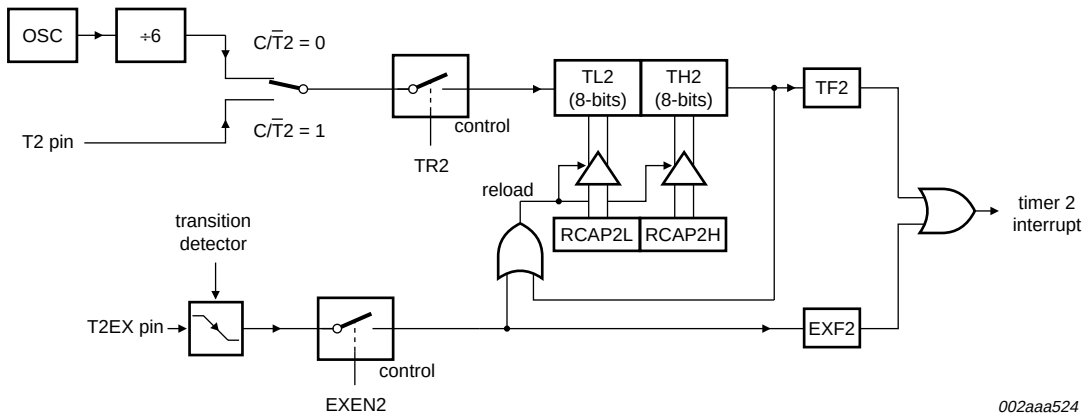



**Fig 12. Timer 2 in Auto-reload mode (DCEN = 0)**

**Table 24. SCON - Serial port control register (address 98H) bit allocation**

*Bit addressable; reset value: 00H.*

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | SM0/FE | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |

**Table 25. SCON - Serial port control register (address 98H) bit description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | SM0/FE | The usage of this bit is determined by SMOD0 in the PCON register. If SMOD0 = 0, this bit is SM0, which with SM1, defines the serial port mode. If SMOD0 = 1, this bit is FE (Framing Error). FE is set by the receiver when an invalid stop bit is detected. Once set, this bit cannot be cleared by valid frames but can only be cleared by software. (Note: It is recommended to set up UART mode bits SM0 and SM1 before setting SMOD0 to 1.) |
| 6 | SM1 | With SM0, defines the serial port mode; see Table 26. |
| 5 | SM2 | Enables the multiprocessor communication feature in modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0. |
| 4 | REN | Enables serial Reception. Set by software to enable reception. Clear by software to disable reception. |
| 3 | TB8 | The 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired. |
| 2 | RB8 | In modes 2 and 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is undefined. |
| 1 | TI | Transmit Interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the stop bit in the other modes, in any serial transmission. Must be cleared by software. |
| 0 | RI | Receive Interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or approximately halfway through the stop bit time in all other modes. (See SM2 for exceptions). Must be cleared by software. |

**Table 26. SCON - Serial port control register (address 98H) SM0/SM1 mode definition**

| SM0, SM1 | UART mode | Baud rate |
|---|---|---|
| 0 0 | 0: shift register | CPU clock / 6 |
| 0 1 | 1: 8-bit UART | variable |
| 1 0 | 2: 9-bit UART | CPU clock / 32 or CPU clock / 16 |
| 1 1 | 3: 9-bit UART | variable |

### 6.6.5 Framing error

Framing Error (FE) is reported in the SCON.7 bit if SMOD0 (PCON.6) = 1. If SMOD0 = 0, SCON.7 is the SM0 bit for the UART, it is recommended that SM0 is set up before SMOD0 is set to 1.

### 6.6.6 More about UART Mode 1

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset to align its roll-overs with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated.

### 6.6.7 More about UART Modes 2 and 3

Reception is performed in the same manner as in Mode 1.

The signal to load special function register SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF.

### 6.6.8 Multiprocessor communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed so that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte: the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte, i.e. the received 9th bit is 0. However, an address byte having the 9th bit set to 1 will interrupt all slaves, so that each slave can examine the received byte to see if it is being addressed or not. The addressed slave will clear its SM2 bit and prepare to receive the data (still 9 bits long) that follow. The slaves that were not addressed leave their SM2 bits set and ignore the subsequent data bytes.

address of all don't cares. This effectively disables the automatic addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

## 6.7 Serial Peripheral Interface (SPI)

### 6.7.1 SPI features

- Master or slave operation
- 10 MHz bit frequency (max)
- LSB first or MSB first data transfer
- Four programmable bit rates
- End of transmission (SPIF)
- Write-collision flag protection (WCOL)
- Wake-up from Idle mode (Slave mode only)

### 6.7.2 SPI description

The serial peripheral interface allows high-speed synchronous data transfer between the P89CV51RB2/RC2/RD2 and peripheral devices or between several P89CV51RB2/RC2/RD2 devices. Figure 16 shows the correspondence between master and slave SPI devices. The SPICLK pin is the clock output and input for the Master and Slave modes, respectively. The SPI clock generator will start following a write to the master devices SPI data register. The written data is then shifted out of the MOSI pin of the master device into the MOSI pin of the slave device. Following a complete transmission of one byte of data, the SPI clock generator is stopped and the SPI interrupt Flag (SPIF) is set. An SPI interrupt request will be generated if the SPI Interrupt Enable bit (SPIE) and the SPI interrupt enable bit, ES, are both set.

An external master drives the Slave Select input pin ($\overline{SS}$) LOW to select the SPI module as a slave. If $\overline{SS}$ has not been driven LOW, then the slave SPI unit is not active and the MOSI pin can also be used as an input port pin.

CPHA and CPOL control the phase and polarity of the SPI clock (SCK). Figure 17 and Figure 18 show the four possible combinations of these two bits.

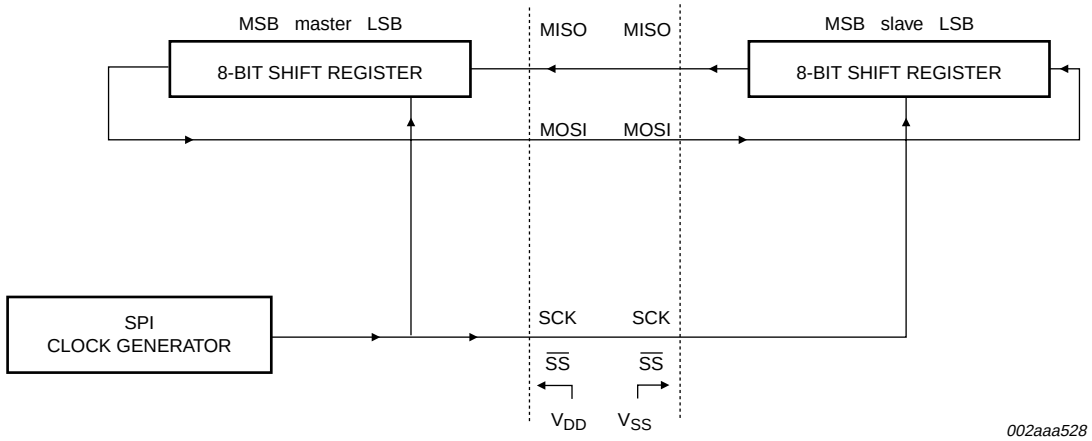



**Fig 16. SPI master-slave interconnection**

**Table 27. SPCR - SPI control register (address D5H) bit allocation**

*Reset source(s): any reset; reset value: 0000 0000B.*

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | SPIE | SPEN | DORD | MSTR | CPOL | CPHA | SPR1 | SPR0 |

**Table 28. SPCR - SPI control register (address D5H) bit description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | SPIE | SPI interrupt enable. If both SPIE = 1 and ES = 1, SPI interrupts are enabled. |
| 6 | SPEN | SPI enable bit. When set enables SPI. |
| 5 | DORD | Data transmission order. 0 = MSB first; 1 = LSB first in data transmission. |
| 4 | MSTR | Master/Slave select. 1 = Master mode, 0 = Slave mode. |
| 3 | CPOL | Clock polarity. 1 = SPICLK is HIGH when idle (active LOW), 0 = SPICLK is LOW when idle (active HIGH). |
| 2 | CPHA | Clock Phase control bit. 1 = shift-triggered on the trailing edge of the clock; 0 = shift-triggered on the leading edge of the clock. |
| 1 | SPR1 | SPI clock Rate select bit 1. Along with SPR0 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave; see Table 29. |
| 0 | SPR0 | SPI clock Rate select bit 0. Along with SPR1 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave; see Table 29. |

**Table 29. SPCR - SPI control register (address D5H) clock rate selection**

| SPR1 | SPR0 | SPICLK = $f_{osc}$ divided by | |
|---|---|---|---|
| | | 6-clock mode | 12-clock mode |
| 0 | 0 | 2 | 4 |
| 0 | 1 | 8 | 16 |
| 1 | 0 | 32 | 64 |
| 1 | 1 | 64 | 128 |

way to disable the WDT, except through a reset (either a hardware reset or a WDT overflow reset). When the WDT overflows, it will drive an output reset HIGH pulse at the RST pin.

When the WDT is enabled (and thus running) the user needs to reset it by writing 01EH and 0E1H, in sequence, to the WDTRST SFR to avoid WDT overflow. The 14-bit counter reaches overflow when it reaches 16383 (3FFFH) and this will reset the device.

The WDT's counter cannot be read or written. When the WDT overflows it will generate an output pulse at the RST pin with a duration of 98 oscillator periods in 6-clock mode or 196 oscillator periods in 12-clock mode.

## 6.9 PCA

The PCA includes a special 16-bit timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse-width modulator. Each module has a pin associated with it: Module 0 is connected to CEX0, module 1 to CEX1, etc. Registers CH and CL contain the current value of the free-running up-counting 16-bit PCA timer. The PCA timer is a common time base for all five modules and can be programmed to run at: $\frac{1}{6}$ the oscillator frequency, $\frac{1}{2}$ the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1[2]). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR; see Table 32 and Table 33.

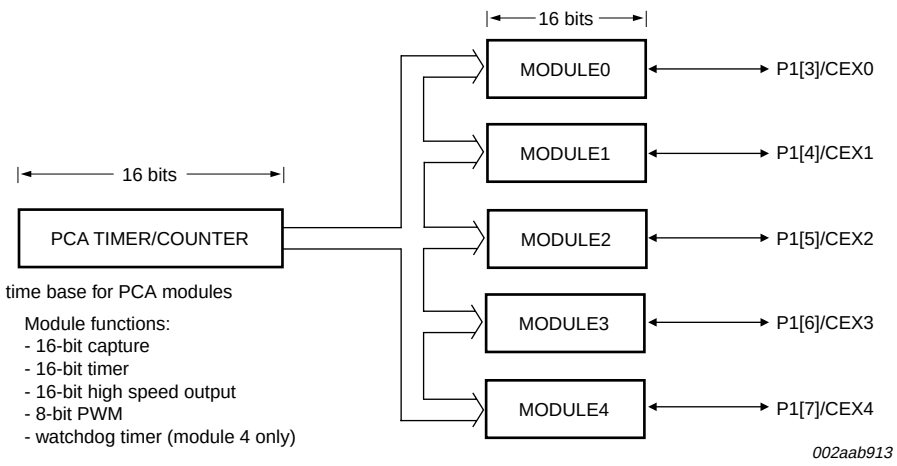



**Fig 19. PCA**

In the CMOD SFR there are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during Idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The watchdog timer function is implemented in module 4 of PCA.

The CCON SFR contains the run control bit for the PCA (CR) and the flags for the PCA timer (CF) and each module (CCF[4:0]). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD

register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags can only be cleared by software. All the modules share one interrupt vector. The PCA interrupt system is shown in Figure 20.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. The registers contain the bits that control the mode that each module will operate in.

The ECCF bit (from CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on the module) enables the CCFn flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module; see Figure 20.

PWM (CCAPMn.1) enables the PWM mode.

The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.

The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.

The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode, these registers are used to control the duty cycle of the output.

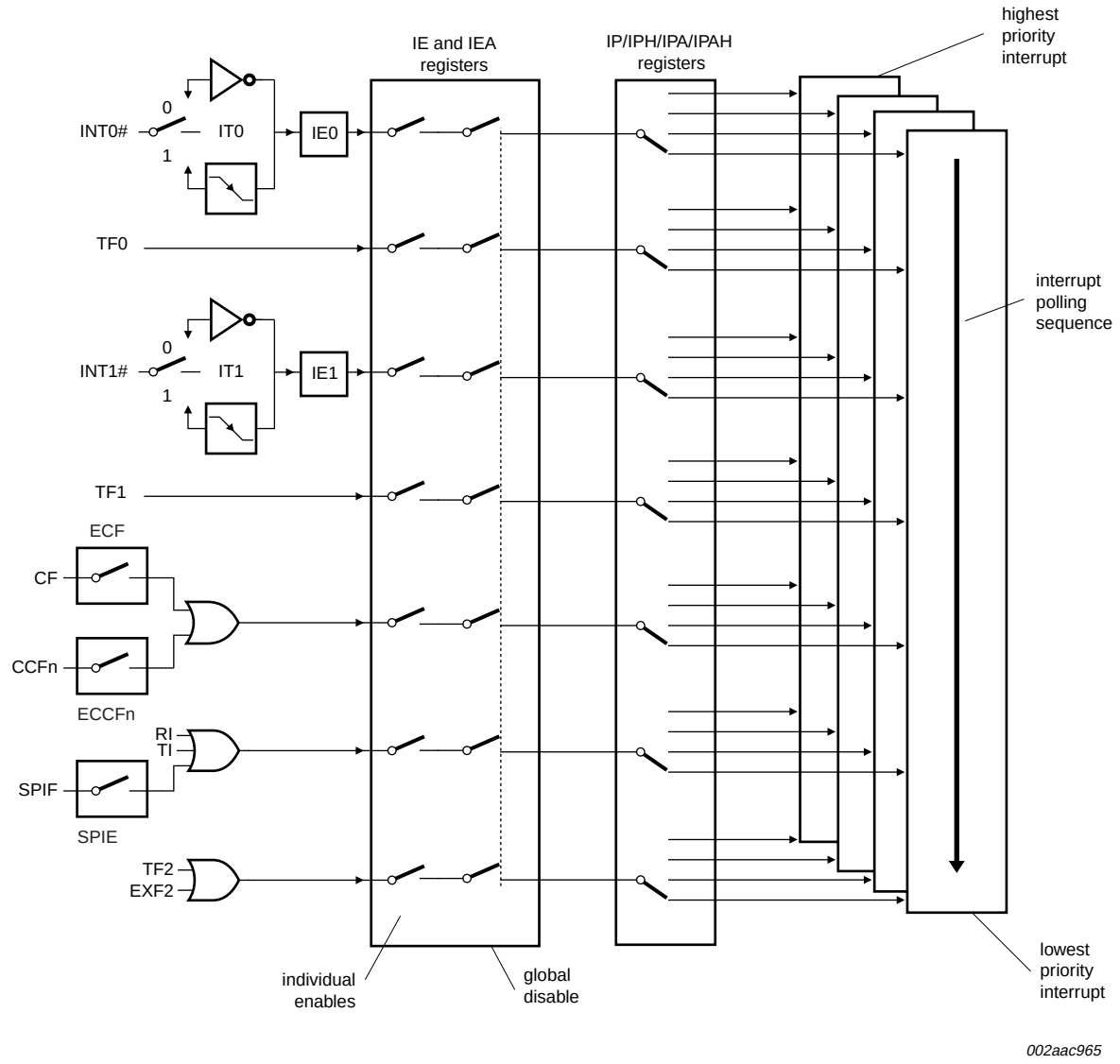



**Fig 25. Interrupt structure**

**Table 42. IE - Interrupt enable register 0 (address A8H) bit allocation**

*Bit addressable; reset value: 00H.*

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | EA | EC | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

**Table 43. IE - Interrupt enable register 0 (address A8H) bit description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | EA | Interrupt Enable. EA = 1: interrupt(s) can be serviced; EA = 0: interrupt servicing disabled. |
| 6 | EC | PCA interrupt Enable. |
| 5 | ET2 | Timer 2 interrupt Enable. |

**Table 43. IE - Interrupt enable register 0 (address A8H) bit description** *...continued*

| Bit | Symbol | Description |
|---|---|---|
| 4 | ES | Serial port interrupt Enable. |
| 3 | ET1 | Timer 1 overflow interrupt Enable. |
| 2 | EX1 | External interrupt 1 Enable. |
| 1 | ET0 | Timer 0 overflow interrupt Enable. |
| 0 | EX0 | External interrupt 0 Enable. |

**Table 44. IP - Interrupt priority low register (address B8H) bit allocation**

*Bit addressable; reset value: 00H.*

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | PPC | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

**Table 45. IP - Interrupt priority low register (address B8H) bit description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | - | Reserved for future use. Should be set to 0 by user programs. |
| 6 | PPC | PCA interrupt Priority Low. |
| 5 | PT2 | Timer 2 interrupt Priority Low. |
| 4 | PS | Serial Port interrupt Priority Low. |
| 3 | PT1 | Timer 1 interrupt Priority Low. |
| 2 | PX1 | External interrupt 1 Priority Low. |
| 1 | PT0 | Timer 0 interrupt Priority Low. |
| 0 | PX0 | External interrupt 0 Priority Low. |

**Table 46. IPH - Interrupt priority high register (address B7H) bit allocation**

*Not bit addressable; reset value: 00H.*

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Symbol | - | PPCH | PT2H | PSH | PT1H | PX1H | PT0H | PX0H |

**Table 47. IPH - Interrupt priority high register (address B7H) bit description**

| Bit | Symbol | Description |
|---|---|---|
| 7 | - | Reserved for future use. Should be set to 0 by user programs. |
| 6 | PPCH | PCA interrupt Priority High. |
| 5 | PT2H | Timer 2 interrupt Priority High. |
| 4 | PSH | Serial Port interrupt Priority High. |
| 3 | PT1H | Timer 1 interrupt Priority High. |
| 2 | PX1H | External interrupt 1 Priority High. |
| 1 | PT0H | Timer 0 interrupt Priority High. |
| 0 | PX0H | External interrupt 0 Priority High. |

## 6.12 Power-saving modes

The device provides two power-saving modes of operation for applications where power consumption is critical. The two modes are Idle and Power-down; see Table 48.

### 6.12.1 Idle mode

Idle mode is entered by setting the IDL bit in the PCON register. In Idle mode, the program counter is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits Idle mode through either a system interrupt or a hardware reset. When exiting Idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits Idle mode. After exiting the Interrupt Service Routine (ISR), the interrupted program resumes execution at the instruction immediately following the instruction which invoked the Idle mode. A hardware reset starts the device similar to a power-on reset.

### 6.12.2 Power-down mode

The Power-down mode is entered by setting the PD bit in the PCON register. In the Power-down mode, the clock is stopped and external interrupts are active for level-sensitive interrupts only. SRAM contents are retained during power-down, the minimum $V_{DD}$ level is 4.5 V.

The device exits Power-down mode through either an enabled external level-sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding an external interrupt pin LOW restarts the oscillator, the signal must hold LOW at least 1024 clock cycles before bringing back HIGH to complete the exit. When the interrupt signal is restored to logic $V_{IH}$, the interrupt service routine program execution resumes at the instruction immediately following the instruction which invoked Power-down mode. A hardware reset starts the device similar to a power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the $V_{DD}$ line is restored to its normal operating voltage. Be sure to hold $V_{DD}$ voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

**Table 48. Power-saving modes**

| Mode | Initiated by | State of MCU | Exited by |
|---|---|---|---|
| Idle | Software (Set IDL bit in PCON)<br>MOV PCON, #01H | CLK is running. Interrupts, serial port and timers/counters are active. Program counter is stopped. ALE and $\overline{PSEN}$ signals at a HIGH-state during Idle. All registers remain unchanged. | Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits Idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked Idle mode. A hardware reset restarts the device similar to a power-on reset. |
| Power-down | Software (Set PD bit in PCON)<br>MOV PCON, #02H | CLK is stopped. On-chip SRAM and SFR data is maintained. ALE and $\overline{PSEN}$ signals at a LOW-state during power-down. External interrupts are only active for level-sensitive interrupts, if enabled. | Enabled external level-sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits Power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked Power-down mode. A hardware reset restarts the device similar to a power-on reset. |

# 7. Limiting values

**Table 53. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Parameters are valid over operating temperature range unless otherwise specified; all voltages are with respect to $V_{SS}$ unless otherwise noted.*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{amb(bias)}$ | bias ambient temperature | | –55 | +125 | °C |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $V_I$ | input voltage | on $\overline{EA}$ pin to $V_{SS}$ | –0.5 | +14 | V |
| $V_n$ | voltage on any other pin | except $V_{SS}$; with respect to $V_{DD}$ | –0.5 | $V_{DD}$ + 0.5 | V |
| $I_{OL(I/O)}$ | LOW-level output current per input/output pin | | - | 15 | mA |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | - | 1.5 | W |

# 8. Static characteristics

**Table 54. Static characteristics**

*$T_{amb}$ = −40 °C to +85 °C; $V_{DD}$ = 4.5 V to 5.5 V; $V_{SS}$ = 0 V.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $n_{endu(fl)}$ | endurance of flash memory | JEDEC Standard A117 | [1] | 10000 | - | - | cycles |
| $t_{ret(fl)}$ | flash memory retention time | JEDEC Standard A103 | [1] | 100 | - | - | years |
| $I_{latch}$ | I/O latch-up current | JEDEC Standard 78 | [1] | 100 + $I_{DD}$ | - | - | mA |
| $V_{th(HL)}$ | HIGH-LOW threshold voltage | | | –0.5 | - | +0.2$V_{DD}$ – 0.1 | V |
| $V_{th(LH)}$ | LOW-HIGH threshold voltage | except XTAL1, RST | | 0.2$V_{DD}$ + 0.9 | - | $V_{DD}$ + 0.5 | V |
| $V_{OL}$ | LOW-level output voltage | $V_{DD}$ = 4.5 V; except $\overline{PSEN}$, ALE | [2][3][4] | | | | |
| | | $I_{OL}$ = 1.6 mA | | - | - | 0.4 | V |
| | | $V_{DD}$ = 4.5 V; ALE, $\overline{PSEN}$ | | | | | |
| | | $I_{OL}$ = 3.2 mA | | - | - | 0.45 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_{DD}$ = 4.5 V; ports 1, 2, 3, 4 | [5] | | | | |
| | | $I_{OH}$ = –30 µA | | $V_{DD}$ – 0.7 | - | - | V |
| | | $V_{DD}$ = 4.5 V; port 0 in External bus mode, ALE, $\overline{PSEN}$ | | | | | |
| | | $I_{OH}$ = –3.2 mA | | $V_{DD}$ – 0.7 | - | - | V |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0.4 V; ports 1, 2, 3, 4 | | –1 | - | –75 | µA |
| $I_{THL}$ | HIGH-LOW transition current | $V_I$ = 2 V; ports 1, 2, 3, 4 | [6] | - | - | –650 | µA |
| $I_{LI}$ | input leakage current | 0.45 V < $V_I$ < $V_{DD}$ – 0.3 V; port 0 | | - | - | ±10 | µA |
| | | 0 V < $V_I$ < 6 V | | - | - | 10 | µA |

**Table 54. Static characteristics** *…continued*

*$T_{amb}$ = −40 °C to +85 °C; $V_{DD}$ = 4.5 V to 5.5 V; $V_{SS}$ = 0 V.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{pd}$ | pull-down resistance | on pin RST | | 40 | - | 225 | kΩ |
| $C_{iss}$ | input capacitance | 1 MHz; $T_{amb}$ = 25 °C; $V_I$ = 0 V | [7] | - | - | 15 | pF |
| $I_{DD(oper)}$ | operating supply current | $f_{osc}$ = 12 MHz | | - | - | 11.5 | mA |
| | | $f_{osc}$ = 40 MHz | | - | - | 50 | mA |
| | | Programming and erase mode | | - | - | 70 | mA |
| $I_{DD(idle)}$ | Idle mode supply current | $f_{osc}$ = 12 MHz | | - | - | 8.5 | mA |
| | | $f_{osc}$ = 40 MHz | | - | - | 42 | mA |
| $I_{DD(pd)}$ | Power-down mode supply current | minimum $V_{DD}$ = 4.5 V | | - | - | 90 | µA |

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2] Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:

a) Maximum $I_{OL}$ per 8-bit port: 26 mA

b) Maximum $I_{OL}$ total for all outputs: 71 mA

c) If $I_{OL}$ exceeds the test condition, $V_{OH}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[3] Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the $V_{OL}$ of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

[4] Load capacitance for Port 0, ALE and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

[5] Capacitive loading on Ports 0 and 2 may cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall below the $V_{DD}$ − 0.7 V specification when the address bits are stabilizing.

[6] Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when $V_I$ is approximately 2 V.

[7] Pin capacitance is characterized but not tested. Capacitance on pin $\overline{EA}$ = 25 pF (max.).

## 9.1 Explanation of symbols

Each timing symbol used in Figure 29 to Figure 33 has 5 characters. The first character is always a 't' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

**A** — Address

**C** — Clock

**D** — Input data

**H** — Logic level HIGH

**I** — Instruction (program memory contents)

**L** — Logic level LOW or ALE

**P** — $\overline{\text{PSEN}}$

**Q** — Output data

**R** — $\overline{\text{RD}}$ signal

**T** — cycle Time

**V** — Valid

**W** — $\overline{\text{WR}}$ signal

**X** — No longer a valid logic level

**Z** — High impedance (float)

Example:

$t_{AVLL}$ = Address valid to ALE LOW time

$t_{LLPL}$ = ALE LOW to $\overline{\text{PSEN}}$ LOW time

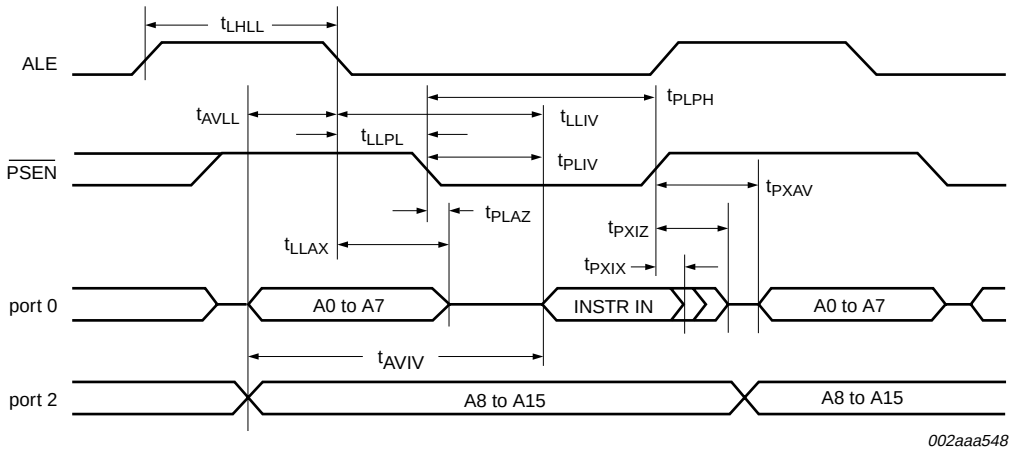



**Fig 29. External program memory read cycle**

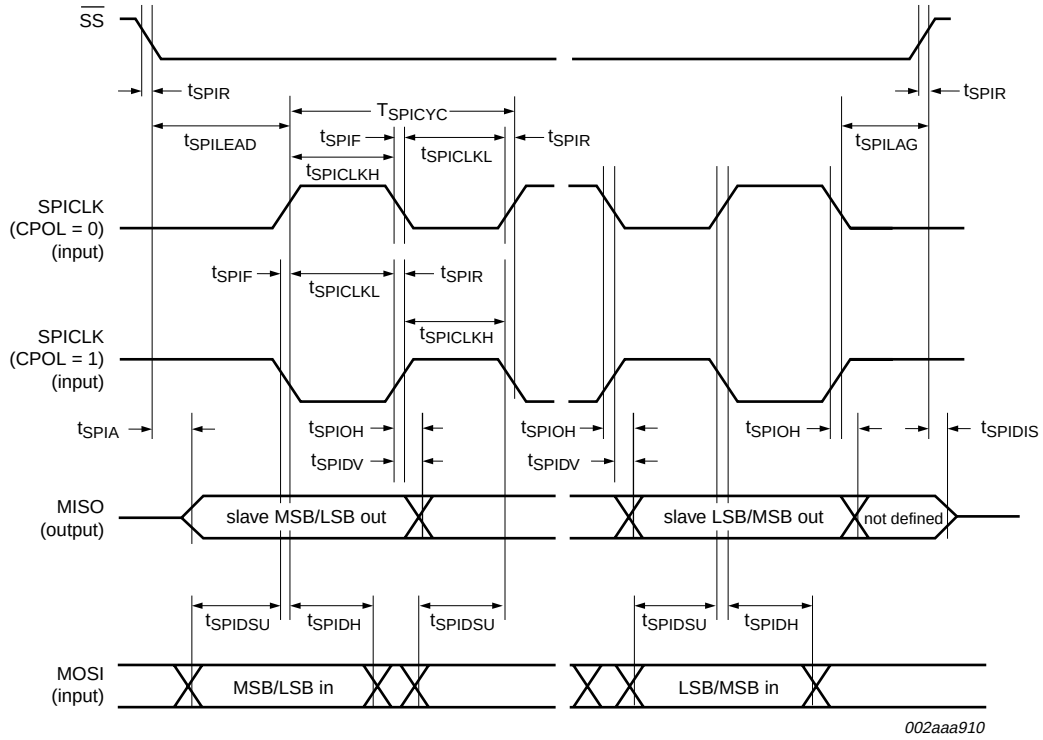



**Fig 36. SPI slave timing (CPHA = 0)**

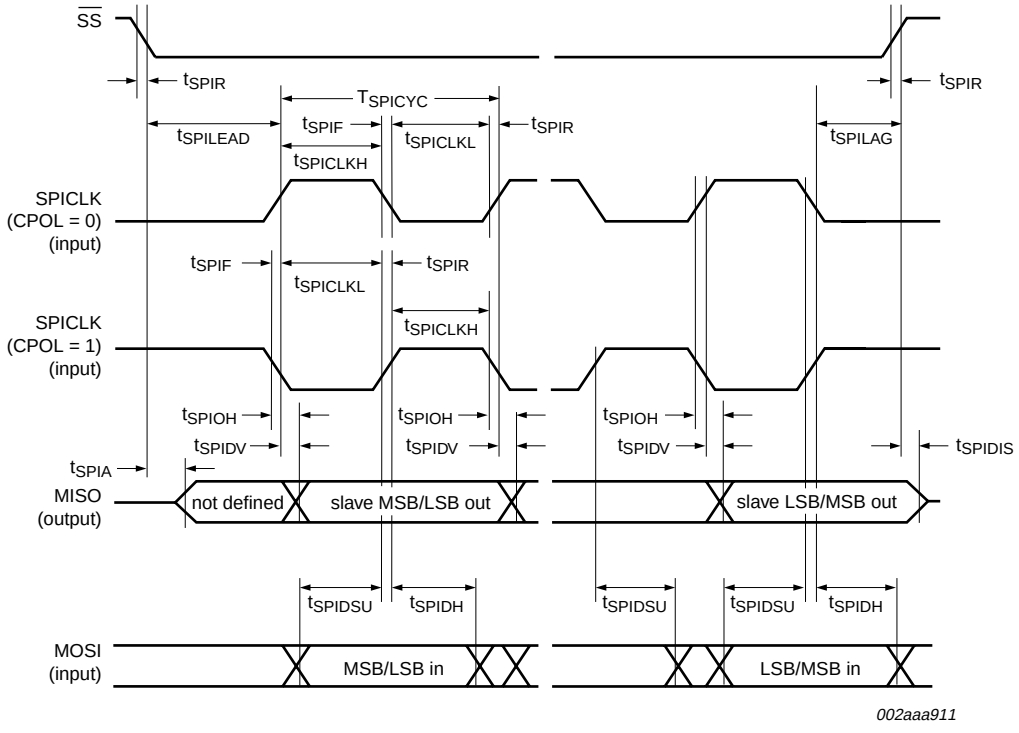
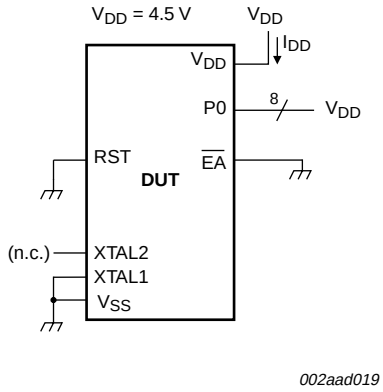



**Fig 37. SPI slave timing (CPHA = 1)**




All other pins disconnected

**Fig 41. $I_{DD}$ test condition, Power-down mode**