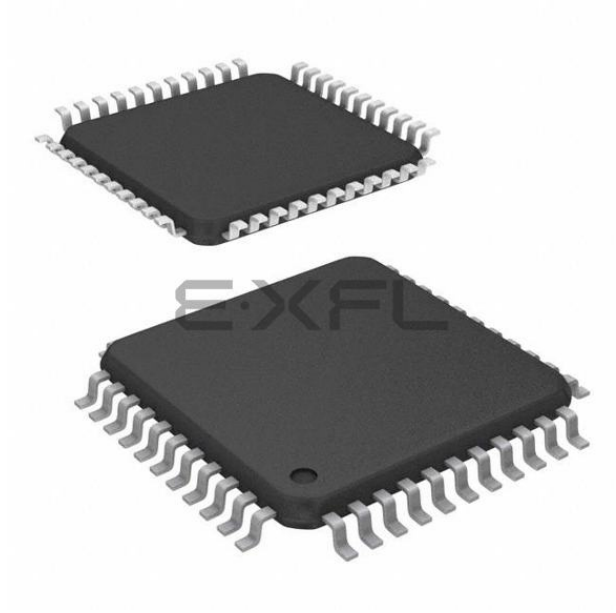

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89cv51rb2fbc-557

Table 3. P89CV51RB2/RC2/RD2 Pin description *...continued*

Symbol	Pin		Type	Description
	PLCC44	TQFP44		
P2[1]/A9	25	19	I/O	**P2[1] —** Port 2 bit 1.
			O	**A9 —** Address bit 9.
P2[2]/A10	26	20	I/O	**P2[2] —** Port 2 bit 2.
			O	**A10 —** Address bit 10.
P2[3]/A11	27	21	I/O	**P2[3] —** Port 2 bit 3.
			O	**A11 —** Address bit 11.
P2[4]/A12	28	22	I/O	**P2[4] —** Port 2 bit 4.
			O	**A12 —** Address bit 12.
P2[5]/A13	29	23	I/O	**P2[5] —** Port 2 bit 5.
			O	**A13 —** Address bit 13.
P2[6]/A14	30	24	I/O	**P2[6] —** Port 2 bit 6.
			O	**A14 —** Address bit 14.
P2[7]/A15	31	25	I/O	**P2[7] —** Port 2 bit 7.
			O	**A15 —** Address bit 15.
P3[0] to P3[7]			I/O with internal pull-up	**Port 3**: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins are pulled HIGH by the internal pull-ups when 1s are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups.
P3[0]/RXD	11	5	I/O	**P3[0] —** Port 3 bit 0.
			I	**RXD —** Serial input port.
P3[1]/TXD	13	7	I/O	**P3[1] —** Port 3 bit 1.
			O	**TXD —** Serial output port.
P3[2]/$\overline{\text{INT0}}$	14	8	I/O	**P3[2] —** Port 3 bit 2.
			I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
P3[3]/$\overline{\text{INT1}}$	15	9	I/O	**P3[3] —** Port 3 bit 3.
			I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P3[4]/T0	16	10	I/O	**P3[4] —** Port 3 bit 4.
			I	**T0 —** External count input to timer/counter 0.
P3[5]/T1	17	11	I/O	**P3[5] —** Port 3 bit 5.
			I	**T1 —** External count input to timer/counter 1.
P3[6]/$\overline{\text{WR}}$	18	12	I/O	**P3[6] —** Port 3 bit 6.
			O	**$\overline{\text{WR}}$ —** External data memory write strobe.
P3[7]/$\overline{\text{RD}}$	19	13	I/O	**P3[7] —** Port 3 bit 7.
			O	**$\overline{\text{RD}}$ —** External data memory read strobe.
$\overline{\text{PSEN}}$	32	26	O	**Program Store Enable**: $\overline{\text{PSEN}}$ is the read strobe for external program memory. When the device is executing from internal program memory, $\overline{\text{PSEN}}$ is inactive (HIGH). When the device is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR address	Bit functions and addresses[1]							
			MSB							LSB
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**
SPCR	SPI Control Register	D5H	SPIE	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
SPSR	SPI Status Register	AAH	SPIF	WCOL	-	-	-	-	-	-
SPDAT	SPI Data	86H	-	-	-	-	-	-	-	-
SP	Stack Pointer	81H	-	-	-	-	-	-	-	-
		Bit address	**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**
TCON*	Timer/counter Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
		Bit address	**CF**	**CE**	**CD**	**CC**	**CB**	**CA**	**C9**	**C8**
T2CON*	Timer/counter 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/$\overline{RL}$2
T2MOD	Timer 2 Mode control	C9H	-	-	-	-	-	-	T2OE	DCEN
TH0	Timer 0 High	8CH	-	-	-	-	-	-	-	-
TH1	Timer 1 High	8DH	-	-	-	-	-	-	-	-
TH2	Timer 2 High	CDH	-	-	-	-	-	-	-	-
TL0	Timer 0 Low	8AH	-	-	-	-	-	-	-	-
TL1	Timer 1 Low	8BH	-	-	-	-	-	-	-	-
TL2	Timer 2 Low	CCH	-	-	-	-	-	-	-	-
TMOD	Timer/counter 0 and 1 Mode	89H	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0
WDTRST	WatchDog Timer Reset	A6H	-	-	-	-	-	-	-	-

[1] Unimplemented bits in SFRs (labeled '-') are 'X' (unknown) at all times. Unless otherwise specified, 1s should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are 0s although they are unknown when read.

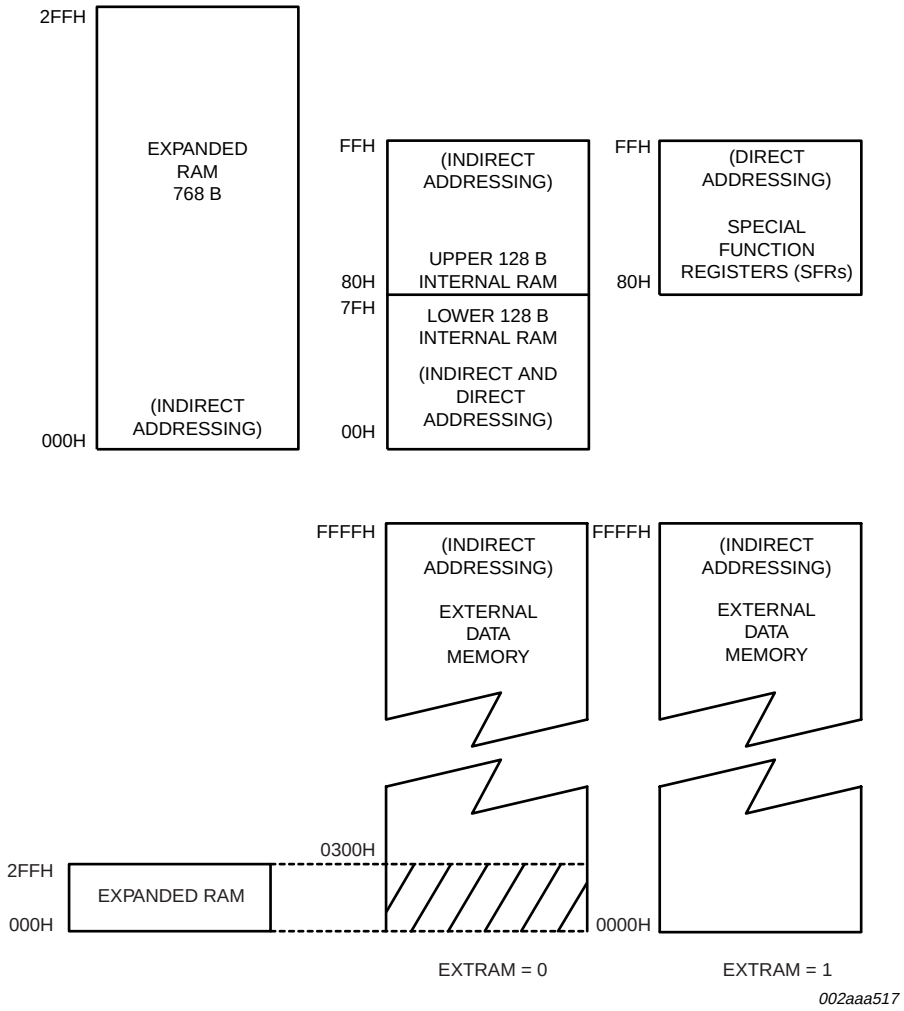


Fig 4. Internal and external data memory structure

6.2.2 Dual data pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS = 0, DPTR0 is selected; when DPS = 1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1; see Figure 5.

Table 12. IAP function calls *…continued*

IAP function	IAP call parameters
Program status bit, boot vector, 6×/12× bit	**Input parameters:** R1 = 06H or 86H (WDT feed) DPL = 00H = program status bit DPL = 01H = program boot vector DPL = 02H = 6×/12× bit ACC = boot vector value to program **Return parameter(s):** ACC = 00: pass ACC is not 00: fail
Read security bits, status bit, boot vector	**Input parameters:** ACC = 07H or 87H (WDT feed) DPL = 00H = security bits DPL = 01H = status bit DPL = 02H = boot vector **Return parameter(s):** ACC = 00 SoftICE S/N-match 0 SB 0 DBL_CLK
Erase page	**Input parameters:** R1 = 08H or 88H (WDT feed) DPH = page address high byte DPL = page address low byte **Return parameter(s):** ACC = 00: pass ACC is not 00: fail

6.4 Timers/counters 0 and 1

The two 16-bit timer/counter registers: Timer 0 and Timer 1 can be configured to operate either as timers or event counters (see Table 13 and Table 14).

In the ‘Timer’ function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of six oscillator periods, the count rate is $\frac{1}{6}$ of the oscillator frequency.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once every machine cycle.

When the samples show a HIGH in one cycle and a LOW in the next cycle, the count is incremented. The new count value appears in the register in the machine cycle following the one in which the transition was detected. Since it takes two machine cycles (12 oscillator periods) for a 1-to-0 transition to be recognized, the maximum count rate is $\frac{1}{12}$ of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle. In addition to the ‘Timer’ or ‘Counter’ selection, Timer 0 and Timer 1 have four selectable operating modes.

The ‘Timer’ or ‘Counter’ function is selected by control bits C/$\overline{T}$ in the special function register TMOD. These two timers/counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both timers/counters. Mode 3 is different. The four operating modes are described in the following text.

Table 13. TMOD - Timer/Counter mode control register (address 89H) bit allocation

Not bit addressable; reset value: 0000 0000B; reset source(s): any source.

Bit	7	6	5	4	3	2	1	0
Symbol	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

Table 14. TMOD - Timer/Counter mode control register (address 89H) bit description

Bit	Symbol	Description
7	T1GATE	Gating control for Timer 1. When set, timer/counter is enabled only while the $\overline{INT1}$ pin is HIGH and the TR1 control bit is set. When cleared, Timer 1 is enabled when the TR1 control bit is set.
6	T1C/$\overline{T}$	Timer or counter select for Timer 1. Cleared for timer operation. Set for counter operation (input from T1 input pin).
5	T1M1	Mode select for Timer 1.
4	T1M0	
3	T0GATE	Gating control for Timer 0. When set, timer/counter is enabled only while the $\overline{INT0}$ pin is HIGH and the TR0 control bit is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
2	T0C/$\overline{T}$	Timer or counter select for Timer 0. Cleared for timer operation. Set for counter operation (input from T0 input pin).
1	T0M1	Mode select for Timer 0.
0	T0M0	

Table 15. TMOD - Timer/Counter mode control register (address 89H) M1/M0 operating mode

M1	M0	Operating mode	
0	0	0	8048 timer ‘TLx’ serves as 5-bit prescaler.
0	1	1	16-bit timer/counter ‘THx’ and ‘TLx' are cascaded; there is no prescaler.
1	0	2	8-bit auto-reload timer/counter ‘THx’ holds a value which is to be reloaded into ‘TLx’ each time it overflows.
1	1	3	(Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	3	(Timer 1) timer/counter 1 stopped.

Table 16. TCON - Timer/Counter control register (address 88H) bit allocation

Bit addressable; reset value: 0000 0000B; reset source(s): any reset.

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

6.4.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register (THn and TLn) are used; see Figure 8.

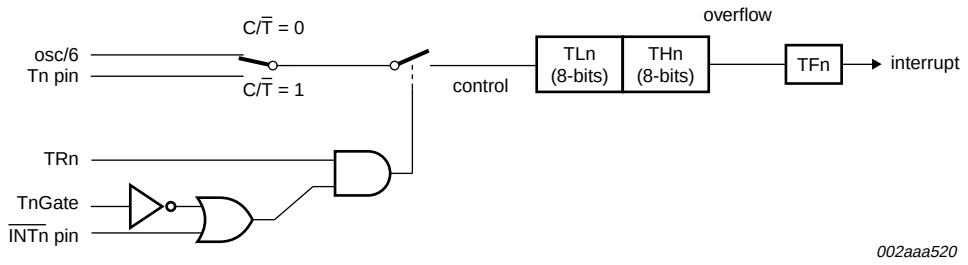


Fig 8. Timer/counter 0 or 1 in Mode 1 (16-bit counter)

6.4.3 Mode 2

Mode 2 configures the timer register as an 8-bit counter (TLn) with automatic reload, as shown in Figure 9. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

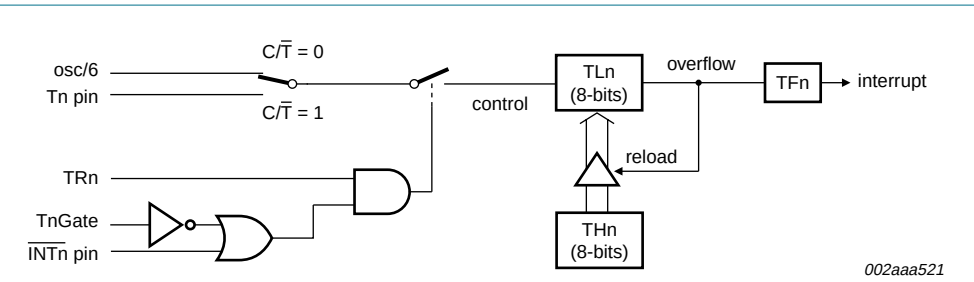


Fig 9. Timer/counter 0 or 1 in Mode 2 (8-bit auto-reload)

6.4.4 Mode 3

When Timer 1 is in Mode 3 it is stopped (holds its count). The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for Mode 3 and Timer 0 is shown in Figure 10. TL0 uses the Timer 0 control bits: T0C/$\overline{T}$, T0GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in mode 3, the P89CV51RB2/RC2/RD2 can look like it has an additional timer.

Note: When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it into and out of its own Mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

6.5.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1[0], Clock-out mode). This pin, besides being a regular I/O pin, has two additional functions. It can be programmed:

1. To input the external clock for timer/counter 2, or
2. To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the timer/counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{OscillatorFrequency}{2 \times (65536 - (RCAP2H, RCAP2L))} \quad (2)$$

Where (RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud rate generator.

6.5.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART transmit and receive baud rates to be derived from either Timer 1 or Timer 2; see Section 6.6 for details. When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When TCLK = 1, Timer 2 is used as the UART transmit baud rate generator. RCLK has the same effect for the UART receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates, Timer 1 or Timer 2.

Figure 14 shows Timer 2 in Baud rate generator mode:

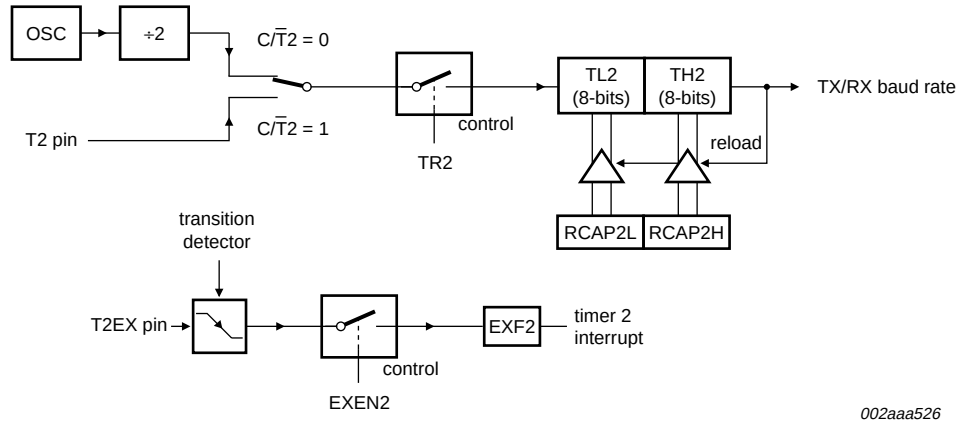


Fig 14. Timer 2 in Baud rate generator mode

The Baud rate generator mode is like the Auto-reload mode, when a roll-over in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

Modes 1 and 3 baud rates = Timer 2 overflow rate / 16

The timer can be configured for either 'timer' or 'counter' operation. In many applications, it is configured for 'timer' operation (C/$\overline{T}$2 = 0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment at every machine cycle (i.e., $\frac{1}{6}$ the oscillator frequency). As a baud rate generator, it increments at the oscillator frequency. Thus the baud rate formula is shown in Equation 3:

Modes 1 and 3 baud rates =

$$\frac{OscillatorFrequency}{16 \times (65536 - (RCAP2H, RCAP2L))} \quad (3)$$

Where: (RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 in Baud rate generator mode is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a roll-over in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the Baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is used as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the Baud rate generator mode, one should not try to read or write TH2 and TL2. Under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers. Table 23 shows commonly used baud rates and how they can be obtained from Timer 2.

6.5.5 Summary of baud rate equations

Timer 2 is in Baud rate generator mode: if Timer 2 is being clocked through pin T2 (P1[0]) the baud rate is:

Baud rate = Timer 2 overflow rate / 16

If Timer 2 is being clocked internally, the baud rate is:

Baud rate = f_{osc} / (16 × (65536 – (RCAP2H, RCAP2L)))

Where f_{osc} = oscillator frequency

To obtain the reload value for RCAP2H and RCAP2L, this equation can be rewritten as:

RCAP2H, RCAP2L = 65536 – f_{osc} / (16 × baud rate)

Table 23. Timer 2-generated commonly used baud rates

Rate	Oscillator frequency	Timer 2	
		RCAP2H	RCAP2L
750 kBd	12 MHz	FF	FF
19.2 kBd	12 MHz	FF	D9
9.6 kBd	12 MHz	FF	B2
4.8 kBd	12 MHz	FF	64
2.4 kBd	12 MHz	FE	C8
600 Bd	12 MHz	FB	1E
220 Bd	12 MHz	F2	AF
600 Bd	6 MHz	FD	8F
220 Bd	6 MHz	F9	57

6.6 UART

The UART operates in all standard modes. Enhancements over the standard 80C51 UART include framing error detection, and automatic address recognition.

6.6.1 Mode 0

Serial data enters and exits through RXD, and TXD outputs the shift clock. Only 8 bits are transmitted or received, LSB first. The baud rate is fixed at $1/6$ of the CPU clock frequency. The UART configured to operate in this mode outputs serial clock on the TXD line no matter whether it sends or receives data on the RXD line.

6.6.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When data is received, the stop bit is stored in RB8 in special function register SCON. The baud rate is variable and is determined by the Timer 1/Timer 2 overflow rate.

6.6.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). When data is transmitted, the 9th data bit (TB8 in special function register SCON) can be assigned the value of 0 or (e.g. the parity bit (P in special function register PSW) could be moved into bit TB8). When data is received, the 9th data bit goes into RB8 in special function register SCON, while the stop bit is ignored. The baud rate is programmable to either $1/16$ or $1/32$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

6.6.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in mode 3 is variable and is determined by the Timer 1/Timer 2 overflow rate.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit, although it is preferable to use the Framing Error flag (FE). When the UART receives data in Mode 1 and SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.6.9 Automatic address recognition

Automatic address recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled for the UART by setting the SM2 bit in SCON. In the 9-bit UART modes, Mode 2 and Mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the 'given' address or the 'broadcast' address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data.

Using the automatic address recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the broadcast address. Two special function registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are don't care. The SADEN mask can be logically ANDed with the SADDR to create the given address which the master will use for addressing each of the slaves. Use of the given address allows multiple slaves to be recognized while excluding others.

This device uses the methods presented in Figure 15 to determine if a given or broadcast address has been received or not.

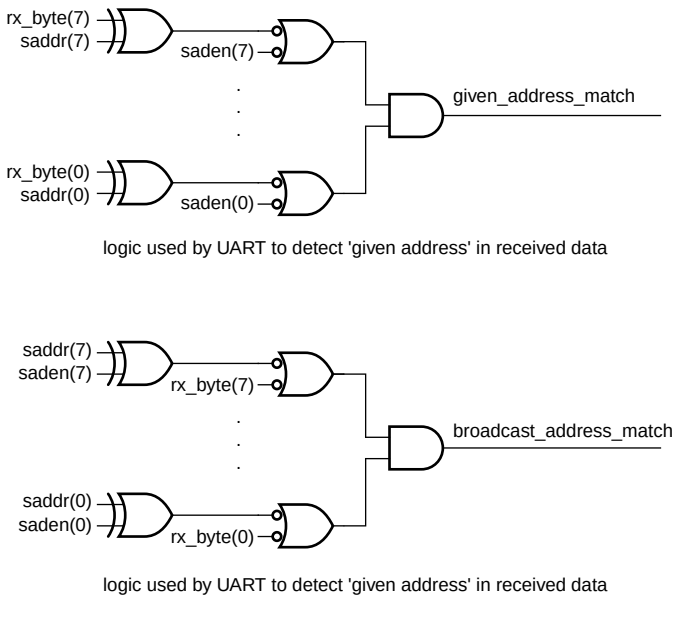


Fig 15. Schemes used by the UART to detect 'given' and 'broadcast' addresses when multiprocessor communications is enabled

The following examples help to show the versatility of this scheme.

Example 1, slave 0:

SADDR = 1100 0000
SADEN = 1111 1101
Given = 1100 00X0

Example 2, slave 1:

SADDR = 1100 0000
SADEN = 1111 1110
Given = 1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0.

Example 1, slave 0:

SADDR = 1100 0000
SADEN = 1111 1001
Given = 1100 0XX0

Example 2, slave 1:

SADDR = 1110 0000
SADEN = 1111 1010
Given = 1110 0X0X

Example 3, slave 2:

SADDR = 1100 0000
SADEN = 1111 1100
Given = 1100 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select slaves 0 and 1 and exclude slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2. The broadcast address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FFH. Upon reset SADDR and SADEN are loaded with 0s. This produces a given address of all don't cares as well as a broadcast

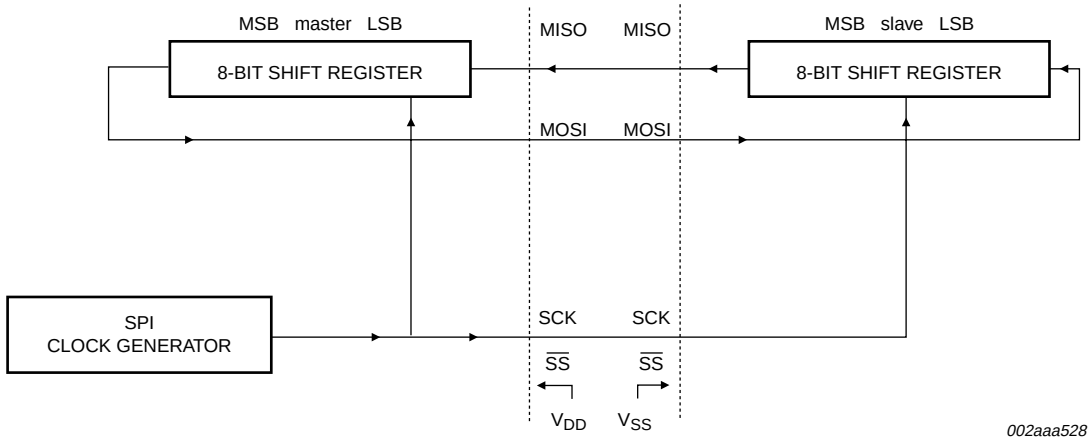


Fig 16. SPI master-slave interconnection

Table 27. SPCR - SPI control register (address D5H) bit allocation

Reset source(s): any reset; reset value: 0000 0000B.

Bit	7	6	5	4	3	2	1	0
Symbol	SPIE	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Table 28. SPCR - SPI control register (address D5H) bit description

Bit	Symbol	Description
7	SPIE	SPI interrupt enable. If both SPIE = 1 and ES = 1, SPI interrupts are enabled.
6	SPEN	SPI enable bit. When set enables SPI.
5	DORD	Data transmission order. 0 = MSB first; 1 = LSB first in data transmission.
4	MSTR	Master/Slave select. 1 = Master mode, 0 = Slave mode.
3	CPOL	Clock polarity. 1 = SPICLK is HIGH when idle (active LOW), 0 = SPICLK is LOW when idle (active HIGH).
2	CPHA	Clock Phase control bit. 1 = shift-triggered on the trailing edge of the clock; 0 = shift-triggered on the leading edge of the clock.
1	SPR1	SPI clock Rate select bit 1. Along with SPR0 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave; see Table 29.
0	SPR0	SPI clock Rate select bit 0. Along with SPR1 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave; see Table 29.

Table 29. SPCR - SPI control register (address D5H) clock rate selection

SPR1	SPR0	SPICLK = f_{osc} divided by	
		6-clock mode	12-clock mode
0	0	2	4
0	1	8	16
1	0	32	64
1	1	64	128

module's CCAPnL SFR, the output will be LOW; when it is equal to, or greater, the output will be HIGH. When CL overflows from FFH to 00H, CCAPnL is reloaded with the value in CCAPnH. This allows the PWM to be updated without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable PWM mode.

6.9.5 PCA watchdog timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 24 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven HIGH.

User's software then must periodically change (CCAP4H, CCAP4L) to keep a match from occurring with the PCA timer (CH, CL). This code is given in the subroutine WATCHDOG shown below.

In order to hold off the reset, the user has three options:

- Periodically change the compare value so it will never match the PCA timer.
- Periodically change the PCA timer value so it will never match the compare values.
- Disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in the third option. If the program counter ever reaches an undesired value, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember that the PCA timer is the time base for **all** modules; changing the time base for other modules is not recommended. Thus, in most applications the first option is best.

```
;CALL the following WATCHDOG subroutine periodically.
   CLR    EA           ;Hold off interrupts
   MOV    CCAP4L,#00   ;Next compare value is within 255 counts of
                        current PCA timer value
   MOV    CCAP4H,CH
   SETB   EA           ;Re-enable interrupts
   RET
```

Do not use this routine as part of an interrupt service routine, because if the program counter would enter an infinite loop, still interrupts will be serviced and the watchdog will continually keep getting reset. Because this would defeat the purpose of the watchdog, it is recommended that this subroutine is called from the main program within 2^{16} PCA timer counts.

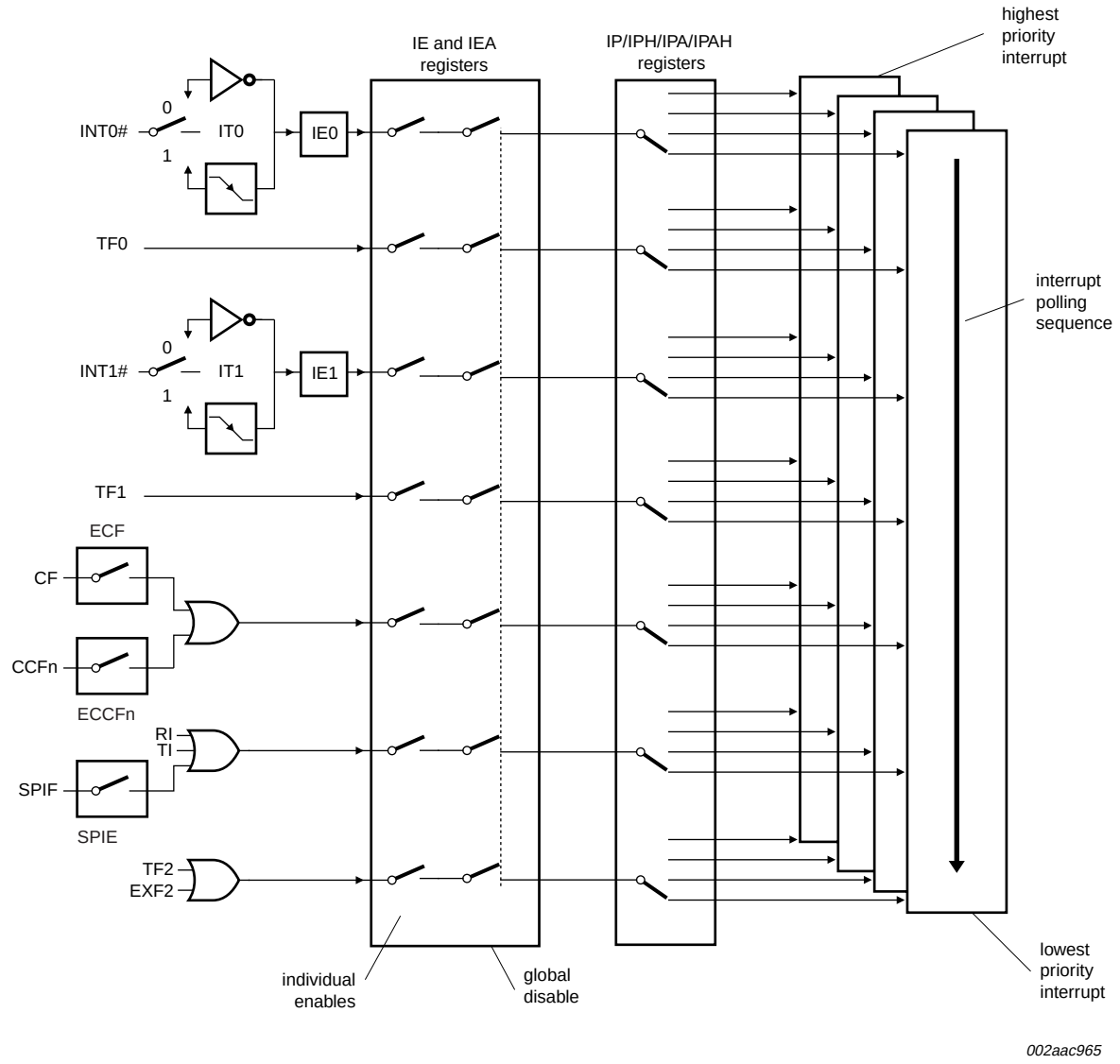


Fig 25. Interrupt structure

Table 42. IE - Interrupt enable register 0 (address A8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Table 43. IE - Interrupt enable register 0 (address A8H) bit description

Bit	Symbol	Description
7	EA	Interrupt Enable. EA = 1: interrupt(s) can be serviced; EA = 0: interrupt servicing disabled.
6	EC	PCA interrupt Enable.
5	ET2	Timer 2 interrupt Enable.

6.12 Power-saving modes

The device provides two power-saving modes of operation for applications where power consumption is critical. The two modes are Idle and Power-down; see Table 48.

6.12.1 Idle mode

Idle mode is entered by setting the IDL bit in the PCON register. In Idle mode, the program counter is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits Idle mode through either a system interrupt or a hardware reset. When exiting Idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits Idle mode. After exiting the Interrupt Service Routine (ISR), the interrupted program resumes execution at the instruction immediately following the instruction which invoked the Idle mode. A hardware reset starts the device similar to a power-on reset.

6.12.2 Power-down mode

The Power-down mode is entered by setting the PD bit in the PCON register. In the Power-down mode, the clock is stopped and external interrupts are active for level-sensitive interrupts only. SRAM contents are retained during power-down, the minimum V_{DD} level is 4.5 V.

The device exits Power-down mode through either an enabled external level-sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding an external interrupt pin LOW restarts the oscillator, the signal must hold LOW at least 1024 clock cycles before bringing back HIGH to complete the exit. When the interrupt signal is restored to logic V_{IH}, the interrupt service routine program execution resumes at the instruction immediately following the instruction which invoked Power-down mode. A hardware reset starts the device similar to a power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

Table 48. Power-saving modes

Mode	Initiated by	State of MCU	Exited by
Idle	Software (Set IDL bit in PCON) MOV PCON, #01H	CLK is running. Interrupts, serial port and timers/counters are active. Program counter is stopped. ALE and $\overline{PSEN}$ signals at a HIGH-state during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits Idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked Idle mode. A hardware reset restarts the device similar to a power-on reset.
Power-down	Software (Set PD bit in PCON) MOV PCON, #02H	CLK is stopped. On-chip SRAM and SFR data is maintained. ALE and $\overline{PSEN}$ signals at a LOW-state during power-down. External interrupts are only active for level-sensitive interrupts, if enabled.	Enabled external level-sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits Power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked Power-down mode. A hardware reset restarts the device similar to a power-on reset.

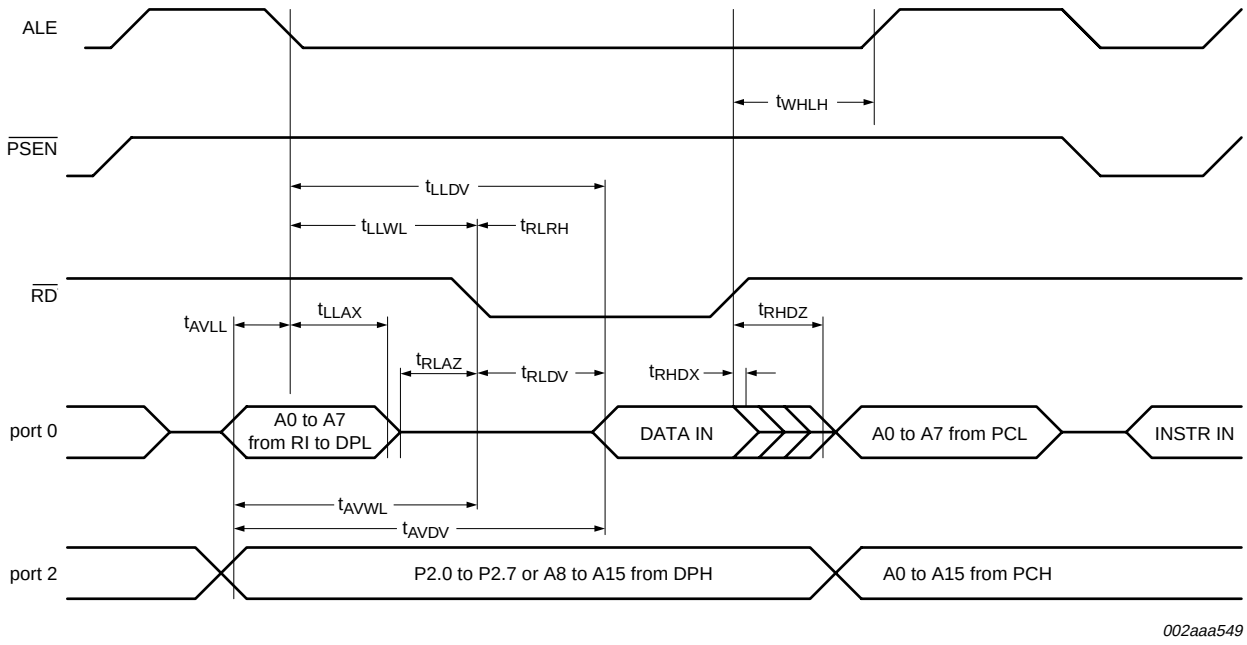


Fig 30. External data memory read cycle

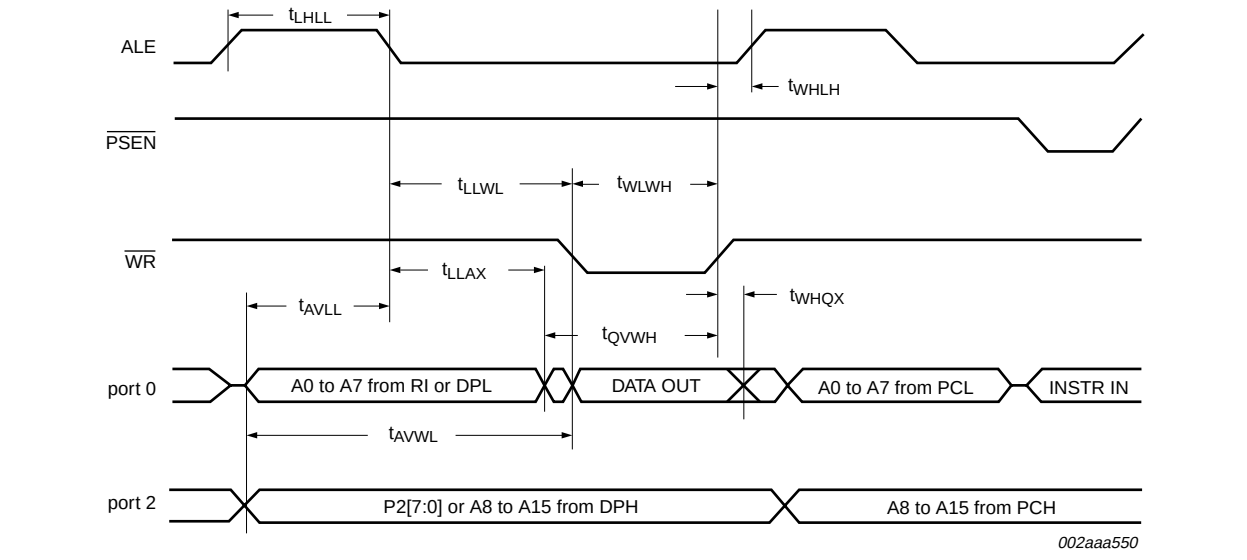


Fig 31. External data memory write cycle

Table 56. External clock drive

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
f_{osc}	oscillator frequency	-	-	0	40	MHz
$T_{cy(clk)}$	clock cycle time	25	-	-	-	ns
t_{CHCX}	clock HIGH time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCX}	clock LOW time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCH}	clock rise time	-	10	-	-	ns
t_{CHCL}	clock fall time	-	10	-	-	ns

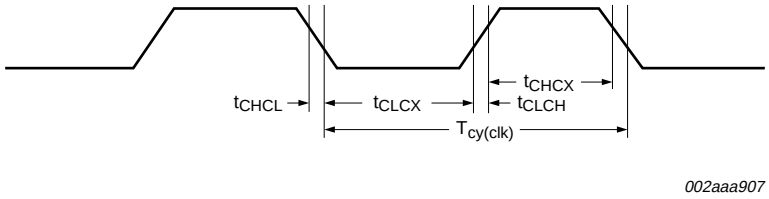


Fig 32. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

Table 57. Serial port timing

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	serial port clock cycle time	0.3	-	$12T_{cy(clk)}$	-	µs
t_{QVXH}	output data set-up to clock rising edge time	117	-	$10T_{cy(clk)} - 133$	-	ns
t_{XHQX}	output data hold after clock rising edge time	0	-	$2T_{cy(clk)} - 50$	-	ns
t_{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t_{XHDV}	input data valid to clock rising edge time	-	117	-	$10T_{cy(clk)} - 133$	ns

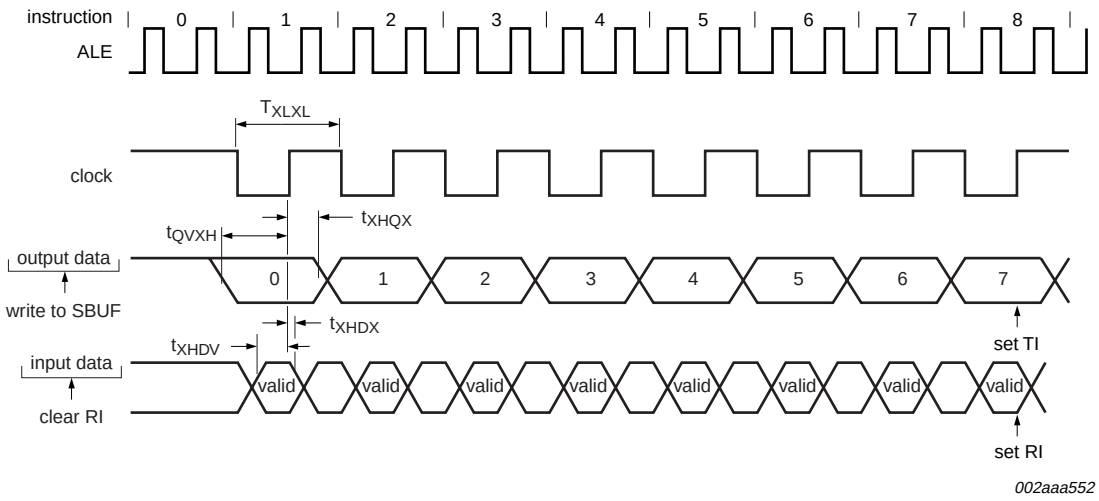
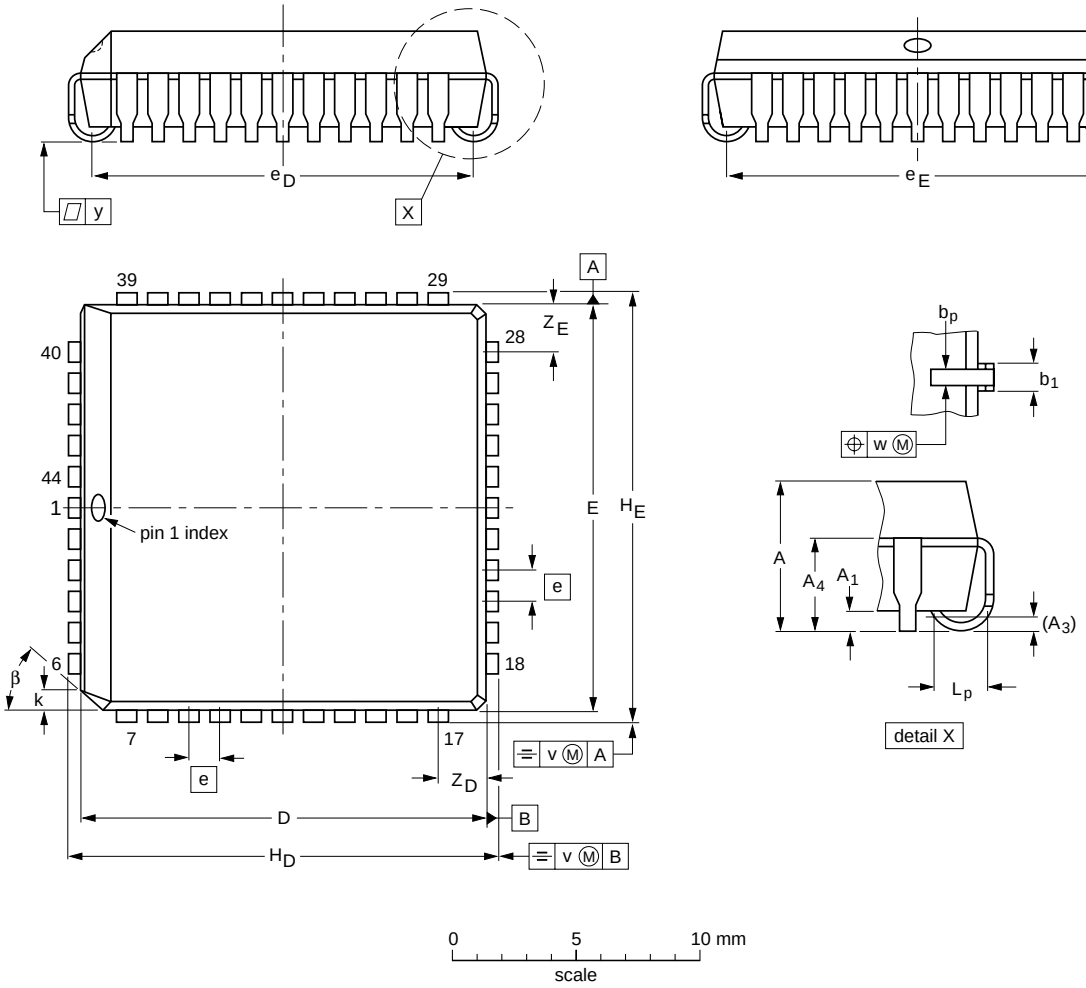


Fig 33. Shift register mode timing waveforms

Table 58. SPI interface timing

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
f_{SPI}	SPI operating frequency		0	$T_{cy(clk)}$ / 4	0	10	MHz
T_{SPICYC}	SPI cycle time	see Figure 34, 35, 36, 37	$4T_{cy(clk)}$	-	222	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 36, 37	250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 36, 37	250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 34, 35, 36, 37	$2T_{cy(clk)}$	-	111	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 34, 35, 36, 37	$2T_{cy(clk)}$	-	111	-	ns
t_{SPIDSU}	SPI data set-up time	master or slave; see Figure 34, 35, 36, 37	100	-	100	-	ns
t_{SPIDH}	SPI data hold time	master or slave; see Figure 34, 35, 36, 37	100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 36, 37	0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 36, 37	0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 34, 35, 36, 37	-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 34, 35, 36, 37	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 34, 35, 36, 37					
		SPI outputs (SPICLK, MOSI, MISO)	-	100	-	100	ns
		SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)	-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 34, 35, 36, 37					
		SPI outputs (SPICLK, MOSI, MISO)	-	100	-	100	ns
		SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)	-	2000	-	2000	ns

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 43. Package outline SOT187-2 (PLCC44)

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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