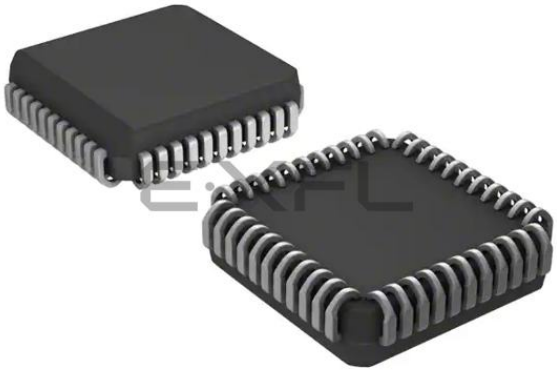

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89cv51rc2fa-512

Table 3. P89CV51RB2/RC2/RD2 Pin description *...continued*

Symbol	Pin		Type	Description
	PLCC44	TQFP44		
RST	10	4	I	**Reset**: While the oscillator is running, a HIGH logic state on this pin for two machine cycles will reset the device.
$\overline{EA}$	35	29	I	**External Access Enable**: $\overline{EA}$ must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. $\overline{EA}$ must be strapped to V_{DD} for internal program execution.
ALE	33	27	I/O	**Address Latch Enable**: ALE is the output signal for latching the low byte of the address during an access to external memory. Normally the ALE[1] is emitted at a constant rate of $\frac{1}{6}$ the crystal frequency[2] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if bit AO is set to 1, ALE is disabled.
XTAL1	21	15	I	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	20	14	O	**Crystal 2**: Output from the inverting oscillator amplifier.
V_{DD}	44	38	supply	**Power supply**
V_{SS}	22	16	supply	**Ground**

[1] ALE loading issue: When ALE pin experiences higher loading (> 30 pF) during the reset, the microcontroller may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor from 3 kΩ to 50 kΩ between e.g., ALE pin and V_{DD}.

[2] For 6-clock mode, ALE is emitted at $\frac{1}{3}$ of crystal frequency.

Table 4. Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR address	Bit functions and addresses[1]							
			MSB							LSB
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0
ACC*	Accumulator	E0H	-	-	-	-	-	-	-	-
AUXR	Auxiliary function Register	8EH	-	-	-	-	-	-	EXTRAM	AO
AUXR1	Auxiliary function Register 1	A2H	-	-	ENBOOT	-	GF2	0	-	DPS
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0
B*	B register	F0H	-	-	-	-	-	-	-	-
CCAP0H	Module 0 Capture High	FAH	-	-	-	-	-	-	-	-
CCAP1H	Module 1 Capture High	FBH	-	-	-	-	-	-	-	-
CCAP2H	Module 2 Capture High	FCH	-	-	-	-	-	-	-	-
CCAP3H	Module 3 Capture High	FDH	-	-	-	-	-	-	-	-
CCAP4H	Module 4 Capture High	FEH	-	-	-	-	-	-	-	-
CCAP0L	Module 0 Capture Low	EAH	-	-	-	-	-	-	-	-
CCAP1L	Module 1 Capture Low	EBH	-	-	-	-	-	-	-	-
CCAP2L	Module 2 Capture Low	ECH	-	-	-	-	-	-	-	-
CCAP3L	Module 3 Capture Low	EDH	-	-	-	-	-	-	-	-
CCAP4L	Module 4 Capture Low	EEH	-	-	-	-	-	-	-	-
CCAPM0	Module 0 mode	DAH	-	ECOM_0	CAPP_0	CAPN_0	MAT_0	TOG_0	PWM_0	ECCF_0
CCAPM1	Module 1 mode	DBH	-	ECOM_1	CAPP_1	CAPN_1	MAT_1	TOG_1	PWM_1	ECCF_1
CCAPM2	Module 2 mode	DCH	-	ECOM_2	CAPP_2	CAPN_2	MAT_2	TOG_2	PWM_2	ECCF_2
CCAPM3	Module 3 mode	DDH	-	ECOM_3	CAPP_3	CAPN_3	MAT_3	TOG_3	PWM_3	ECCF_3
CCAPM4	Module 4 mode	DEH	-	ECOM_4	CAPP_4	CAPN_4	MAT_4	TOG_4	PWM_4	ECCF_4
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8
CCON*	PCA Counter Control	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0
CH	PCA Counter High	F9H	-	-	-	-	-	-	-	-
CL	PCA Counter Low	E9H	-	-	-	-	-	-	-	-
CMOD	PCA Counter Mode	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF
CKCON	Clock Control	8FH	SPIX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

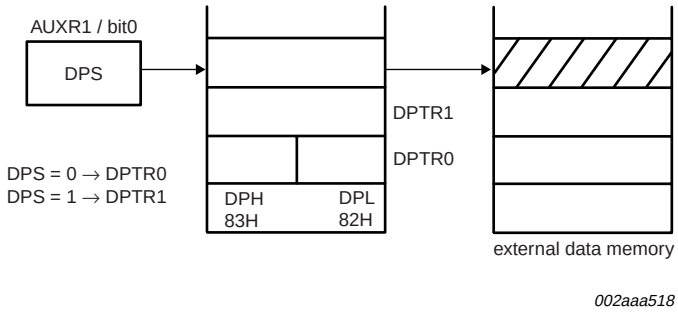

Fig 5. Dual data pointer organization

Table 8. AUXR1 - Auxiliary function register 1 (address A2H) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	ENBOOT	-	GF2	0	-	DPS

Table 9. AUXR1 - Auxiliary function register 1 (address A2H) bit description

Bit	Symbol	Description
7, 6, 4	-	Reserved for future use. Should be set to 0 by user programs.
5	ENBOOT	Enable BOOTROM
3	GF2	General purpose user-defined Flag.
2	0	This bit contains a hard-wired 0. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should be set to 0 by user programs.
0	DPS	Data Pointer Select. Chooses one of two data pointers for use by the program. See text for details.

6.2.3 Reset

At initial power-up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins HIGH. Powering up the device without a valid reset could cause the MCU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash. A system reset will not affect the on-chip RAM while the device is running, however, the contents of the on-chip RAM during power-up are indeterminate.

When power is applied to the device, the RST pin must be held HIGH long enough for the oscillator to start-up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement an RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2 kΩ resistor as shown in Figure 6.

During initial power-up the POF flag in the PCON register is set to indicate an initial power-up condition. The POF flag will remain active until cleared by software.

Table 11. ISP Hex record formats *…continued*

Record type	Command/data function
03	Miscellaneous write functions :nnxxxx03ffssddcc Where: nn = number of bytes in the record xxxx = required field but value is a don't care ff = subfunction code ss = selection code dd = data (if needed) cc = checksum Subfunction code = 0C (erase 4 kB blocks) ff = 0C ss = block code, as shown below: block 0, 0 kB to 4 kB, 00H block 1, 4 kB to 8 kB, 10H block 2, 8 kB to 12 kB, 20H block 3, 12 kB to 16 kB, 30H block 4, 16 kB to 20 kB, 40H (only available on P89CV51RC2/RD2) block 5, 20 kB to 24 kB, 50H (only available on P89CV51RC2/RD2) block 6, 24 kB to 28 kB, 60H (only available on P89CV51RC2/RD2) block 7, 28 kB to 32 kB, 70H (only available on P89CV51RC2/RD2) block 8, 32 kB to 36 kB, 80H (only available on P89CV51RD2) block 9, 36 kB to 40 kB, 90H (only available on P89CV51RD2) block 10, 40 kB to 44 kB, A0H (only available on P89CV51RD2) block 11, 44 kB to 48 kB, B0H (only available on P89CV51RD2) block 12, 48 kB to 52 kB, C0H (only available on P89CV51RD2) block 13, 52 kB to 56 kB, D0H (only available on P89CV51RD2) block 14, 56 kB to 60 kB, E0H (only available on P89CV51RD2) block 15, 60 kB to 64 kB, F0H (only available on P89CV51RD2) Example: :020000030C20CF (erase 4 kB block #2)

Table 11. ISP Hex record formats *…continued*

Record type	Command/data function
03 (continued)	Subfunction code = 01 (erase blocks) ff = 01 ss = block code, as shown below block 0, 0 kB to 8 kB, 00H block 1, 8 kB to 16 kB, 20H block 2, 16 kB to 32 kB, 40H block 3, 32 kB to 48 kB, 80H block 4, 48 kB to 64 kB, C0H Subfunction code = 04 (erase boot vector and status bit) ff = 04 ss = don't care Subfunction code = 05 (program security bits) ff = 05 ss = 00 program security bit 1 ss = 01 program security bit 2 ss = 02 program security bit 3 Subfunction code = 06 (program status bit, boot vector, 6×/12× bit) ff = 06 dd = data (for boot vector) ss = 00 program status bit ss = 01 program boot vector ss = 02 program 6×/12× bit Subfunction code = 07 (chip erase) Erases code memory and security bits, programs default boot vector and status bit ff = 07 Subfunction code = 08 (erase page, 128 B) ff = 08 ss = high byte of page address (A[15:8]) dd = low byte of page address (A[7:0]) Example: :0300000308E000F2 (erase page at E000H)

Table 12. IAP function calls *…continued*

IAP function	IAP call parameters
Erase 8 kB/16 kB code block	**Input parameters:** R1 = 01H or 81H (WDT feed) DPH = 00H, block 0, 0 kB to 8 kB DPH = 20H, block 1, 8 kB to 16 kB DPH = 40H, block 2, 16 kB to 32 kB DPH = 80H, block 3, 32 kB to 48 kB DPH = C0H, block 4, 48 kB to 64 kB **Return parameter(s):** ACC = 00: pass ACC is not 00: fail
Program user code	**Input parameters:** R1 = 02H or 82H (WDT feed) DPH = memory address MSB DPL = memory address LSB ACC = byte to program **Return parameter(s):** ACC = 00: pass ACC is not 00: fail
Read user code	**Input parameters:** R1 = 03H or 83H (WDT feed) DPH = memory address MSB DPL = memory address LSB **Return parameter(s):** ACC = device data
Erase status bit and boot vector	**Input parameters:** R1 = 04H or 84H (WDT feed) DPL = don’t care DPH = don’t care **Return parameter(s):** ACC = 00: pass ACC is not 00: fail
Program security bits	**Input parameters:** R1 = 05H or 85H (WDT feed) DPL = 00H = security bit 1 DPL = 01H = security bit 2 DPL = 02H = security bit 3 **Return parameter(s):** ACC = 00: pass ACC is not 00: fail

Table 17. TCON - Timer/Counter control register (address 88H) bit description

Bit	Symbol	Description
7	TF1	Timer 1 overflow Flag. Set by hardware on timer/counter overflow. Cleared by hardware when the processor vectors to Timer 1 interrupt routine, or by software.
6	TR1	Timer 1 Run control bit. Set/cleared by software to turn timer/counter 1 on/off.
5	TF0	Timer 0 overflow Flag. Set by hardware on timer/counter overflow. Cleared by hardware when the processor vectors to Timer 0 interrupt routine, or by software.
4	TR0	Timer 0 Run control bit. Set/cleared by software to turn timer/counter 0 on/off.
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge/LOW-state is detected. Cleared by hardware when the interrupt is processed, or by software.
2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/LOW-state that triggers external interrupt 1.
1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge/LOW-state is detected. Cleared by hardware when the interrupt is processed, or by software.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/LOW-state that triggers external interrupt 0.

6.4.1 Mode 0

Putting either timer into Mode 0 makes it look like an 8048 timer, which is an 8-bit counter with a fixed divide-by-32 prescaler. Figure 7 shows Mode 0 operation.

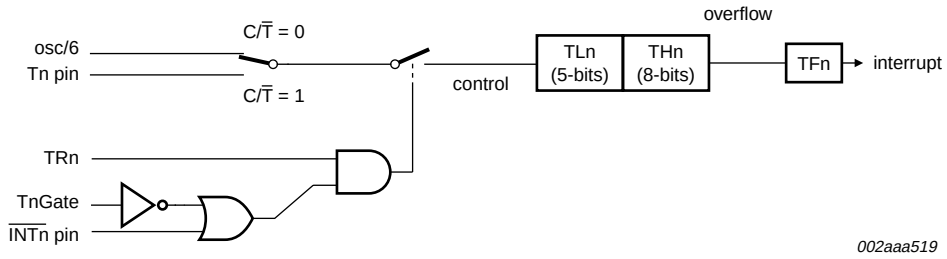

Fig 7. Timer/counter 0 or 1 in Mode 0 (13-bit counter)

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TFn. The count input is enabled to the timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the special function register TCON (Table 17). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 and Timer 1; see Figure 7. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

6.5.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1[0], Clock-out mode). This pin, besides being a regular I/O pin, has two additional functions. It can be programmed:

1. To input the external clock for timer/counter 2, or
2. To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the timer/counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{OscillatorFrequency}{2 \times (65536 - (RCAP2H, RCAP2L))} \quad (2)$$

Where (RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud rate generator.

6.5.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART transmit and receive baud rates to be derived from either Timer 1 or Timer 2; see Section 6.6 for details. When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When TCLK = 1, Timer 2 is used as the UART transmit baud rate generator. RCLK has the same effect for the UART receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates, Timer 1 or Timer 2.

Figure 14 shows Timer 2 in Baud rate generator mode:

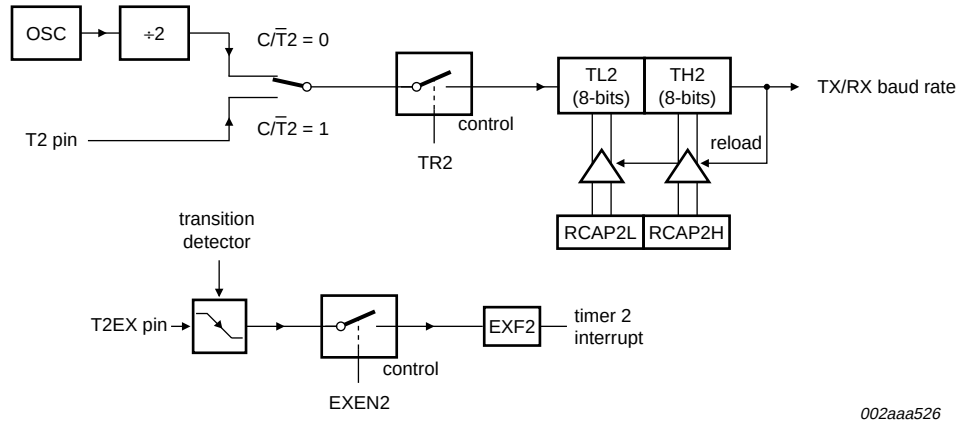

Fig 14. Timer 2 in Baud rate generator mode

Table 23. Timer 2-generated commonly used baud rates

Rate	Oscillator frequency	Timer 2	
		RCAP2H	RCAP2L
750 kBd	12 MHz	FF	FF
19.2 kBd	12 MHz	FF	D9
9.6 kBd	12 MHz	FF	B2
4.8 kBd	12 MHz	FF	64
2.4 kBd	12 MHz	FE	C8
600 Bd	12 MHz	FB	1E
220 Bd	12 MHz	F2	AF
600 Bd	6 MHz	FD	8F
220 Bd	6 MHz	F9	57

6.6 UART

The UART operates in all standard modes. Enhancements over the standard 80C51 UART include framing error detection, and automatic address recognition.

6.6.1 Mode 0

Serial data enters and exits through RXD, and TXD outputs the shift clock. Only 8 bits are transmitted or received, LSB first. The baud rate is fixed at $1/6$ of the CPU clock frequency. The UART configured to operate in this mode outputs serial clock on the TXD line no matter whether it sends or receives data on the RXD line.

6.6.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When data is received, the stop bit is stored in RB8 in special function register SCON. The baud rate is variable and is determined by the Timer 1/Timer 2 overflow rate.

6.6.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). When data is transmitted, the 9th data bit (TB8 in special function register SCON) can be assigned the value of 0 or (e.g. the parity bit (P in special function register PSW) could be moved into bit TB8). When data is received, the 9th data bit goes into RB8 in special function register SCON, while the stop bit is ignored. The baud rate is programmable to either $1/16$ or $1/32$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

6.6.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in mode 3 is variable and is determined by the Timer 1/Timer 2 overflow rate.

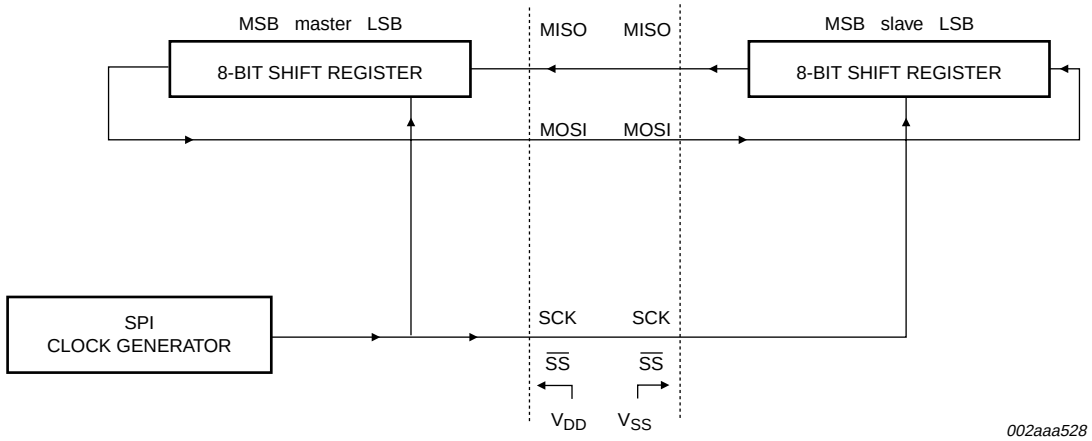

Fig 16. SPI master-slave interconnection

Table 27. SPCR - SPI control register (address D5H) bit allocation

Reset source(s): any reset; reset value: 0000 0000B.

Bit	7	6	5	4	3	2	1	0
Symbol	SPIE	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Table 28. SPCR - SPI control register (address D5H) bit description

Bit	Symbol	Description
7	SPIE	SPI interrupt enable. If both SPIE = 1 and ES = 1, SPI interrupts are enabled.
6	SPEN	SPI enable bit. When set enables SPI.
5	DORD	Data transmission order. 0 = MSB first; 1 = LSB first in data transmission.
4	MSTR	Master/Slave select. 1 = Master mode, 0 = Slave mode.
3	CPOL	Clock polarity. 1 = SPICLK is HIGH when idle (active LOW), 0 = SPICLK is LOW when idle (active HIGH).
2	CPHA	Clock Phase control bit. 1 = shift-triggered on the trailing edge of the clock; 0 = shift-triggered on the leading edge of the clock.
1	SPR1	SPI clock Rate select bit 1. Along with SPR0 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave; see Table 29.
0	SPR0	SPI clock Rate select bit 0. Along with SPR1 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave; see Table 29.

Table 29. SPCR - SPI control register (address D5H) clock rate selection

SPR1	SPR0	SPICLK = f_{osc} divided by	
		6-clock mode	12-clock mode
0	0	2	4
0	1	8	16
1	0	32	64
1	1	64	128

register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags can only be cleared by software. All the modules share one interrupt vector. The PCA interrupt system is shown in Figure 20.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. The registers contain the bits that control the mode that each module will operate in.

The ECCF bit (from CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on the module) enables the CCFn flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module; see Figure 20.

PWM (CCAPMn.1) enables the PWM mode.

The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.

The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.

The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode, these registers are used to control the duty cycle of the output.

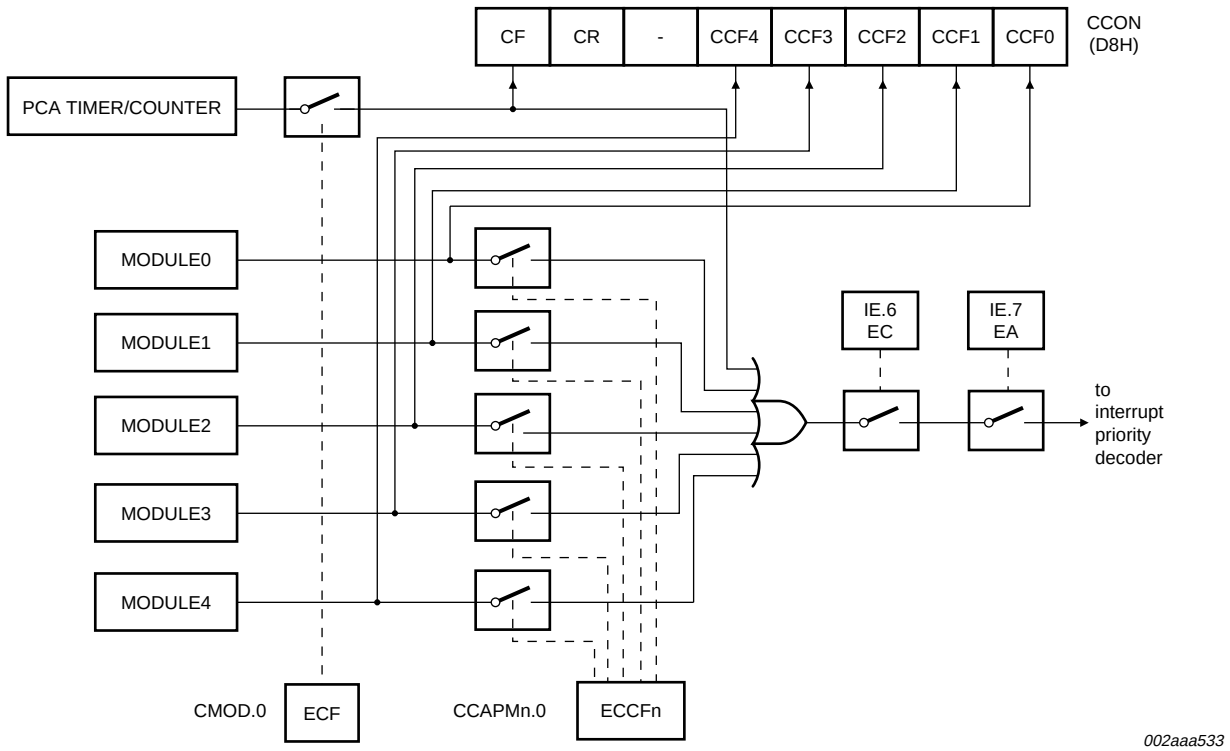

Fig 20. PCA interrupt system

Table 32. CMOD - PCA counter mode register (address D9H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF

Table 33. CMOD - PCA counter mode register (address D9H) bit description

Bit	Symbol	Description
7	CIDL	Counter Idle control. CIDL = 0 programs the PCA counter to continue functioning during Idle mode; CIDL = 1 programs it to be gated off during Idle mode.
6	WDTE	WatchDog Timer Enable. WDTE = 0 disables watchdog timer function on module 4; WDTE = 1 enables it.
5 to 3	-	Reserved for future use. Should be set to 0 by user programs.
2 to 1	CPS1, CPS0	PCA Count Pulse Select; see Table 34.
0	ECF	PCA Enable Counter overflow interrupt Flag. ECF = 1 enables CF bit in CCON to generate an interrupt; ECF = 0 disables that function.

Table 34. CMOD - PCA counter mode register (address D9H) count pulse select

CPS1	CPS0	Select PCA input
0	0	0 internal clock, f_{osc} / 6

module's CCAPnL SFR, the output will be LOW; when it is equal to, or greater, the output will be HIGH. When CL overflows from FFH to 00H, CCAPnL is reloaded with the value in CCAPnH. This allows the PWM to be updated without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable PWM mode.

6.9.5 PCA watchdog timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 24 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven HIGH.

User's software then must periodically change (CCAP4H, CCAP4L) to keep a match from occurring with the PCA timer (CH, CL). This code is given in the subroutine WATCHDOG shown below.

In order to hold off the reset, the user has three options:

- Periodically change the compare value so it will never match the PCA timer.
- Periodically change the PCA timer value so it will never match the compare values.
- Disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in the third option. If the program counter ever reaches an undesired value, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember that the PCA timer is the time base for **all** modules; changing the time base for other modules is not recommended. Thus, in most applications the first option is best.

```
;CALL the following WATCHDOG subroutine periodically.
   CLR    EA           ;Hold off interrupts
   MOV    CCAP4L,#00   ;Next compare value is within 255 counts of
                        current PCA timer value
   MOV    CCAP4H,CH
   SETB   EA           ;Re-enable interrupts
   RET
```

Do not use this routine as part of an interrupt service routine, because if the program counter would enter an infinite loop, still interrupts will be serviced and the watchdog will continually keep getting reset. Because this would defeat the purpose of the watchdog, it is recommended that this subroutine is called from the main program within 2^{16} PCA timer counts.

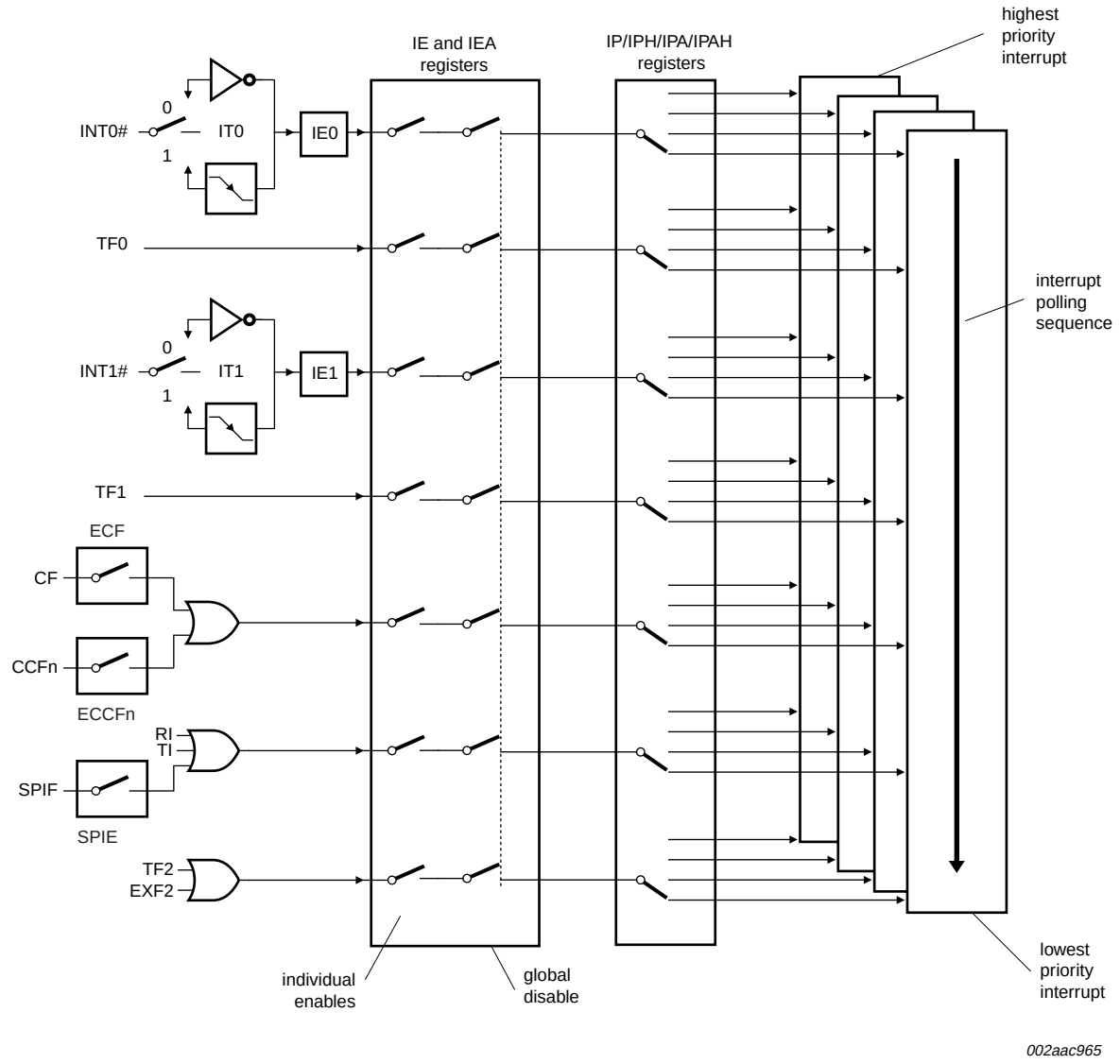

Fig 25. Interrupt structure

Table 42. IE - Interrupt enable register 0 (address A8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Table 43. IE - Interrupt enable register 0 (address A8H) bit description

Bit	Symbol	Description
7	EA	Interrupt Enable. EA = 1: interrupt(s) can be serviced; EA = 0: interrupt servicing disabled.
6	EC	PCA interrupt Enable.
5	ET2	Timer 2 interrupt Enable.

6.13 System clock and clock options

6.13.1 Clock input options and recommended capacitor values for oscillator

Shown in Figure 26 and Figure 27 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Resonator manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C_1 and C_2 should be adjusted appropriately for each design. Table 49 shows the typical values for C_1 and C_2 versus resonator type for various frequencies.

Table 49. Recommended values for C_1 and C_2 by crystal type

Resonator	$C_1 = C_2$
Quartz	20 pF to 30 pF
Ceramic	40 pF to 50 pF

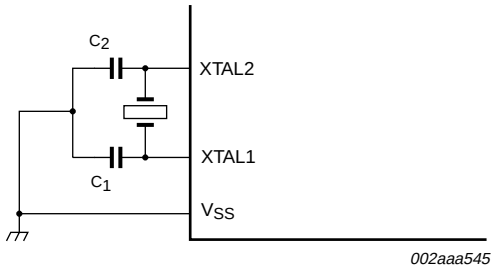

Fig 26. Oscillator characteristics (using the on-chip oscillator)

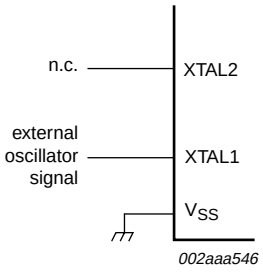

Fig 27. Oscillator characteristics (external clock drive)

6.13.1.1 Clock control register (CKCON)

By default, the device runs at twelve clock cycles per machine cycle (12-clock mode). The device may be run at 6 clock cycles per machine cycle (6-clock mode) by programming of either a non-volatile bit (FX2) or an SFR bit (X2); see Table 52 “Clock modes”. If the FX2 non-volatile bit is programmed, the device will run in 6-clock mode and the X2 SFR bit has no effect. If the FX2 bit is erased, then the clock mode is controlled by the X2 SFR bit.

Table 50. CKCON - Clock control register (address 8FH) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	SPIX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

Table 51. CKCON - Clock control register (address 8FH) bit description

Bit	Symbol	Description
7	SPIX2	SPI clock; 0 = 6 clock cycles for each SPI clock cycle; 1 = 12 clock cycles
6	WDX2	Watchdog clock; 0 = 6 clock cycles for each WDT clock cycle; 1 = 12 clock cycles
5	PCAX2	PCA clock; 0 = 6 clock cycles for each PCA clock cycle; 1 = 12 clock cycles
4	SIX2	UART clock; 0 = 6 clock cycles for each UART clock cycle; 1 = 12 clock cycles
3	T2X2	Timer 2 clock; 0 = 6 clock cycles for each Timer 2 clock cycle; 1 = 12 clock cycles
2	T1X2	Timer 1 clock; 0 = 6 clock cycles for each Timer 1 clock cycle; 1 = 12 clock cycles
1	T0X2	Timer 0 clock; 0 = 6 clock cycles for each Timer 0 clock cycle; 1 = 12 clock cycles
0	X2	CPU clock; 0 = 12 clock cycles for each machine cycle; 1 = 6 clock cycles

Table 52. Clock modes

FX2 clock mode bit	X2 bit	CPU clock mode	Peripheral clock mode bit (e.g. T0X2)	Mode
erased	0	12-clock (default)	X	12-clock (default)
	1	6-clock	0	6-clock
			1	12-clock
programmed	X	6-clock	0	6-clock
			1	12-clock

9. Dynamic characteristics

Table 55. Dynamic characteristics

Over operating conditions: load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

T_{amb} = −40 °C to +85 °C; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V.[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	12-clock mode	0	-	40	MHz
		6-clock mode	0	-	20	MHz
		IAP	0.25	-	40	MHz
t_{LHLL}	ALE pulse width		$2T_{cy(clk)} - 15$	-	-	ns
t_{AVLL}	address valid to ALE LOW time		$T_{cy(clk)} - 15$	-	-	ns
t_{LLAX}	address hold after ALE LOW time		$T_{cy(clk)} - 15$	-	-	ns
t_{LLIV}	ALE LOW to valid instruction in time		-	-	$4T_{cy(clk)} - 45$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW time		$T_{cy(clk)} - 15$	-	-	ns
t_{PLPH}	$\overline{PSEN}$ pulse width		$3T_{cy(clk)} - 15$	-	-	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in time		-	-	$3T_{cy(clk)} - 50$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$ time		0	-	-	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$ time		-	-	$T_{cy(clk)} - 15$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid time		$T_{cy(clk)} - 8$	-	-	ns
t_{AVIV}	address to valid instruction in time		-	-	$5T_{cy(clk)} - 60$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float time		-	-	10	ns
t_{RLRH}	$\overline{RD}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	-	ns
t_{WLWH}	$\overline{WR}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	-	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in time		-	-	$5T_{cy(clk)} - 50$	ns
t_{RHDX}	data hold after $\overline{RD}$ time		0	-	-	ns
t_{RHDZ}	data float after $\overline{RD}$ time		-	-	$2T_{cy(clk)} - 12$	ns
t_{LLDV}	ALE LOW to valid data in time		-	-	$8T_{cy(clk)} - 50$	ns
t_{AVDV}	address to valid data in time		-	-	$9T_{cy(clk)} - 75$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW time		$3T_{cy(clk)} - 15$	-	$3T_{cy(clk)} + 15$	ns
t_{AVWL}	address to $\overline{RD}$ or $\overline{WR}$ LOW time		$4T_{cy(clk)} - 30$	-	-	ns
t_{WHQX}	data hold after $\overline{WR}$ time		$T_{cy(clk)} - 20$	-	-	ns
t_{QVWH}	data output valid to $\overline{WR}$ HIGH time		$7T_{cy(clk)} - 50$	-	-	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float time		-	-	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH time		$T_{cy(clk)} - 15$	-	$T_{cy(clk)} + 15$	ns

[1] $T_{cy(clk)} = 1 / f_{osc}$.

[2] Calculated values are for 6-clock mode only.

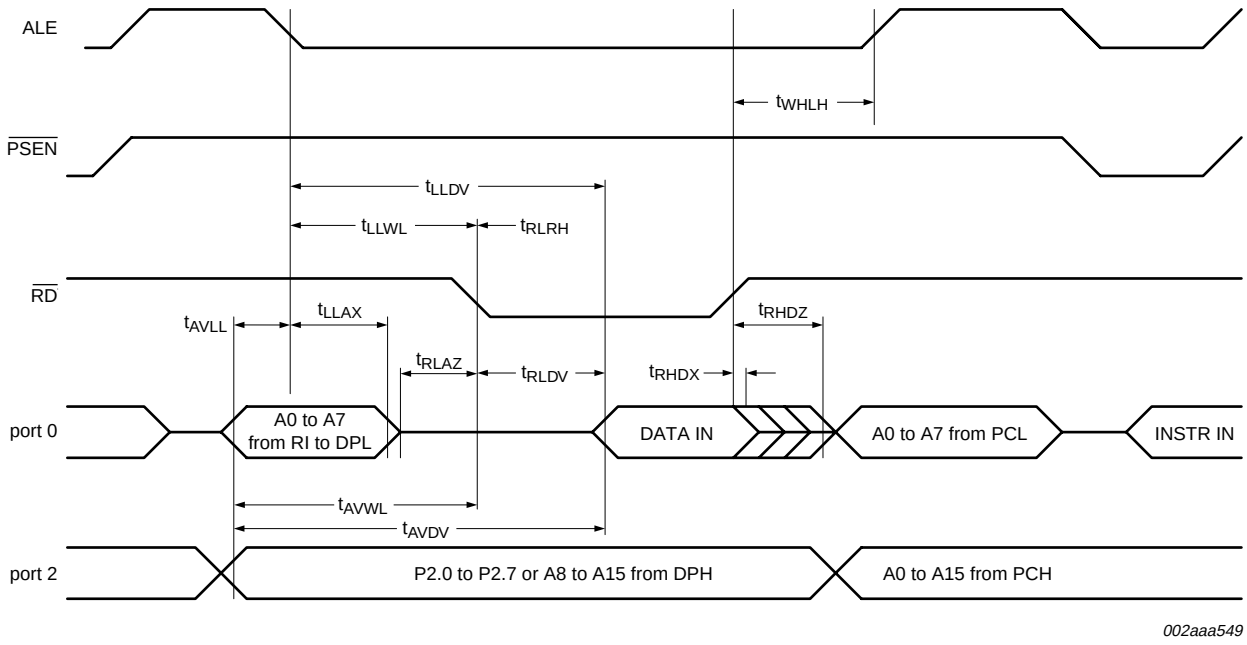

Fig 30. External data memory read cycle

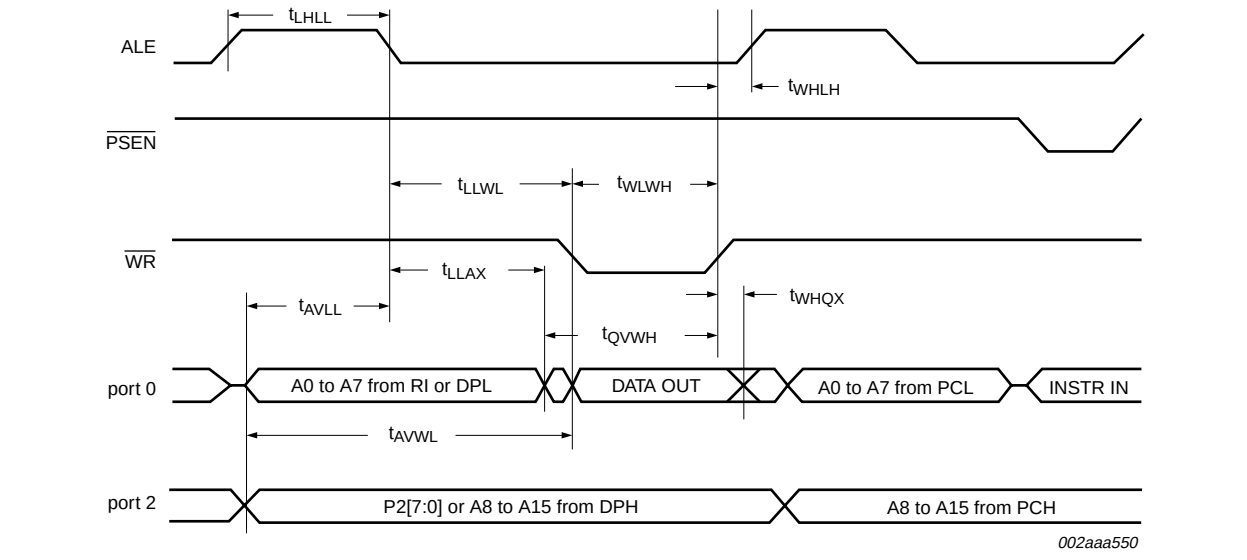

Fig 31. External data memory write cycle

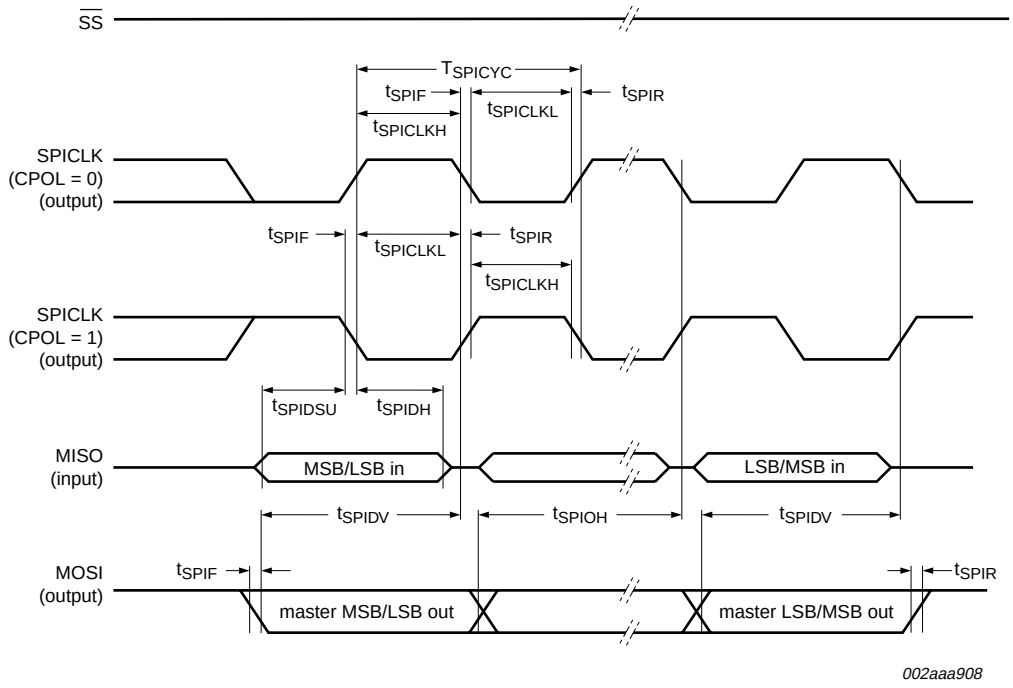

Fig 34. SPI master timing (CPHA = 0)

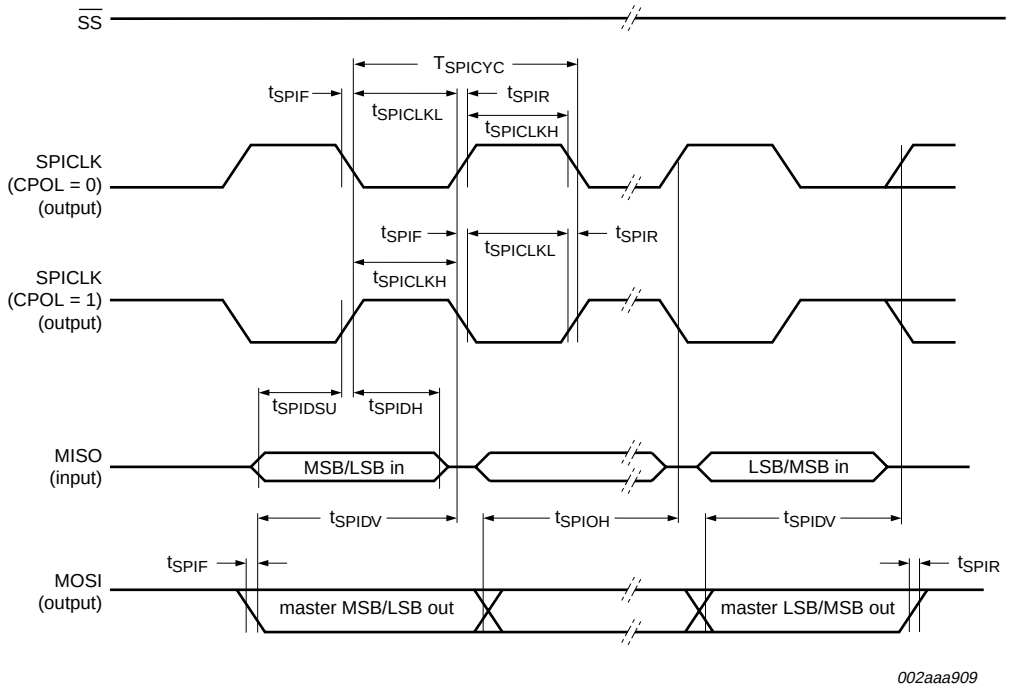

Fig 35. SPI master timing (CPHA = 1)

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13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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