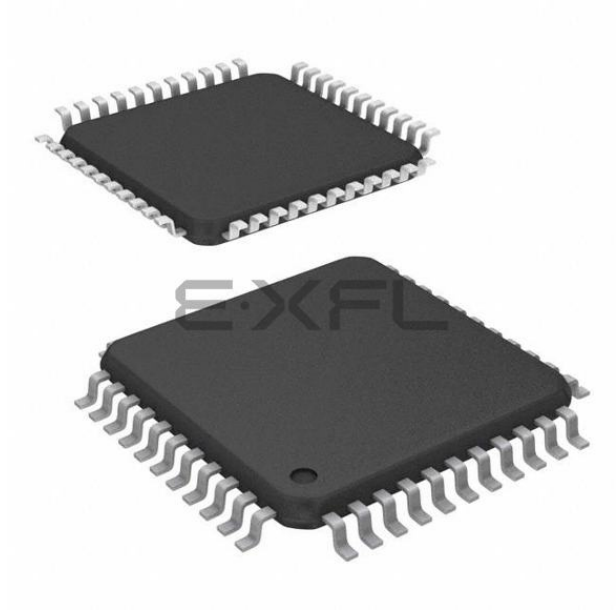

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89cv51rc2fbc-557

- Power-down mode with external interrupt wake-up
- Idle mode

2.3 Comparison to P89C51RB2/RC2/RD2 devices

- **SPI:** The P89CV51RB2/RC2/RD2 devices have an SPI interface that was not present on the P89C51RB2/RC2/RD2 devices.
- **Smaller block size:** The page size decreased from 4 kB to 128 B. These smaller pages can be erased and reprogrammed using IAP function calls, which makes practical use of code memory for non-volatile data storage. A page is erased in 30 ms or less. IAP and ISP code both support 128-B page operations. The IAP and ISP code uses multiple page-erase operations to emulate the erasing of larger block sizes (8 kB and 16 kB) to maintain firmware compatibility.
- **Status bit replaces Status byte:** Automatic entry into ISP mode following a reset is now controlled by one status bit. Its operation is almost identical to that used by the previous devices, which was based on the zero/non-zero value of the status byte.
- **Faster block erase:** The erase time for the entire user-code memory of the P89CV51RB2/RC2/RD2 devices is 150 ms, which is a significant improvement.
- **Larger RAM size:** RAM size increased from 512 B to 1 kB.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
P89CV51RB2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89CV51RB2FBC	TQFP44	plastic thin quad flat package; 44 leads; body 10 × 10 × 1.0 mm	SOT376-1
P89CV51RC2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89CV51RC2FBC	TQFP44	plastic thin quad flat package; 44 leads; body 10 × 10 × 1.0 mm	SOT376-1
P89CV51RD2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89CV51RD2FBC	TQFP44	plastic thin quad flat package; 44 leads; body 10 × 10 × 1.0 mm	SOT376-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Temperature range	Frequency
P89CV51RB2FA	16 kB	1 kB	–40 °C to +85 °C	0 MHz to 40 MHz
P89CV51RB2FBC				
P89CV51RC2FA	32 kB	1 kB		
P89CV51RC2FBC				
P89CV51RD2FA	64 kB	1 kB		
P89CV51RD2FBC				

4. Block diagram

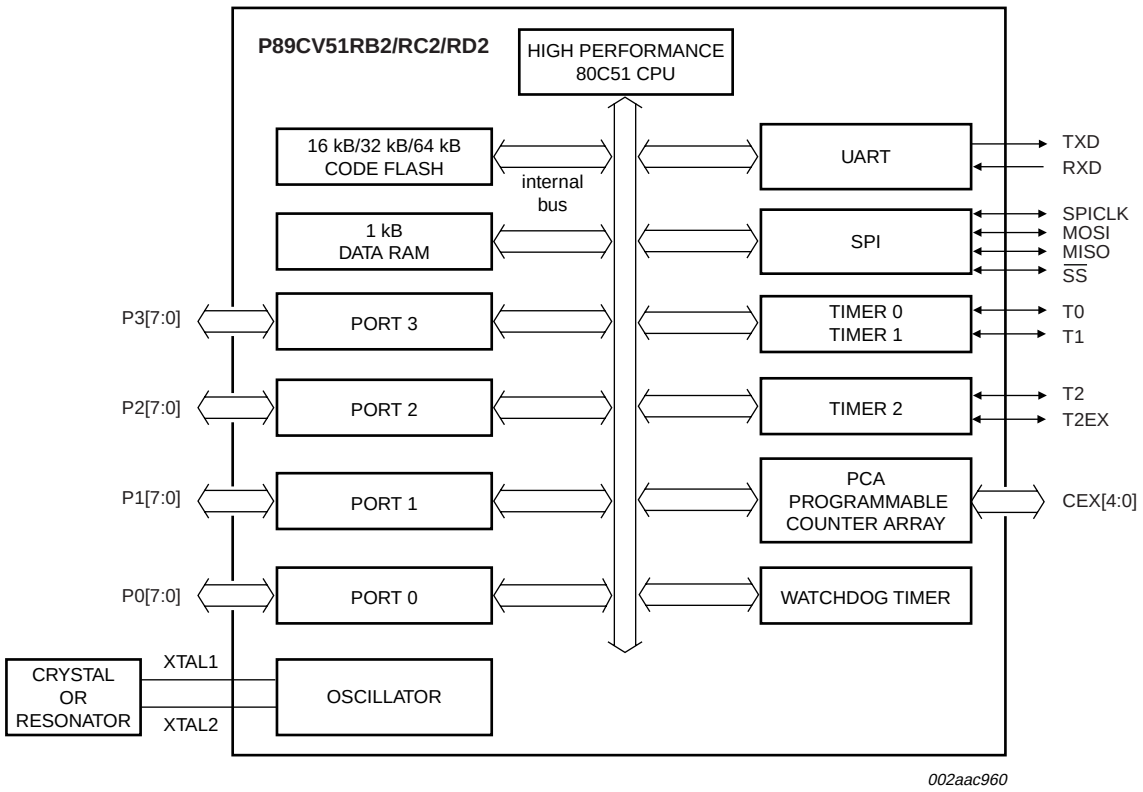

Fig 1. Block diagram

Table 3. P89CV51RB2/RC2/RD2 Pin description *...continued*

Symbol	Pin		Type	Description
	PLCC44	TQFP44		
P2[1]/A9	25	19	I/O	**P2[1] —** Port 2 bit 1.
			O	**A9 —** Address bit 9.
P2[2]/A10	26	20	I/O	**P2[2] —** Port 2 bit 2.
			O	**A10 —** Address bit 10.
P2[3]/A11	27	21	I/O	**P2[3] —** Port 2 bit 3.
			O	**A11 —** Address bit 11.
P2[4]/A12	28	22	I/O	**P2[4] —** Port 2 bit 4.
			O	**A12 —** Address bit 12.
P2[5]/A13	29	23	I/O	**P2[5] —** Port 2 bit 5.
			O	**A13 —** Address bit 13.
P2[6]/A14	30	24	I/O	**P2[6] —** Port 2 bit 6.
			O	**A14 —** Address bit 14.
P2[7]/A15	31	25	I/O	**P2[7] —** Port 2 bit 7.
			O	**A15 —** Address bit 15.
P3[0] to P3[7]			I/O with internal pull-up	**Port 3**: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins are pulled HIGH by the internal pull-ups when 1s are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups.
P3[0]/RXD	11	5	I/O	**P3[0] —** Port 3 bit 0.
			I	**RXD —** Serial input port.
P3[1]/TXD	13	7	I/O	**P3[1] —** Port 3 bit 1.
			O	**TXD —** Serial output port.
P3[2]/$\overline{\text{INT0}}$	14	8	I/O	**P3[2] —** Port 3 bit 2.
			I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
P3[3]/$\overline{\text{INT1}}$	15	9	I/O	**P3[3] —** Port 3 bit 3.
			I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P3[4]/T0	16	10	I/O	**P3[4] —** Port 3 bit 4.
			I	**T0 —** External count input to timer/counter 0.
P3[5]/T1	17	11	I/O	**P3[5] —** Port 3 bit 5.
			I	**T1 —** External count input to timer/counter 1.
P3[6]/$\overline{\text{WR}}$	18	12	I/O	**P3[6] —** Port 3 bit 6.
			O	**$\overline{\text{WR}}$ —** External data memory write strobe.
P3[7]/$\overline{\text{RD}}$	19	13	I/O	**P3[7] —** Port 3 bit 7.
			O	**$\overline{\text{RD}}$ —** External data memory read strobe.
$\overline{\text{PSEN}}$	32	26	O	**Program Store Enable**: $\overline{\text{PSEN}}$ is the read strobe for external program memory. When the device is executing from internal program memory, $\overline{\text{PSEN}}$ is inactive (HIGH). When the device is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR address	Bit functions and addresses[1]							
			MSB							LSB
DPTR	Data Pointer (2 B)									
DPH	Data Pointer High	83H	-	-	-	-	-	-	-	-
DPL	Data Pointer Low	82H	-	-	-	-	-	-	-	-
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**
IE*	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**
IP*	Interrupt Priority Low	B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0
IPH	Interrupt Priority High	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**
P1*	Port 1	90H	CEX4/ SPICLK	CEX3/ MISO	CEX2/ MOSI	CEX1/$\overline{SS}$	CEX0	ECI	T2EX	T2
		Bit address	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
P2*	Port 2	A0H	A15	A14	A13	A12	A11	A10	A9	A8
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TXD	RXD
PCON	Power Control	87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P
RCAP2H	Timer 2 Capture High	CBH	-	-	-	-	-	-	-	-
RCAP2L	Timer 2 Capture Low	CAH	-	-	-	-	-	-	-	-
		Bit address	**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**
SCON*	Serial port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	Serial port data Buffer	99H	-	-	-	-	-	-	-	-
SADDR	Serial port Address	A9H	-	-	-	-	-	-	-	-
SADEN	Serial port Address Enable	B9H	-	-	-	-	-	-	-	-

6.2 Memory organization

The various P89CV51RB2/RC2/RD2 memory spaces are as follows:

- DATA

  128 B of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the stack may be in this area.

- IDATA

  Indirect Data. 256 B of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the stack may be in this area. This area includes the DATA area and the 128 B immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  'External' Data or auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the DPTR, R0, or R1. The P89CV51RB2/RC2/RD2 have 768 B of on-chip XDATA memory.

- CODE

  64 kB of code memory space, accessed as part of program execution and via the MOVC instruction. The P89CV51RB2/RC2/RD2 have 16/32/64 kB of on-chip code memory.

6.2.1 Expanded data RAM addressing

The P89CV51RB2/RC2/RD2 have 1 kB of data RAM; see Figure 4.

To access the expanded RAM (XRAM), the EXTRAM bit must be set and MOVX instructions must be used. The expanded memory is physically located on the chip and logically occupies the first bytes of external memory (addresses 000H to 2FFH).

Table 5. AUXR - Auxiliary function register (address 8EH) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	EXTRAM	AO

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3[6] ($\overline{WR}$), P3[7] ($\overline{RD}$), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM access (indirect addressing only):

```
MOVX @DPTR, A; DPTR contains 0A0H
```

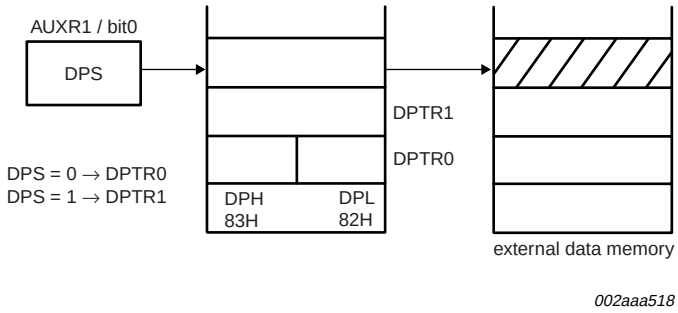

Fig 5. Dual data pointer organization

Table 8. AUXR1 - Auxiliary function register 1 (address A2H) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	ENBOOT	-	GF2	0	-	DPS

Table 9. AUXR1 - Auxiliary function register 1 (address A2H) bit description

Bit	Symbol	Description
7, 6, 4	-	Reserved for future use. Should be set to 0 by user programs.
5	ENBOOT	Enable BOOTROM
3	GF2	General purpose user-defined Flag.
2	0	This bit contains a hard-wired 0. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should be set to 0 by user programs.
0	DPS	Data Pointer Select. Chooses one of two data pointers for use by the program. See text for details.

6.2.3 Reset

At initial power-up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins HIGH. Powering up the device without a valid reset could cause the MCU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash. A system reset will not affect the on-chip RAM while the device is running, however, the contents of the on-chip RAM during power-up are indeterminate.

When power is applied to the device, the RST pin must be held HIGH long enough for the oscillator to start-up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement an RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2 kΩ resistor as shown in Figure 6.

During initial power-up the POF flag in the PCON register is set to indicate an initial power-up condition. The POF flag will remain active until cleared by software.

Table 11. ISP Hex record formats *…continued*

Record type	Command/data function
04	Display device data or blank check :05xxxx04sssseeeeffcc Where 05 = number of bytes in the record xxxx = required field but value is a don't care 04 = function code for display or blank check ssss = starting address, MSB first eeee = ending address, MSB first ff = subfunction 00 = display data 01 = blank check cc = checksum Subfunction codes: Example: :0500000400001FFF00D9 (display from 0000H to 1FFFH)
05	Miscellaneous read functions :02xxxx05ffsscc Where: 02 = number of bytes in the record xxxx = required field but value is a don't care 05 = function code for miscellaneous read ffss = subfunction and selection code 0000 = read manufacturer ID 0001 = read device ID 1 0002 = read device ID 2 0003 = read 6×/12× bit (bit 7 = 1 is 6×, bit 7 = 0 is 12×) 0080 = read boot code version 0700 = read security bits 0701 = read status bit 0702 = read boot vector cc = checksum Example: :020000050000F9 (display manufacturer ID)
06	Direct load of baud rate :02xxxx06HHLLcc Where: 02 = number of bytes in the record xxxx = required field but value is a don't care HH = high byte of timer T2 LL = low byte of timer T2 cc = checksum Example: :02000006FFFFcc (load T2 = FFFF)

The ‘Timer’ or ‘Counter’ function is selected by control bits C/$\overline{T}$ in the special function register TMOD. These two timers/counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both timers/counters. Mode 3 is different. The four operating modes are described in the following text.

Table 13. TMOD - Timer/Counter mode control register (address 89H) bit allocation

Not bit addressable; reset value: 0000 0000B; reset source(s): any source.

Bit	7	6	5	4	3	2	1	0
Symbol	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

Table 14. TMOD - Timer/Counter mode control register (address 89H) bit description

Bit	Symbol	Description
7	T1GATE	Gating control for Timer 1. When set, timer/counter is enabled only while the $\overline{INT1}$ pin is HIGH and the TR1 control bit is set. When cleared, Timer 1 is enabled when the TR1 control bit is set.
6	T1C/$\overline{T}$	Timer or counter select for Timer 1. Cleared for timer operation. Set for counter operation (input from T1 input pin).
5	T1M1	Mode select for Timer 1.
4	T1M0	
3	T0GATE	Gating control for Timer 0. When set, timer/counter is enabled only while the $\overline{INT0}$ pin is HIGH and the TR0 control bit is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
2	T0C/$\overline{T}$	Timer or counter select for Timer 0. Cleared for timer operation. Set for counter operation (input from T0 input pin).
1	T0M1	Mode select for Timer 0.
0	T0M0	

Table 15. TMOD - Timer/Counter mode control register (address 89H) M1/M0 operating mode

M1	M0	Operating mode	
0	0	0	8048 timer ‘TLx’ serves as 5-bit prescaler.
0	1	1	16-bit timer/counter ‘THx’ and ‘TLx' are cascaded; there is no prescaler.
1	0	2	8-bit auto-reload timer/counter ‘THx’ holds a value which is to be reloaded into ‘TLx’ each time it overflows.
1	1	3	(Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	3	(Timer 1) timer/counter 1 stopped.

Table 16. TCON - Timer/Counter control register (address 88H) bit allocation

Bit addressable; reset value: 0000 0000B; reset source(s): any reset.

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 17. TCON - Timer/Counter control register (address 88H) bit description

Bit	Symbol	Description
7	TF1	Timer 1 overflow Flag. Set by hardware on timer/counter overflow. Cleared by hardware when the processor vectors to Timer 1 interrupt routine, or by software.
6	TR1	Timer 1 Run control bit. Set/cleared by software to turn timer/counter 1 on/off.
5	TF0	Timer 0 overflow Flag. Set by hardware on timer/counter overflow. Cleared by hardware when the processor vectors to Timer 0 interrupt routine, or by software.
4	TR0	Timer 0 Run control bit. Set/cleared by software to turn timer/counter 0 on/off.
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge/LOW-state is detected. Cleared by hardware when the interrupt is processed, or by software.
2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/LOW-state that triggers external interrupt 1.
1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge/LOW-state is detected. Cleared by hardware when the interrupt is processed, or by software.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/LOW-state that triggers external interrupt 0.

6.4.1 Mode 0

Putting either timer into Mode 0 makes it look like an 8048 timer, which is an 8-bit counter with a fixed divide-by-32 prescaler. Figure 7 shows Mode 0 operation.

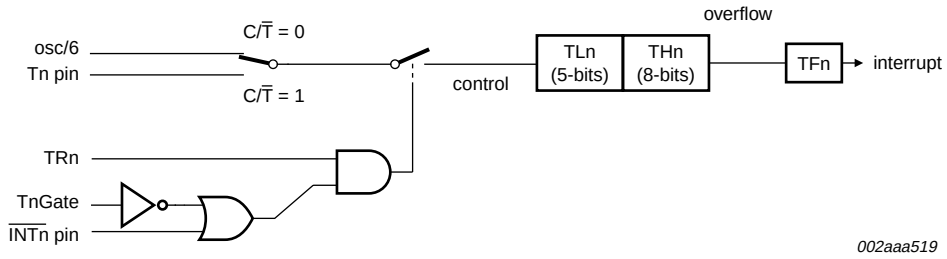

Fig 7. Timer/counter 0 or 1 in Mode 0 (13-bit counter)

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TFn. The count input is enabled to the timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the special function register TCON (Table 17). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 and Timer 1; see Figure 7. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

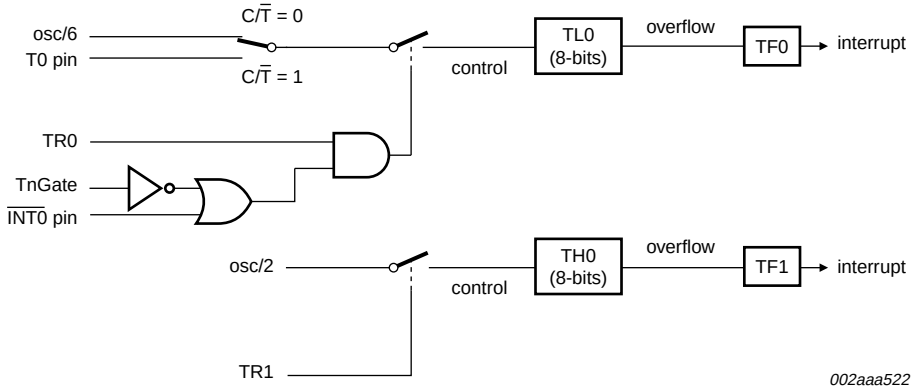

Fig 10. Timer/counter 0 Mode 3 (two 8-bit counters)

6.5 Timer 2

Timer 2 is a 16-bit timer/counter which can operate as either an event timer or an event counter, as selected by C/$\overline{T}$2 in the special function register T2CON. Timer 2 has four operating modes: Capture, Auto-reload (up or down counting), Clock-out, and Baud rate generator which are selected according to Table 18 using T2CON (Table 19 and Table 20) and T2MOD (Table 21 and Table 22).

Table 18. Timer 2 operating mode

RCLK + TCLK	CP/$\overline{RL}$2	TR2	T2OE	Mode
0	0	1	0	16-bit auto reload
0	1	1	0	16-bit capture
0	0	1	1	Programmable clock-out
1	X	1	0	Baud rate generator
X	X	0	X	off

Table 19. T2CON - Timer/Counter 2 control register (address C8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/$\overline{RL}$2

Table 20. T2CON - Timer/Counter 2 control register (address C8H) bit description

Bit	Symbol	Description
7	TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1 or when Timer 2 is in Clock-out mode.
6	EXF2	Timer 2 external flag is set when Timer 2 is in capture, reload or baud rate mode, EXEN2 = 1 and a negative transition on T2EX occurs. If Timer 2 interrupt is enabled EXF2 = 1 causes the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
5	RCLK	Receive clock flag. When set, causes the UART to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.

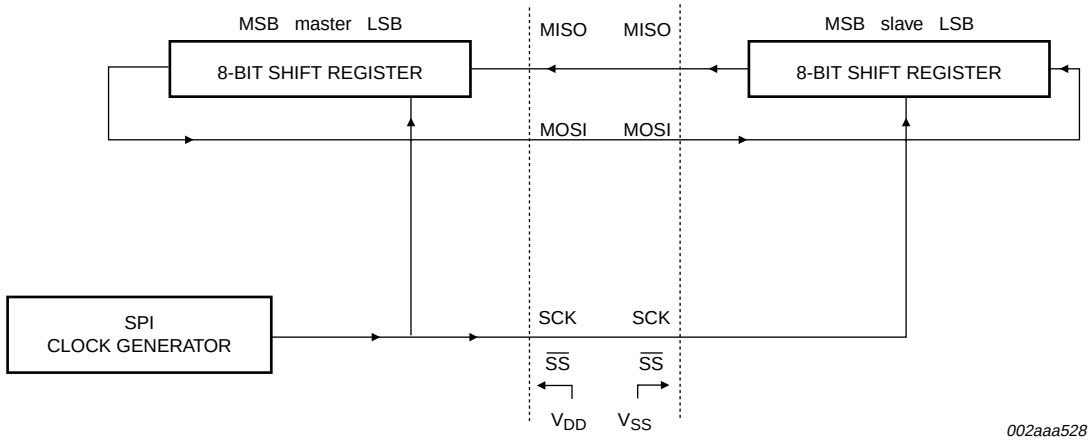

Fig 16. SPI master-slave interconnection

Table 27. SPCR - SPI control register (address D5H) bit allocation

Reset source(s): any reset; reset value: 0000 0000B.

Bit	7	6	5	4	3	2	1	0
Symbol	SPIE	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Table 28. SPCR - SPI control register (address D5H) bit description

Bit	Symbol	Description
7	SPIE	SPI interrupt enable. If both SPIE = 1 and ES = 1, SPI interrupts are enabled.
6	SPEN	SPI enable bit. When set enables SPI.
5	DORD	Data transmission order. 0 = MSB first; 1 = LSB first in data transmission.
4	MSTR	Master/Slave select. 1 = Master mode, 0 = Slave mode.
3	CPOL	Clock polarity. 1 = SPICLK is HIGH when idle (active LOW), 0 = SPICLK is LOW when idle (active HIGH).
2	CPHA	Clock Phase control bit. 1 = shift-triggered on the trailing edge of the clock; 0 = shift-triggered on the leading edge of the clock.
1	SPR1	SPI clock Rate select bit 1. Along with SPR0 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave; see Table 29.
0	SPR0	SPI clock Rate select bit 0. Along with SPR1 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave; see Table 29.

Table 29. SPCR - SPI control register (address D5H) clock rate selection

SPR1	SPR0	SPICLK = f_{osc} divided by	
		6-clock mode	12-clock mode
0	0	2	4
0	1	8	16
1	0	32	64
1	1	64	128

way to disable the WDT, except through a reset (either a hardware reset or a WDT overflow reset). When the WDT overflows, it will drive an output reset HIGH pulse at the RST pin.

When the WDT is enabled (and thus running) the user needs to reset it by writing 01EH and 0E1H, in sequence, to the WDTRST SFR to avoid WDT overflow. The 14-bit counter reaches overflow when it reaches 16383 (3FFFH) and this will reset the device.

The WDT's counter cannot be read or written. When the WDT overflows it will generate an output pulse at the RST pin with a duration of 98 oscillator periods in 6-clock mode or 196 oscillator periods in 12-clock mode.

6.9 PCA

The PCA includes a special 16-bit timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse-width modulator. Each module has a pin associated with it: Module 0 is connected to CEX0, module 1 to CEX1, etc. Registers CH and CL contain the current value of the free-running up-counting 16-bit PCA timer. The PCA timer is a common time base for all five modules and can be programmed to run at: $\frac{1}{6}$ the oscillator frequency, $\frac{1}{2}$ the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1[2]). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR; see Table 32 and Table 33.

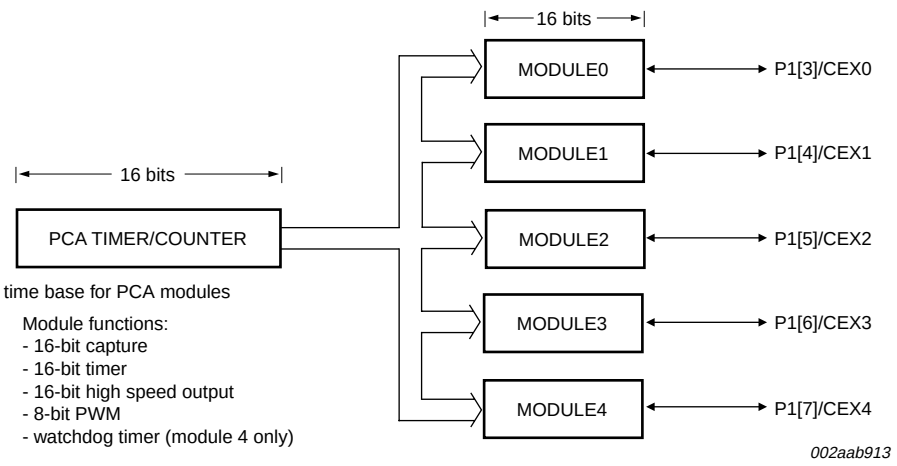

Fig 19. PCA

In the CMOD SFR there are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during Idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The watchdog timer function is implemented in module 4 of PCA.

The CCON SFR contains the run control bit for the PCA (CR) and the flags for the PCA timer (CF) and each module (CCF[4:0]). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD

Table 34. CMOD - PCA counter mode register (address D9H) count pulse select *...continued*

CPS1	CPS0	Select PCA input
0	1	1 internal clock, f_{osc} / 6
1	0	2 Timer 0 overflow
1	1	3 external clock at pin P1[2]/ECI (maximum rate = f_{osc} / 4)

Table 35. CCON - PCA counter control register (address D8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0

Table 36. CCON - PCA counter control register (address D8H) bit description

Bit	Symbol	Description
7	CF	PCA Counter overflow Flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
6	CR	PCA Counter Run control. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
5	-	Reserved for future use. Should be set to 0 by user programs.
4	CCF4	PCA Module 4 interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
3	CCF3	PCA Module 3 interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
2	CCF2	PCA Module 2 interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
1	CCF1	PCA Module 1 interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
0	CCF0	PCA Module 0 interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.

Table 37. CCAPMn - PCA modules compare/capture register (address CCAPM0 DAH, CCAPM1 DBH, CCAPM2 DCH, CCAPM3 DDH, CCAPM4 DEH) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn

Table 38. CCAPMn - PCA modules compare/capture register (address CCAPM0 DAH, CCAPM1 DBH, CCAPM2 DCH, CCAPM3 DDH, CCAPM4 DEH) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to 0 by user programs.
6	ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
5	CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
4	CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
3	MATn	Match. When MATn = 1 a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.

module's CCAPnL SFR, the output will be LOW; when it is equal to, or greater, the output will be HIGH. When CL overflows from FFH to 00H, CCAPnL is reloaded with the value in CCAPnH. This allows the PWM to be updated without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable PWM mode.

6.9.5 PCA watchdog timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 24 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven HIGH.

User's software then must periodically change (CCAP4H, CCAP4L) to keep a match from occurring with the PCA timer (CH, CL). This code is given in the subroutine WATCHDOG shown below.

In order to hold off the reset, the user has three options:

- Periodically change the compare value so it will never match the PCA timer.
- Periodically change the PCA timer value so it will never match the compare values.
- Disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in the third option. If the program counter ever reaches an undesired value, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember that the PCA timer is the time base for **all** modules; changing the time base for other modules is not recommended. Thus, in most applications the first option is best.

```
;CALL the following WATCHDOG subroutine periodically.
   CLR    EA           ;Hold off interrupts
   MOV    CCAP4L,#00   ;Next compare value is within 255 counts of
                        current PCA timer value
   MOV    CCAP4H,CH
   SETB   EA           ;Re-enable interrupts
   RET
```

Do not use this routine as part of an interrupt service routine, because if the program counter would enter an infinite loop, still interrupts will be serviced and the watchdog will continually keep getting reset. Because this would defeat the purpose of the watchdog, it is recommended that this subroutine is called from the main program within 2^{16} PCA timer counts.

Table 43. IE - Interrupt enable register 0 (address A8H) bit description *...continued*

Bit	Symbol	Description
4	ES	Serial port interrupt Enable.
3	ET1	Timer 1 overflow interrupt Enable.
2	EX1	External interrupt 1 Enable.
1	ET0	Timer 0 overflow interrupt Enable.
0	EX0	External interrupt 0 Enable.

Table 44. IP - Interrupt priority low register (address B8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Table 45. IP - Interrupt priority low register (address B8H) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to 0 by user programs.
6	PPC	PCA interrupt Priority Low.
5	PT2	Timer 2 interrupt Priority Low.
4	PS	Serial Port interrupt Priority Low.
3	PT1	Timer 1 interrupt Priority Low.
2	PX1	External interrupt 1 Priority Low.
1	PT0	Timer 0 interrupt Priority Low.
0	PX0	External interrupt 0 Priority Low.

Table 46. IPH - Interrupt priority high register (address B7H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Table 47. IPH - Interrupt priority high register (address B7H) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to 0 by user programs.
6	PPCH	PCA interrupt Priority High.
5	PT2H	Timer 2 interrupt Priority High.
4	PSH	Serial Port interrupt Priority High.
3	PT1H	Timer 1 interrupt Priority High.
2	PX1H	External interrupt 1 Priority High.
1	PT0H	Timer 0 interrupt Priority High.
0	PX0H	External interrupt 0 Priority High.

6.13.1.1 Clock control register (CKCON)

By default, the device runs at twelve clock cycles per machine cycle (12-clock mode). The device may be run at 6 clock cycles per machine cycle (6-clock mode) by programming of either a non-volatile bit (FX2) or an SFR bit (X2); see Table 52 “Clock modes”. If the FX2 non-volatile bit is programmed, the device will run in 6-clock mode and the X2 SFR bit has no effect. If the FX2 bit is erased, then the clock mode is controlled by the X2 SFR bit.

Table 50. CKCON - Clock control register (address 8FH) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	SPIX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

Table 51. CKCON - Clock control register (address 8FH) bit description

Bit	Symbol	Description
7	SPIX2	SPI clock; 0 = 6 clock cycles for each SPI clock cycle; 1 = 12 clock cycles
6	WDX2	Watchdog clock; 0 = 6 clock cycles for each WDT clock cycle; 1 = 12 clock cycles
5	PCAX2	PCA clock; 0 = 6 clock cycles for each PCA clock cycle; 1 = 12 clock cycles
4	SIX2	UART clock; 0 = 6 clock cycles for each UART clock cycle; 1 = 12 clock cycles
3	T2X2	Timer 2 clock; 0 = 6 clock cycles for each Timer 2 clock cycle; 1 = 12 clock cycles
2	T1X2	Timer 1 clock; 0 = 6 clock cycles for each Timer 1 clock cycle; 1 = 12 clock cycles
1	T0X2	Timer 0 clock; 0 = 6 clock cycles for each Timer 0 clock cycle; 1 = 12 clock cycles
0	X2	CPU clock; 0 = 12 clock cycles for each machine cycle; 1 = 6 clock cycles

Table 52. Clock modes

FX2 clock mode bit	X2 bit	CPU clock mode	Peripheral clock mode bit (e.g. T0X2)	Mode
erased	0	12-clock (default)	X	12-clock (default)
	1	6-clock	0	6-clock
			1	12-clock
programmed	X	6-clock	0	6-clock
			1	12-clock

7. Limiting values

Table 53. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Parameters are valid over operating temperature range unless otherwise specified; all voltages are with respect to V_{SS} unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
V_I	input voltage	on $\overline{EA}$ pin to V_{SS}	–0.5	+14	V
V_n	voltage on any other pin	except V_{SS}; with respect to V_{DD}	–0.5	V_{DD} + 0.5	V
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	15	mA
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

8. Static characteristics

Table 54. Static characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$n_{endu(fl)}$	endurance of flash memory	JEDEC Standard A117	[1]	10000	-	-	cycles
$t_{ret(fl)}$	flash memory retention time	JEDEC Standard A103	[1]	100	-	-	years
I_{latch}	I/O latch-up current	JEDEC Standard 78	[1]	100 + I_{DD}	-	-	mA
$V_{th(HL)}$	HIGH-LOW threshold voltage			–0.5	-	+0.2V_{DD} – 0.1	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except XTAL1, RST		0.2V_{DD} + 0.9	-	V_{DD} + 0.5	V
V_{OL}	LOW-level output voltage	V_{DD} = 4.5 V; except $\overline{PSEN}$, ALE	[2][3][4]				
		I_{OL} = 1.6 mA		-	-	0.4	V
		V_{DD} = 4.5 V; ALE, $\overline{PSEN}$					
		I_{OL} = 3.2 mA		-	-	0.45	V
V_{OH}	HIGH-level output voltage	V_{DD} = 4.5 V; ports 1, 2, 3, 4	[5]				
		I_{OH} = –30 µA		V_{DD} – 0.7	-	-	V
		V_{DD} = 4.5 V; port 0 in External bus mode, ALE, $\overline{PSEN}$					
		I_{OH} = –3.2 mA		V_{DD} – 0.7	-	-	V
I_{IL}	LOW-level input current	V_I = 0.4 V; ports 1, 2, 3, 4		–1	-	–75	µA
I_{THL}	HIGH-LOW transition current	V_I = 2 V; ports 1, 2, 3, 4	[6]	-	-	–650	µA
I_{LI}	input leakage current	0.45 V < V_I < V_{DD} – 0.3 V; port 0		-	-	±10	µA
		0 V < V_I < 6 V		-	-	10	µA

Table 56. External clock drive

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
f_{osc}	oscillator frequency	-	-	0	40	MHz
$T_{cy(clk)}$	clock cycle time	25	-	-	-	ns
t_{CHCX}	clock HIGH time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCX}	clock LOW time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCH}	clock rise time	-	10	-	-	ns
t_{CHCL}	clock fall time	-	10	-	-	ns

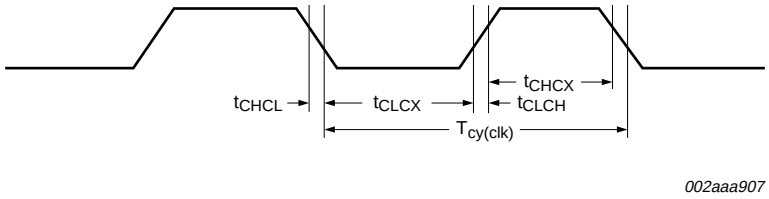

Fig 32. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

Table 57. Serial port timing

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	serial port clock cycle time	0.3	-	$12T_{cy(clk)}$	-	µs
t_{QVXH}	output data set-up to clock rising edge time	117	-	$10T_{cy(clk)} - 133$	-	ns
t_{XHQX}	output data hold after clock rising edge time	0	-	$2T_{cy(clk)} - 50$	-	ns
t_{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t_{XHDV}	input data valid to clock rising edge time	-	117	-	$10T_{cy(clk)} - 133$	ns

11. Abbreviations

Table 59. Abbreviations

Acronym	Description
ALE	Address Latch Enable
CPU	Central Processing Unit
DPTR	Data PoinTeR
DUT	Device Under Test
EPROM	Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
ID	IDentifier
IAP	In-Application Programming
ISP	In-System Programming
LSB	Least Significant Bit
MCU	MicroController Unit
MSB	Most Significant Bit
PCA	Programmable Counter Array
PCH	Programmable Counter High
PCL	Programmable Counter Low
PWM	Pulse-Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
SFR	Special Function Register
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter
WDT	WatchDog Timer

13. Legal information

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Document status[1][2]	Product status[3]	Definition
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