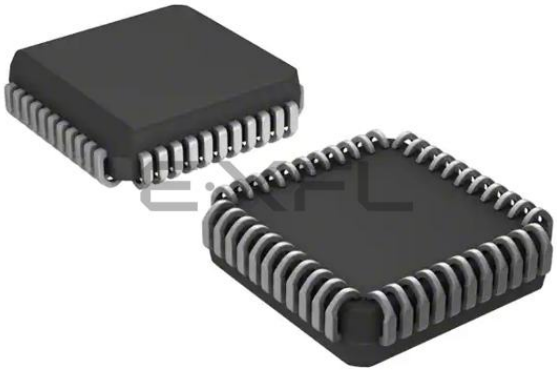

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89cv51rd2fa-512

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR address	Bit functions and addresses[1]							
			MSB							LSB
DPTR	Data Pointer (2 B)									
DPH	Data Pointer High	83H	-	-	-	-	-	-	-	-
DPL	Data Pointer Low	82H	-	-	-	-	-	-	-	-
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**
IE*	Interrupt Enable	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**
IP*	Interrupt Priority Low	B8H	-	PPC	PT2	PS	PT1	PX1	PT0	PX0
IPH	Interrupt Priority High	B7H	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**
P1*	Port 1	90H	CEX4/ SPICLK	CEX3/ MISO	CEX2/ MOSI	CEX1/$\overline{SS}$	CEX0	ECI	T2EX	T2
		Bit address	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
P2*	Port 2	A0H	A15	A14	A13	A12	A11	A10	A9	A8
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TXD	RXD
PCON	Power Control	87H	SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P
RCAP2H	Timer 2 Capture High	CBH	-	-	-	-	-	-	-	-
RCAP2L	Timer 2 Capture Low	CAH	-	-	-	-	-	-	-	-
		Bit address	**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**
SCON*	Serial port Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	Serial port data Buffer	99H	-	-	-	-	-	-	-	-
SADDR	Serial port Address	A9H	-	-	-	-	-	-	-	-
SADEN	Serial port Address Enable	B9H	-	-	-	-	-	-	-	-

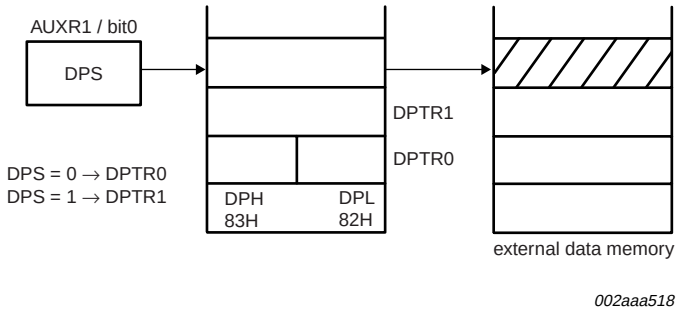


Fig 5. Dual data pointer organization

Table 8. AUXR1 - Auxiliary function register 1 (address A2H) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	ENBOOT	-	GF2	0	-	DPS

Table 9. AUXR1 - Auxiliary function register 1 (address A2H) bit description

Bit	Symbol	Description
7, 6, 4	-	Reserved for future use. Should be set to 0 by user programs.
5	ENBOOT	Enable BOOTROM
3	GF2	General purpose user-defined Flag.
2	0	This bit contains a hard-wired 0. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should be set to 0 by user programs.
0	DPS	Data Pointer Select. Chooses one of two data pointers for use by the program. See text for details.

6.2.3 Reset

At initial power-up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins HIGH. Powering up the device without a valid reset could cause the MCU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash. A system reset will not affect the on-chip RAM while the device is running, however, the contents of the on-chip RAM during power-up are indeterminate.

When power is applied to the device, the RST pin must be held HIGH long enough for the oscillator to start-up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement an RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2 kΩ resistor as shown in Figure 6.

During initial power-up the POF flag in the PCON register is set to indicate an initial power-up condition. The POF flag will remain active until cleared by software.

Following a reset condition, under normal conditions, the MCU will start executing code from address 0000H in the user's code memory. However if either the $\overline{PSEN}$ pin was LOW when reset was exited, or the status bit = 1, the MCU will start executing code from the boot address. The boot address is formed using the value of the boot vector as the high byte of the address and 00H as the low byte.

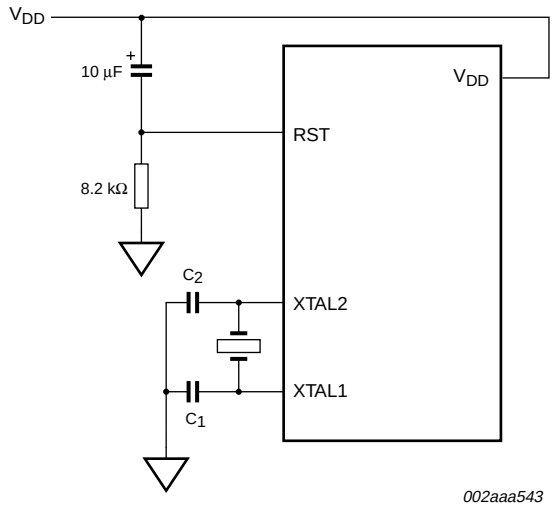


Fig 6. Power-on reset circuit

6.3 Flash memory

6.3.1 Flash organization

The P89CV51RB2/RC2/RD2 program memory consists of a 16/32/64 kB block for user code. The flash can be read or written in bytes and can be erased in 128-B pages. A chip erase function will erase the entire user code memory and its associated security bits. There are three methods for erasing or programming the flash memory that may be used. First, the flash may be programmed or erased in the end-user application by calling LOW-state routines through a common IAP entry point. Second, the on-chip ISP bootloader may be invoked. This ISP bootloader will, in turn, call LOW-state routines through the same common entry point that can be used by the end-user application. Third, the flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer which supports this device.

6.3.2 Features

- Flash internal program memory with 128-B page erase.
- Internal boot block, containing LOW-state IAP routines available to user code.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Default loader providing ISP via the serial port, located in upper-end of program memory.
- Programming and erase over the full operating voltage range.
- Read/Programming/Erase using ISP/IAP.

Table 11. ISP Hex record formats *…continued*

Record type	Command/data function
03	Miscellaneous write functions :nnxxxx03ffssddcc Where: nn = number of bytes in the record xxxx = required field but value is a don't care ff = subfunction code ss = selection code dd = data (if needed) cc = checksum Subfunction code = 0C (erase 4 kB blocks) ff = 0C ss = block code, as shown below: block 0, 0 kB to 4 kB, 00H block 1, 4 kB to 8 kB, 10H block 2, 8 kB to 12 kB, 20H block 3, 12 kB to 16 kB, 30H block 4, 16 kB to 20 kB, 40H (only available on P89CV51RC2/RD2) block 5, 20 kB to 24 kB, 50H (only available on P89CV51RC2/RD2) block 6, 24 kB to 28 kB, 60H (only available on P89CV51RC2/RD2) block 7, 28 kB to 32 kB, 70H (only available on P89CV51RC2/RD2) block 8, 32 kB to 36 kB, 80H (only available on P89CV51RD2) block 9, 36 kB to 40 kB, 90H (only available on P89CV51RD2) block 10, 40 kB to 44 kB, A0H (only available on P89CV51RD2) block 11, 44 kB to 48 kB, B0H (only available on P89CV51RD2) block 12, 48 kB to 52 kB, C0H (only available on P89CV51RD2) block 13, 52 kB to 56 kB, D0H (only available on P89CV51RD2) block 14, 56 kB to 60 kB, E0H (only available on P89CV51RD2) block 15, 60 kB to 64 kB, F0H (only available on P89CV51RD2) Example: :020000030C20CF (erase 4 kB block #2)

6.3.8 IAP method

Several IAP calls are available for use by an application program to permit selective erasing, reading and programming of flash pages, security bits, status bit, and device ID. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FFF0H. The IAP calls are shown in Table 12.

Table 12. IAP function calls

IAP function	IAP call parameters
Read ID	**Input parameters:** R1 = 00H or 80H (WDT feed) DPH = 00H DPL = 00H = manufacturer ID DPL = 01H = device ID 1 DPL = 02H = device ID 2 DPL = 03H = 6×/12× bit (if bit 7 = 1: 6×) DPL = 80H = ISP version number **Return parameter(s):** ACC = requested parameter
Erase 4 kB code block (new function)	**Input parameters:** R0 = oscillator frequency (integer) R1 = 0CH or 8CH (WDT feed) DPH = address of 4 kB code block DPH = 00H, 4 kB block 0, 0 kB to 4 kB DPH = 10H, 4 kB block 1, 4 kB to 8 kB DPH = 20H, 4 kB block 2, 8 kB to 12 kB DPH = 30H, 4 kB block 3, 12 kB to 16 kB DPH = 40H, 4 kB block 4, 16 kB to 20 kB DPH = 50H, 4 kB block 5, 20 kB to 24 kB DPH = 60H, 4 kB block 6, 24 kB to 28 kB DPH = 70H, 4 kB block 7, 28 kB to 32 kB DPH = 80H, 4 kB block 8, 32 kB to 36 kB DPH = 90H, 4 kB block 9, 36 kB to 40 kB DPH = A0H, 4 kB block 10, 40 kB to 44 kB DPH = B0H, 4 kB block 11, 44 kB to 48 kB DPH = C0H, 4 kB block 12, 48 kB to 52 kB DPH = D0H, 4 kB block 13, 52 kB to 56 kB DPH = E0H, 4 kB block 14, 56 kB to 60 kB DPH = F0H, 4 kB block 15, 60 kB to 64 kB DPL = 00H **Return parameter(s):** ACC = 00: pass ACC is not 00: fail

Table 17. TCON - Timer/Counter control register (address 88H) bit description

Bit	Symbol	Description
7	TF1	Timer 1 overflow Flag. Set by hardware on timer/counter overflow. Cleared by hardware when the processor vectors to Timer 1 interrupt routine, or by software.
6	TR1	Timer 1 Run control bit. Set/cleared by software to turn timer/counter 1 on/off.
5	TF0	Timer 0 overflow Flag. Set by hardware on timer/counter overflow. Cleared by hardware when the processor vectors to Timer 0 interrupt routine, or by software.
4	TR0	Timer 0 Run control bit. Set/cleared by software to turn timer/counter 0 on/off.
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge/LOW-state is detected. Cleared by hardware when the interrupt is processed, or by software.
2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/LOW-state that triggers external interrupt 1.
1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge/LOW-state is detected. Cleared by hardware when the interrupt is processed, or by software.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/LOW-state that triggers external interrupt 0.

6.4.1 Mode 0

Putting either timer into Mode 0 makes it look like an 8048 timer, which is an 8-bit counter with a fixed divide-by-32 prescaler. Figure 7 shows Mode 0 operation.

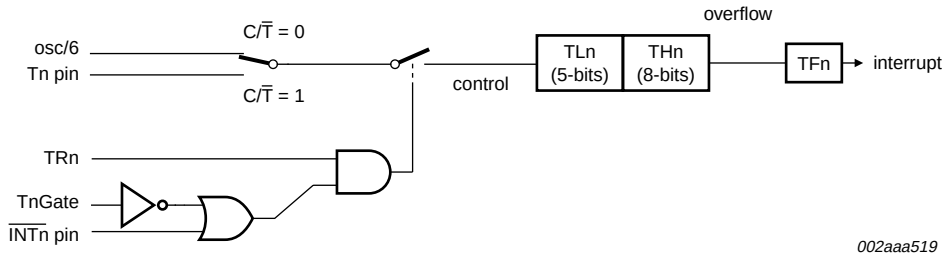


Fig 7. Timer/counter 0 or 1 in Mode 0 (13-bit counter)

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TFn. The count input is enabled to the timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the special function register TCON (Table 17). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 and Timer 1; see Figure 7. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit, although it is preferable to use the Framing Error flag (FE). When the UART receives data in Mode 1 and SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

6.6.9 Automatic address recognition

Automatic address recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled for the UART by setting the SM2 bit in SCON. In the 9-bit UART modes, Mode 2 and Mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the 'given' address or the 'broadcast' address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data.

Using the automatic address recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the broadcast address. Two special function registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are don't care. The SADEN mask can be logically ANDed with the SADDR to create the given address which the master will use for addressing each of the slaves. Use of the given address allows multiple slaves to be recognized while excluding others.

This device uses the methods presented in Figure 15 to determine if a given or broadcast address has been received or not.

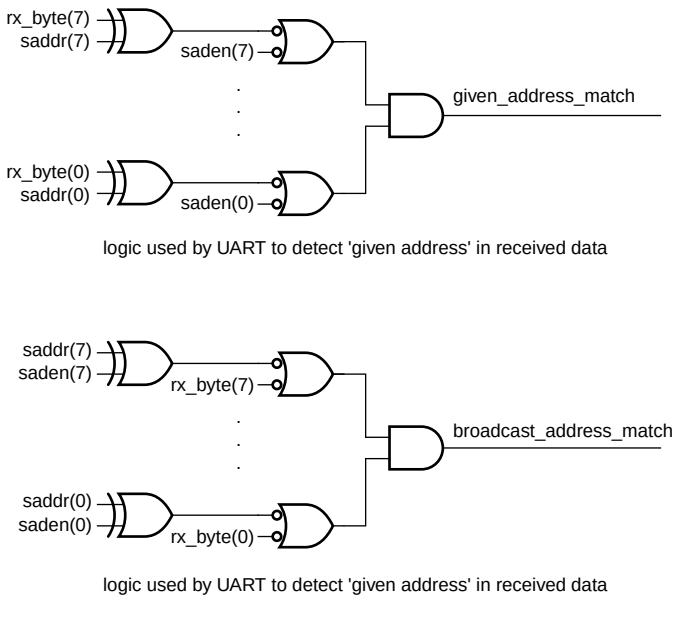


Fig 15. Schemes used by the UART to detect 'given' and 'broadcast' addresses when multiprocessor communications is enabled

address of all don't cares. This effectively disables the automatic addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

6.7 Serial Peripheral Interface (SPI)

6.7.1 SPI features

- Master or slave operation
- 10 MHz bit frequency (max)
- LSB first or MSB first data transfer
- Four programmable bit rates
- End of transmission (SPIF)
- Write-collision flag protection (WCOL)
- Wake-up from Idle mode (Slave mode only)

6.7.2 SPI description

The serial peripheral interface allows high-speed synchronous data transfer between the P89CV51RB2/RC2/RD2 and peripheral devices or between several P89CV51RB2/RC2/RD2 devices. Figure 16 shows the correspondence between master and slave SPI devices. The SPICLK pin is the clock output and input for the Master and Slave modes, respectively. The SPI clock generator will start following a write to the master devices SPI data register. The written data is then shifted out of the MOSI pin of the master device into the MOSI pin of the slave device. Following a complete transmission of one byte of data, the SPI clock generator is stopped and the SPI interrupt Flag (SPIF) is set. An SPI interrupt request will be generated if the SPI Interrupt Enable bit (SPIE) and the SPI interrupt enable bit, ES, are both set.

An external master drives the Slave Select input pin ($\overline{SS}$) LOW to select the SPI module as a slave. If $\overline{SS}$ has not been driven LOW, then the slave SPI unit is not active and the MOSI pin can also be used as an input port pin.

CPHA and CPOL control the phase and polarity of the SPI clock (SCK). Figure 17 and Figure 18 show the four possible combinations of these two bits.

register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags can only be cleared by software. All the modules share one interrupt vector. The PCA interrupt system is shown in Figure 20.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. The registers contain the bits that control the mode that each module will operate in.

The ECCF bit (from CCAPMn.0 where n = 0, 1, 2, 3, or 4 depending on the module) enables the CCFn flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module; see Figure 20.

PWM (CCAPMn.1) enables the PWM mode.

The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register.

The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition.

The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode, these registers are used to control the duty cycle of the output.

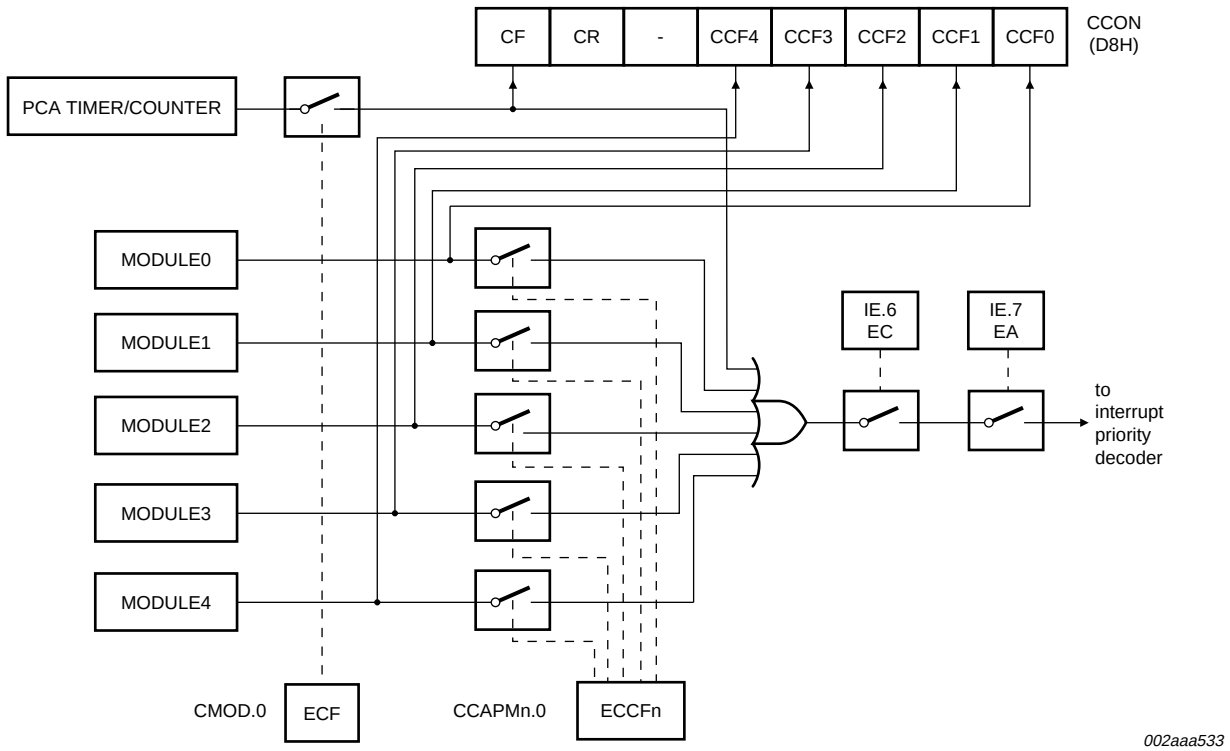


Fig 20. PCA interrupt system

Table 32. CMOD - PCA counter mode register (address D9H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF

Table 33. CMOD - PCA counter mode register (address D9H) bit description

Bit	Symbol	Description
7	CIDL	Counter Idle control. CIDL = 0 programs the PCA counter to continue functioning during Idle mode; CIDL = 1 programs it to be gated off during Idle mode.
6	WDTE	WatchDog Timer Enable. WDTE = 0 disables watchdog timer function on module 4; WDTE = 1 enables it.
5 to 3	-	Reserved for future use. Should be set to 0 by user programs.
2 to 1	CPS1, CPS0	PCA Count Pulse Select; see Table 34.
0	ECF	PCA Enable Counter overflow interrupt Flag. ECF = 1 enables CF bit in CCON to generate an interrupt; ECF = 0 disables that function.

Table 34. CMOD - PCA counter mode register (address D9H) count pulse select

CPS1	CPS0	Select PCA input
0	0	0 internal clock, f_{osc} / 6

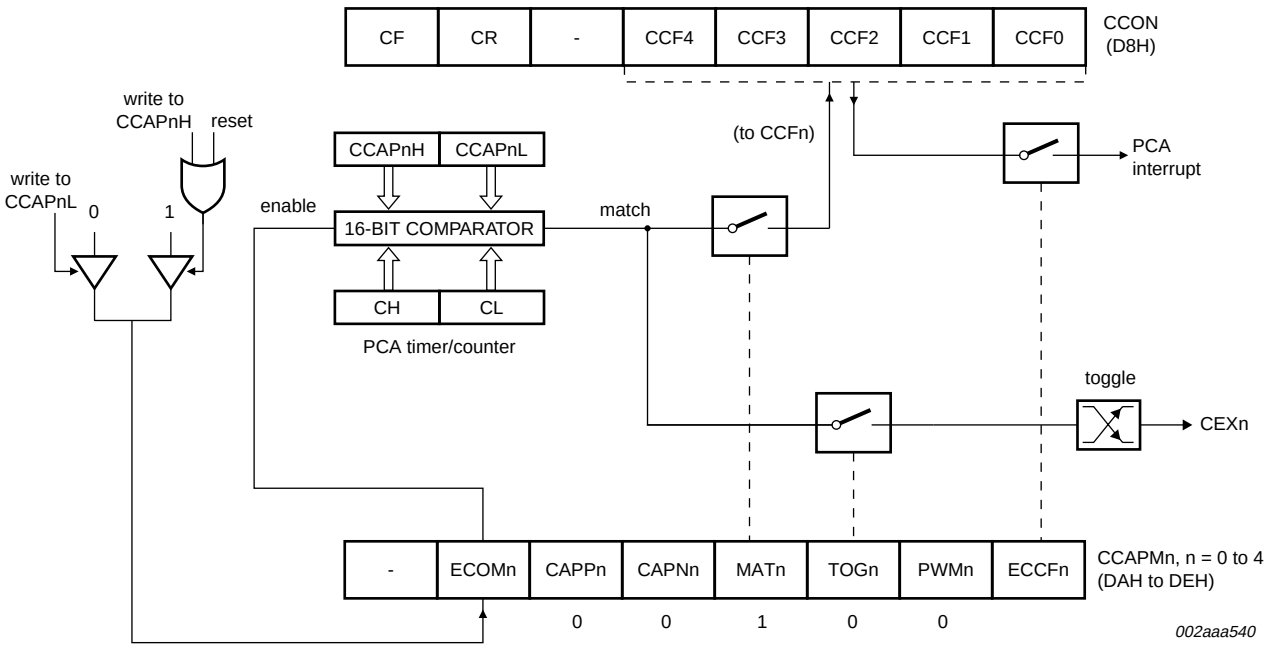


Fig 23. PCA High-speed output mode

6.9.4 Pulse width modulator mode

All of the PCA modules can be used as PWM outputs (Figure 24). Output frequency depends on the source for the PCA timer.

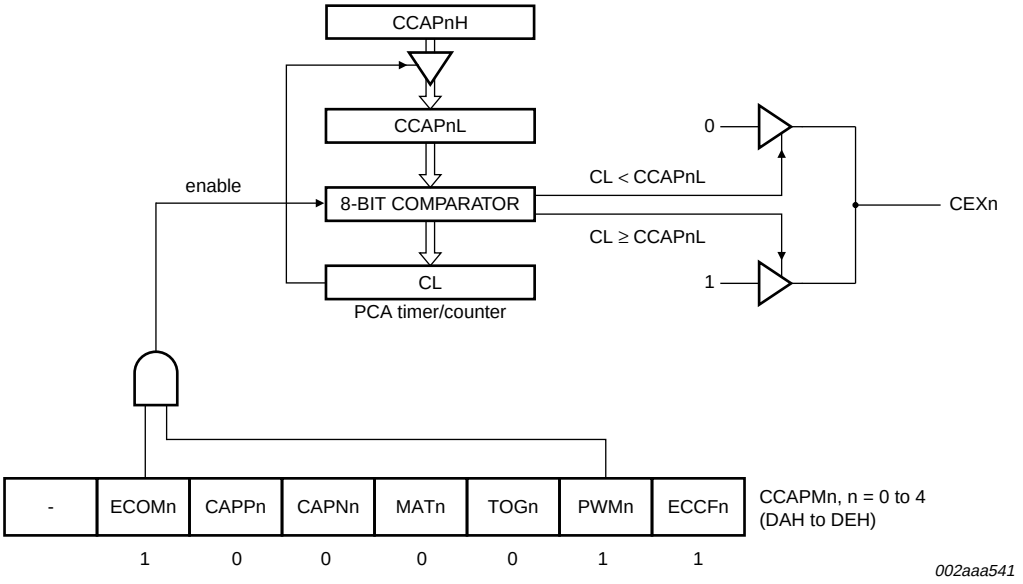


Fig 24. PCA PWM mode

All of the modules will have the same output frequency because they all share only one PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPnL. When the value of the PCA CL SFR is less than the value in the

Table 43. IE - Interrupt enable register 0 (address A8H) bit description *...continued*

Bit	Symbol	Description
4	ES	Serial port interrupt Enable.
3	ET1	Timer 1 overflow interrupt Enable.
2	EX1	External interrupt 1 Enable.
1	ET0	Timer 0 overflow interrupt Enable.
0	EX0	External interrupt 0 Enable.

Table 44. IP - Interrupt priority low register (address B8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Table 45. IP - Interrupt priority low register (address B8H) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to 0 by user programs.
6	PPC	PCA interrupt Priority Low.
5	PT2	Timer 2 interrupt Priority Low.
4	PS	Serial Port interrupt Priority Low.
3	PT1	Timer 1 interrupt Priority Low.
2	PX1	External interrupt 1 Priority Low.
1	PT0	Timer 0 interrupt Priority Low.
0	PX0	External interrupt 0 Priority Low.

Table 46. IPH - Interrupt priority high register (address B7H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Table 47. IPH - Interrupt priority high register (address B7H) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to 0 by user programs.
6	PPCH	PCA interrupt Priority High.
5	PT2H	Timer 2 interrupt Priority High.
4	PSH	Serial Port interrupt Priority High.
3	PT1H	Timer 1 interrupt Priority High.
2	PX1H	External interrupt 1 Priority High.
1	PT0H	Timer 0 interrupt Priority High.
0	PX0H	External interrupt 0 Priority High.

6.12 Power-saving modes

The device provides two power-saving modes of operation for applications where power consumption is critical. The two modes are Idle and Power-down; see Table 48.

6.12.1 Idle mode

Idle mode is entered by setting the IDL bit in the PCON register. In Idle mode, the program counter is stopped. The system clock continues to run and all interrupts and peripherals remain active. The on-chip RAM and the special function registers hold their data during this mode.

The device exits Idle mode through either a system interrupt or a hardware reset. When exiting Idle mode via system interrupt, the start of the interrupt clears the IDL bit and exits Idle mode. After exiting the Interrupt Service Routine (ISR), the interrupted program resumes execution at the instruction immediately following the instruction which invoked the Idle mode. A hardware reset starts the device similar to a power-on reset.

6.12.2 Power-down mode

The Power-down mode is entered by setting the PD bit in the PCON register. In the Power-down mode, the clock is stopped and external interrupts are active for level-sensitive interrupts only. SRAM contents are retained during power-down, the minimum V_{DD} level is 4.5 V.

The device exits Power-down mode through either an enabled external level-sensitive interrupt or a hardware reset. The start of the interrupt clears the PD bit and exits power-down. Holding an external interrupt pin LOW restarts the oscillator, the signal must hold LOW at least 1024 clock cycles before bringing back HIGH to complete the exit. When the interrupt signal is restored to logic V_{IH}, the interrupt service routine program execution resumes at the instruction immediately following the instruction which invoked Power-down mode. A hardware reset starts the device similar to a power-on reset.

To exit properly out of power-down, the reset or external interrupt should not be executed before the V_{DD} line is restored to its normal operating voltage. Be sure to hold V_{DD} voltage long enough at its normal operating level for the oscillator to restart and stabilize (normally less than 10 ms).

Table 48. Power-saving modes

Mode	Initiated by	State of MCU	Exited by
Idle	Software (Set IDL bit in PCON) MOV PCON, #01H	CLK is running. Interrupts, serial port and timers/counters are active. Program counter is stopped. ALE and $\overline{PSEN}$ signals at a HIGH-state during Idle. All registers remain unchanged.	Enabled interrupt or hardware reset. Start of interrupt clears IDL bit and exits Idle mode, after the ISR RETI instruction, program resumes execution beginning at the instruction following the one that invoked Idle mode. A hardware reset restarts the device similar to a power-on reset.
Power-down	Software (Set PD bit in PCON) MOV PCON, #02H	CLK is stopped. On-chip SRAM and SFR data is maintained. ALE and $\overline{PSEN}$ signals at a LOW-state during power-down. External interrupts are only active for level-sensitive interrupts, if enabled.	Enabled external level-sensitive interrupt or hardware reset. Start of interrupt clears PD bit and exits Power-down mode, after the ISR RETI instruction program resumes execution beginning at the instruction following the one that invoked Power-down mode. A hardware reset restarts the device similar to a power-on reset.

6.13.1.1 Clock control register (CKCON)

By default, the device runs at twelve clock cycles per machine cycle (12-clock mode). The device may be run at 6 clock cycles per machine cycle (6-clock mode) by programming of either a non-volatile bit (FX2) or an SFR bit (X2); see Table 52 “Clock modes”. If the FX2 non-volatile bit is programmed, the device will run in 6-clock mode and the X2 SFR bit has no effect. If the FX2 bit is erased, then the clock mode is controlled by the X2 SFR bit.

Table 50. CKCON - Clock control register (address 8FH) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	SPIX2	WDX2	PCAX2	SIX2	T2X2	T1X2	T0X2	X2

Table 51. CKCON - Clock control register (address 8FH) bit description

Bit	Symbol	Description
7	SPIX2	SPI clock; 0 = 6 clock cycles for each SPI clock cycle; 1 = 12 clock cycles
6	WDX2	Watchdog clock; 0 = 6 clock cycles for each WDT clock cycle; 1 = 12 clock cycles
5	PCAX2	PCA clock; 0 = 6 clock cycles for each PCA clock cycle; 1 = 12 clock cycles
4	SIX2	UART clock; 0 = 6 clock cycles for each UART clock cycle; 1 = 12 clock cycles
3	T2X2	Timer 2 clock; 0 = 6 clock cycles for each Timer 2 clock cycle; 1 = 12 clock cycles
2	T1X2	Timer 1 clock; 0 = 6 clock cycles for each Timer 1 clock cycle; 1 = 12 clock cycles
1	T0X2	Timer 0 clock; 0 = 6 clock cycles for each Timer 0 clock cycle; 1 = 12 clock cycles
0	X2	CPU clock; 0 = 12 clock cycles for each machine cycle; 1 = 6 clock cycles

Table 52. Clock modes

FX2 clock mode bit	X2 bit	CPU clock mode	Peripheral clock mode bit (e.g. T0X2)	Mode
erased	0	12-clock (default)	X	12-clock (default)
	1	6-clock	0	6-clock
			1	12-clock
programmed	X	6-clock	0	6-clock
			1	12-clock

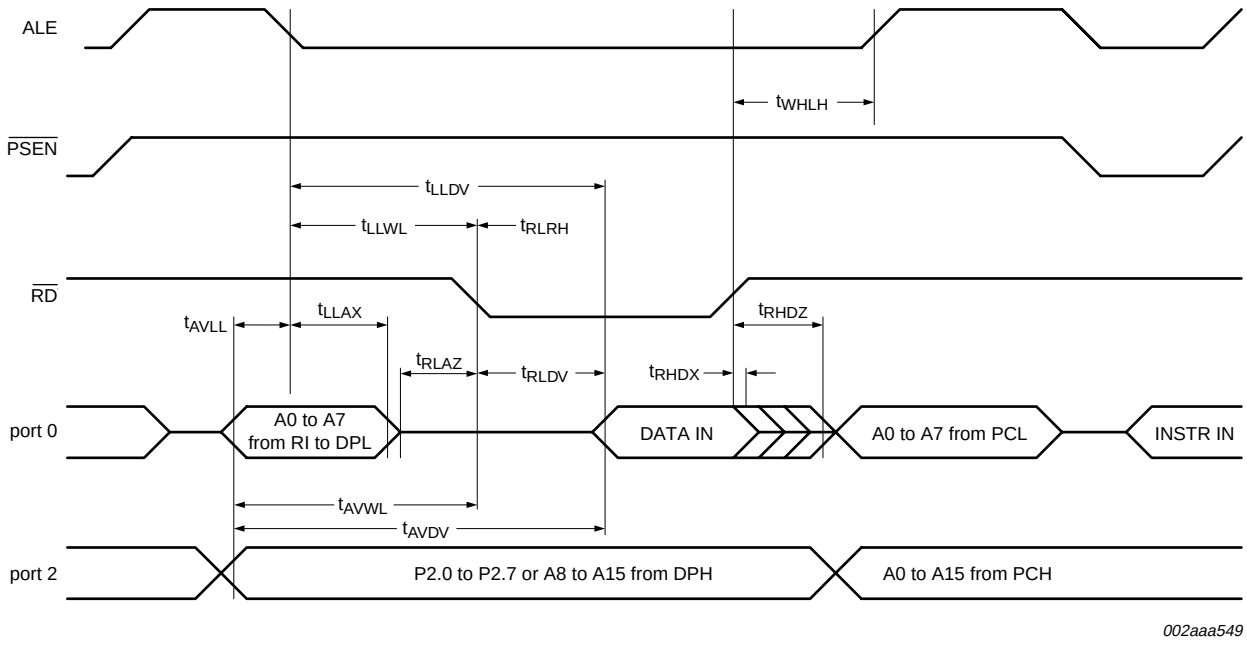


Fig 30. External data memory read cycle

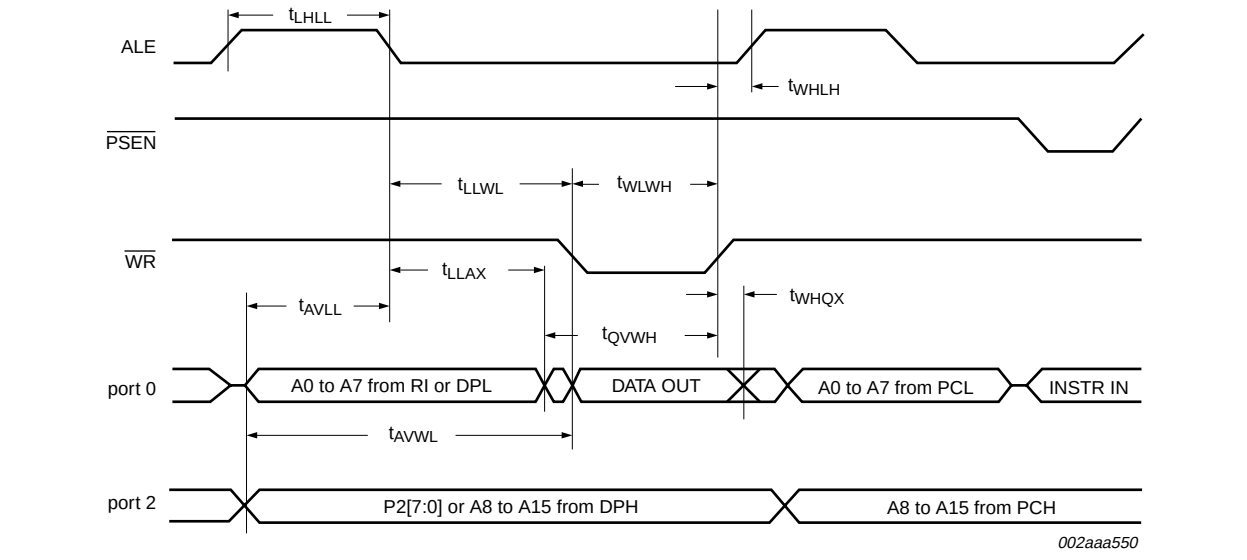


Fig 31. External data memory write cycle

Table 56. External clock drive

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
f_{osc}	oscillator frequency	-	-	0	40	MHz
$T_{cy(clk)}$	clock cycle time	25	-	-	-	ns
t_{CHCX}	clock HIGH time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCX}	clock LOW time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCH}	clock rise time	-	10	-	-	ns
t_{CHCL}	clock fall time	-	10	-	-	ns

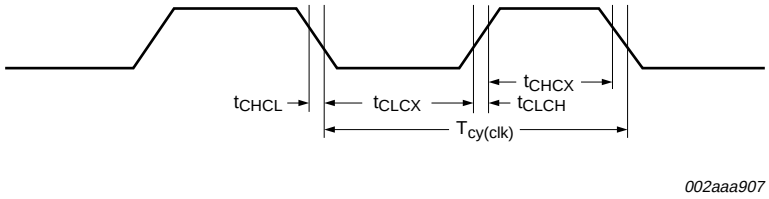


Fig 32. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

Table 57. Serial port timing

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	serial port clock cycle time	0.3	-	$12T_{cy(clk)}$	-	µs
t_{QVXH}	output data set-up to clock rising edge time	117	-	$10T_{cy(clk)} - 133$	-	ns
t_{XHQX}	output data hold after clock rising edge time	0	-	$2T_{cy(clk)} - 50$	-	ns
t_{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t_{XHDV}	input data valid to clock rising edge time	-	117	-	$10T_{cy(clk)} - 133$	ns

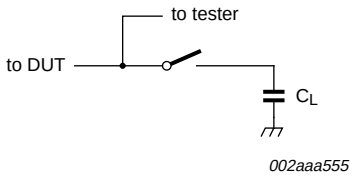
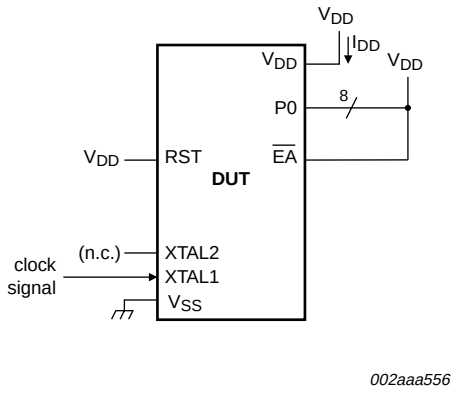
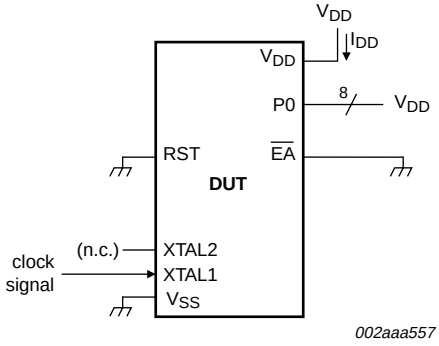


Fig 38. Test load example



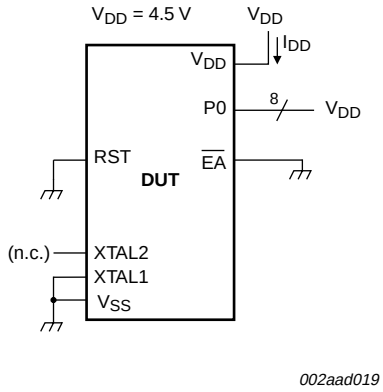
All other pins disconnected

Fig 39. I_{DD} test condition, Active mode



All other pins disconnected

Fig 40. I_{DD} test condition, Idle mode



All other pins disconnected

Fig 41. I_{DD} test condition, Power-down mode

11. Abbreviations

Table 59. Abbreviations

Acronym	Description
ALE	Address Latch Enable
CPU	Central Processing Unit
DPTR	Data PoinTeR
DUT	Device Under Test
EPROM	Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
ID	IDentifier
IAP	In-Application Programming
ISP	In-System Programming
LSB	Least Significant Bit
MCU	MicroController Unit
MSB	Most Significant Bit
PCA	Programmable Counter Array
PCH	Programmable Counter High
PCL	Programmable Counter Low
PWM	Pulse-Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
SFR	Special Function Register
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter
WDT	WatchDog Timer

12. Revision history

Table 60. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89CV51RB2_RC2_RD2_3	20090825	Product data sheet	-	P89CV51RB2_RC2_RD2_2
Modifications:	• Table 4: AUXR1, replaced '-' with 'ENBOOT'. • Table 4: CMOD, replaced 'C1H' with 'D9H'. • Table 8: Replaced '-' with 'ENBOOT'. • Table 32: Replaced 'C1H' with 'D9H'. • Table 33: Replaced 'C1H' with 'D9H'. • Table 34: Replaced 'C1H' with 'D9H'.			
P89CV51RB2_RC2_RD2_2	20090422	Product data sheet	-	P89CV51RB2_RC2_RD2_1
Modifications:	• Section 6.2.1: Corrected value for EXTRAM bit setting.			
P89CV51RB2_RC2_RD2_1	20071005	Product data sheet	-	-