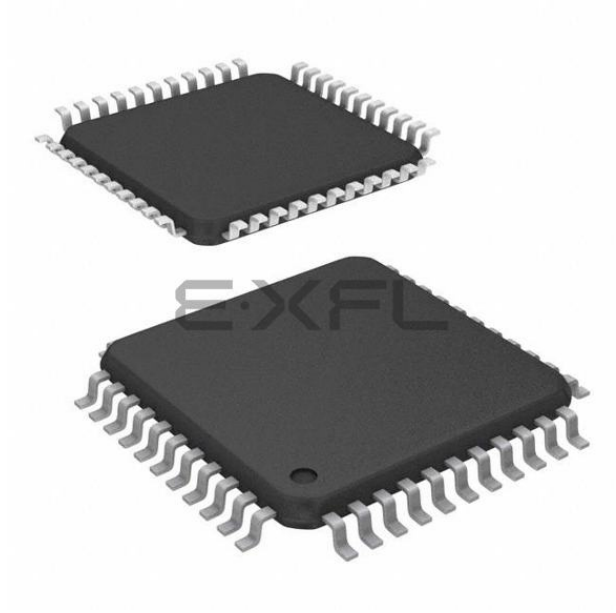

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Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89cv51rd2fbc-557

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR address	Bit functions and addresses[1]							
			MSB							LSB
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**
SPCR	SPI Control Register	D5H	SPIE	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
SPSR	SPI Status Register	AAH	SPIF	WCOL	-	-	-	-	-	-
SPDAT	SPI Data	86H	-	-	-	-	-	-	-	-
SP	Stack Pointer	81H	-	-	-	-	-	-	-	-
		Bit address	**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**
TCON*	Timer/counter Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
		Bit address	**CF**	**CE**	**CD**	**CC**	**CB**	**CA**	**C9**	**C8**
T2CON*	Timer/counter 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T}$2	CP/$\overline{RL}$2
T2MOD	Timer 2 Mode control	C9H	-	-	-	-	-	-	T2OE	DCEN
TH0	Timer 0 High	8CH	-	-	-	-	-	-	-	-
TH1	Timer 1 High	8DH	-	-	-	-	-	-	-	-
TH2	Timer 2 High	CDH	-	-	-	-	-	-	-	-
TL0	Timer 0 Low	8AH	-	-	-	-	-	-	-	-
TL1	Timer 1 Low	8BH	-	-	-	-	-	-	-	-
TL2	Timer 2 Low	CCH	-	-	-	-	-	-	-	-
TMOD	Timer/counter 0 and 1 Mode	89H	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0
WDTRST	WatchDog Timer Reset	A6H	-	-	-	-	-	-	-	-

[1] Unimplemented bits in SFRs (labeled '-') are 'X' (unknown) at all times. Unless otherwise specified, 1s should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are 0s although they are unknown when read.

6.2 Memory organization

The various P89CV51RB2/RC2/RD2 memory spaces are as follows:

- DATA

  128 B of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the stack may be in this area.

- IDATA

  Indirect Data. 256 B of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the stack may be in this area. This area includes the DATA area and the 128 B immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  'External' Data or auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the DPTR, R0, or R1. The P89CV51RB2/RC2/RD2 have 768 B of on-chip XDATA memory.

- CODE

  64 kB of code memory space, accessed as part of program execution and via the MOVC instruction. The P89CV51RB2/RC2/RD2 have 16/32/64 kB of on-chip code memory.

6.2.1 Expanded data RAM addressing

The P89CV51RB2/RC2/RD2 have 1 kB of data RAM; see Figure 4.

To access the expanded RAM (XRAM), the EXTRAM bit must be set and MOVX instructions must be used. The expanded memory is physically located on the chip and logically occupies the first bytes of external memory (addresses 000H to 2FFH).

Table 5. AUXR - Auxiliary function register (address 8EH) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	EXTRAM	AO

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3[6] ($\overline{WR}$), P3[7] ($\overline{RD}$), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM access (indirect addressing only):

```
MOVX @DPTR, A; DPTR contains 0A0H
```

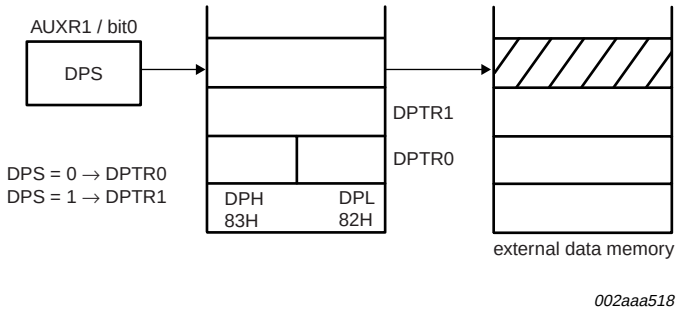


Fig 5. Dual data pointer organization

Table 8. AUXR1 - Auxiliary function register 1 (address A2H) bit allocation

Not bit addressable; reset value 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	ENBOOT	-	GF2	0	-	DPS

Table 9. AUXR1 - Auxiliary function register 1 (address A2H) bit description

Bit	Symbol	Description
7, 6, 4	-	Reserved for future use. Should be set to 0 by user programs.
5	ENBOOT	Enable BOOTROM
3	GF2	General purpose user-defined Flag.
2	0	This bit contains a hard-wired 0. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should be set to 0 by user programs.
0	DPS	Data Pointer Select. Chooses one of two data pointers for use by the program. See text for details.

6.2.3 Reset

At initial power-up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has weakly pulled all pins HIGH. Powering up the device without a valid reset could cause the MCU to start executing instructions from an indeterminate location. Such undefined states may inadvertently corrupt the code in the flash. A system reset will not affect the on-chip RAM while the device is running, however, the contents of the on-chip RAM during power-up are indeterminate.

When power is applied to the device, the RST pin must be held HIGH long enough for the oscillator to start-up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid power-on reset. An example of a method to extend the RST signal is to implement an RC circuit by connecting the RST pin to V_{DD} through a 10 µF capacitor and to V_{SS} through an 8.2 kΩ resistor as shown in Figure 6.

During initial power-up the POF flag in the PCON register is set to indicate an initial power-up condition. The POF flag will remain active until cleared by software.

Following a reset condition, under normal conditions, the MCU will start executing code from address 0000H in the user's code memory. However if either the $\overline{PSEN}$ pin was LOW when reset was exited, or the status bit = 1, the MCU will start executing code from the boot address. The boot address is formed using the value of the boot vector as the high byte of the address and 00H as the low byte.

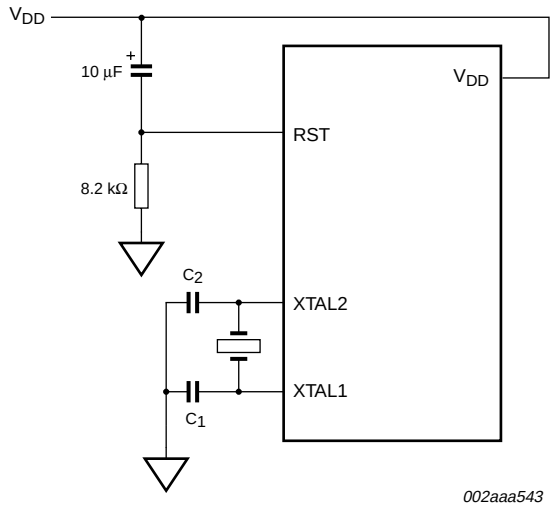


Fig 6. Power-on reset circuit

6.3 Flash memory

6.3.1 Flash organization

The P89CV51RB2/RC2/RD2 program memory consists of a 16/32/64 kB block for user code. The flash can be read or written in bytes and can be erased in 128-B pages. A chip erase function will erase the entire user code memory and its associated security bits. There are three methods for erasing or programming the flash memory that may be used. First, the flash may be programmed or erased in the end-user application by calling LOW-state routines through a common IAP entry point. Second, the on-chip ISP bootloader may be invoked. This ISP bootloader will, in turn, call LOW-state routines through the same common entry point that can be used by the end-user application. Third, the flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer which supports this device.

6.3.2 Features

- Flash internal program memory with 128-B page erase.
- Internal boot block, containing LOW-state IAP routines available to user code.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Default loader providing ISP via the serial port, located in upper-end of program memory.
- Programming and erase over the full operating voltage range.
- Read/Programming/Erase using ISP/IAP.

6.3.7 Using ISP

The ISP feature allows for a wide range of baud rates to be used in your application, independent of the oscillator frequency. It is also adaptable to a wide range of oscillator frequencies. This is accomplished by measuring the bit-time of a single bit in a received character. This information is then used to program the baud rate in terms of timer counts based on the oscillator frequency. The ISP feature requires that an initial character (an uppercase U) be sent to the P89CV51RB2/RC2/RD2 to establish the baud rate. The ISP firmware provides auto-echo of received characters. Once baud rate initialization has been performed, the ISP firmware will only accept Intel Hex-type records. Intel Hex records consist of ASCII characters used to represent hexadecimal values and are summarized below:

:NNAAAARRDD..DDCC<crlf>

In the Intel Hex record, the ‘NN’ represents the number of data bytes in the record. The P89CV51RB2/RC2/RD2 will accept up to 32 data bytes. The ‘AAAA’ string represents the address of the first byte in the record. If there are zero bytes in the record, this field is often set to 0000. The ‘RR’ string indicates the record type. A record type of ‘00’ is a data record. A record type of ‘01’ indicates the end-of-file mark. In this application, additional record types will be added to indicate either commands or data for the ISP facility.

The maximum number of data bytes in a record is limited to 32 (decimal). ISP commands are summarized in Table 11. As a record is received by the P89CV51RB2/RC2/RD2, the information in the record is stored internally and a checksum calculation is performed. The operation indicated by the record type is not performed until the entire record has been received. Should an error occur in the checksum, the P89CV51RB2/RC2/RD2 will send an ‘X’ out the serial port indicating a checksum error. If the checksum calculation is found to match the checksum in the record, then the command will be executed. In most cases, successful reception of the record will be indicated by transmitting a ‘.’ character out the serial port.

Table 12. IAP function calls *…continued*

IAP function	IAP call parameters
Program status bit, boot vector, 6×/12× bit	**Input parameters:** R1 = 06H or 86H (WDT feed) DPL = 00H = program status bit DPL = 01H = program boot vector DPL = 02H = 6×/12× bit ACC = boot vector value to program **Return parameter(s):** ACC = 00: pass ACC is not 00: fail
Read security bits, status bit, boot vector	**Input parameters:** ACC = 07H or 87H (WDT feed) DPL = 00H = security bits DPL = 01H = status bit DPL = 02H = boot vector **Return parameter(s):** ACC = 00 SoftICE S/N-match 0 SB 0 DBL_CLK
Erase page	**Input parameters:** R1 = 08H or 88H (WDT feed) DPH = page address high byte DPL = page address low byte **Return parameter(s):** ACC = 00: pass ACC is not 00: fail

6.4 Timers/counters 0 and 1

The two 16-bit timer/counter registers: Timer 0 and Timer 1 can be configured to operate either as timers or event counters (see Table 13 and Table 14).

In the ‘Timer’ function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of six oscillator periods, the count rate is $\frac{1}{6}$ of the oscillator frequency.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once every machine cycle.

When the samples show a HIGH in one cycle and a LOW in the next cycle, the count is incremented. The new count value appears in the register in the machine cycle following the one in which the transition was detected. Since it takes two machine cycles (12 oscillator periods) for a 1-to-0 transition to be recognized, the maximum count rate is $\frac{1}{12}$ of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle. In addition to the ‘Timer’ or ‘Counter’ selection, Timer 0 and Timer 1 have four selectable operating modes.

The ‘Timer’ or ‘Counter’ function is selected by control bits C/$\overline{T}$ in the special function register TMOD. These two timers/counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both timers/counters. Mode 3 is different. The four operating modes are described in the following text.

Table 13. TMOD - Timer/Counter mode control register (address 89H) bit allocation

Not bit addressable; reset value: 0000 0000B; reset source(s): any source.

Bit	7	6	5	4	3	2	1	0
Symbol	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

Table 14. TMOD - Timer/Counter mode control register (address 89H) bit description

Bit	Symbol	Description
7	T1GATE	Gating control for Timer 1. When set, timer/counter is enabled only while the $\overline{INT1}$ pin is HIGH and the TR1 control bit is set. When cleared, Timer 1 is enabled when the TR1 control bit is set.
6	T1C/$\overline{T}$	Timer or counter select for Timer 1. Cleared for timer operation. Set for counter operation (input from T1 input pin).
5	T1M1	Mode select for Timer 1.
4	T1M0	
3	T0GATE	Gating control for Timer 0. When set, timer/counter is enabled only while the $\overline{INT0}$ pin is HIGH and the TR0 control bit is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
2	T0C/$\overline{T}$	Timer or counter select for Timer 0. Cleared for timer operation. Set for counter operation (input from T0 input pin).
1	T0M1	Mode select for Timer 0.
0	T0M0	

Table 15. TMOD - Timer/Counter mode control register (address 89H) M1/M0 operating mode

M1	M0	Operating mode	
0	0	0	8048 timer ‘TLx’ serves as 5-bit prescaler.
0	1	1	16-bit timer/counter ‘THx’ and ‘TLx' are cascaded; there is no prescaler.
1	0	2	8-bit auto-reload timer/counter ‘THx’ holds a value which is to be reloaded into ‘TLx’ each time it overflows.
1	1	3	(Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	3	(Timer 1) timer/counter 1 stopped.

Table 16. TCON - Timer/Counter control register (address 88H) bit allocation

Bit addressable; reset value: 0000 0000B; reset source(s): any reset.

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 20. T2CON - Timer/Counter 2 control register (address C8H) bit description *...continued*

Bit	Symbol	Description
4	TCLK	Transmit clock flag. When set, causes the UART to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	Start/stop control for Timer 2. A logic 1 enables the timer to run.
1	C/$\overline{T}$2	Timer or counter select. (Timer 2) 0 = internal timer (f_{osc} / 6) 1 = external event counter (falling edge triggered; external clock's maximum rate = f_{osc} / 12)
0	CP/$\overline{RL}$2	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 21. T2MOD - Timer 2 mode control register (address C9H) bit allocation

Not bit addressable; reset value: XX00 0000B.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T2OE	DCEN

Table 22. T2MOD - Timer 2 mode control register (address C9H) bit description

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to 0 by user programs.
1	T2OE	Timer 2 Output Enable bit. Used in programmable Clock-out mode only.
0	DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

6.5.1 Capture mode

In the Capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0 Timer 2 is a 16-bit timer or counter (as selected by C/$\overline{T}$2 in T2CON) which upon overflowing sets bit TF2, the Timer 2 overflow bit. The Capture mode is illustrated in Figure 11.

This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit ET2 in the IE register). If EXEN2 = 1, Timer 2 operates as described above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively.

In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt). The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt.

6.5.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1[0], Clock-out mode). This pin, besides being a regular I/O pin, has two additional functions. It can be programmed:

1. To input the external clock for timer/counter 2, or
2. To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the timer/counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{OscillatorFrequency}{2 \times (65536 - (RCAP2H, RCAP2L))} \quad (2)$$

Where (RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-out mode, Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud rate generator.

6.5.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART transmit and receive baud rates to be derived from either Timer 1 or Timer 2; see Section 6.6 for details. When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When TCLK = 1, Timer 2 is used as the UART transmit baud rate generator. RCLK has the same effect for the UART receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates, Timer 1 or Timer 2.

Figure 14 shows Timer 2 in Baud rate generator mode:

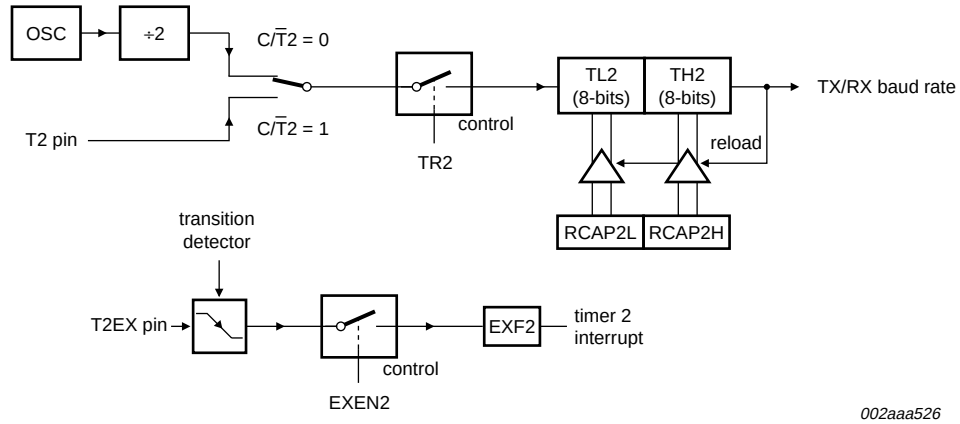


Fig 14. Timer 2 in Baud rate generator mode

6.6.6 More about UART Mode 1

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset to align its roll-overs with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated.

6.6.7 More about UART Modes 2 and 3

Reception is performed in the same manner as in Mode 1.

The signal to load special function register SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF.

6.6.8 Multiprocessor communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed so that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte: the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte, i.e. the received 9th bit is 0. However, an address byte having the 9th bit set to 1 will interrupt all slaves, so that each slave can examine the received byte to see if it is being addressed or not. The addressed slave will clear its SM2 bit and prepare to receive the data (still 9 bits long) that follow. The slaves that were not addressed leave their SM2 bits set and ignore the subsequent data bytes.

address of all don't cares. This effectively disables the automatic addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

6.7 Serial Peripheral Interface (SPI)

6.7.1 SPI features

- Master or slave operation
- 10 MHz bit frequency (max)
- LSB first or MSB first data transfer
- Four programmable bit rates
- End of transmission (SPIF)
- Write-collision flag protection (WCOL)
- Wake-up from Idle mode (Slave mode only)

6.7.2 SPI description

The serial peripheral interface allows high-speed synchronous data transfer between the P89CV51RB2/RC2/RD2 and peripheral devices or between several P89CV51RB2/RC2/RD2 devices. Figure 16 shows the correspondence between master and slave SPI devices. The SPICLK pin is the clock output and input for the Master and Slave modes, respectively. The SPI clock generator will start following a write to the master devices SPI data register. The written data is then shifted out of the MOSI pin of the master device into the MOSI pin of the slave device. Following a complete transmission of one byte of data, the SPI clock generator is stopped and the SPI interrupt Flag (SPIF) is set. An SPI interrupt request will be generated if the SPI Interrupt Enable bit (SPIE) and the SPI interrupt enable bit, ES, are both set.

An external master drives the Slave Select input pin ($\overline{SS}$) LOW to select the SPI module as a slave. If $\overline{SS}$ has not been driven LOW, then the slave SPI unit is not active and the MOSI pin can also be used as an input port pin.

CPHA and CPOL control the phase and polarity of the SPI clock (SCK). Figure 17 and Figure 18 show the four possible combinations of these two bits.

Table 38. CCAPMn - PCA modules compare/capture register (address CCAPM0 DAH, CCAPM1 DBH, CCAPM2 DCH, CCAPM3 DDH, CCAPM4 DEH) bit description

Bit	Symbol	Description
2	TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
1	PWMn	Pulse Width Modulation mode. PWMn = 1 enables the CEXn pin to be used as a pulse-width modulated output.
0	ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

Table 39. PCA module modes (CCAPMn register)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	Module function
0	0	0	0	0	0	0	no operation
X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	0	1	0	0	0	X	16-bit capture by a negative-edge trigger on CEXn
X	1	1	0	0	0	X	16-bit capture by any transition on CEXn
1	0	0	1	0	0	X	16-bit software timer
1	0	0	1	1	0	X	16-bit high-speed output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	X	0	X	watchdog timer

6.9.1 PCA capture mode

To use one of the PCA modules in the Capture mode (Figure 21), either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs, the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH).

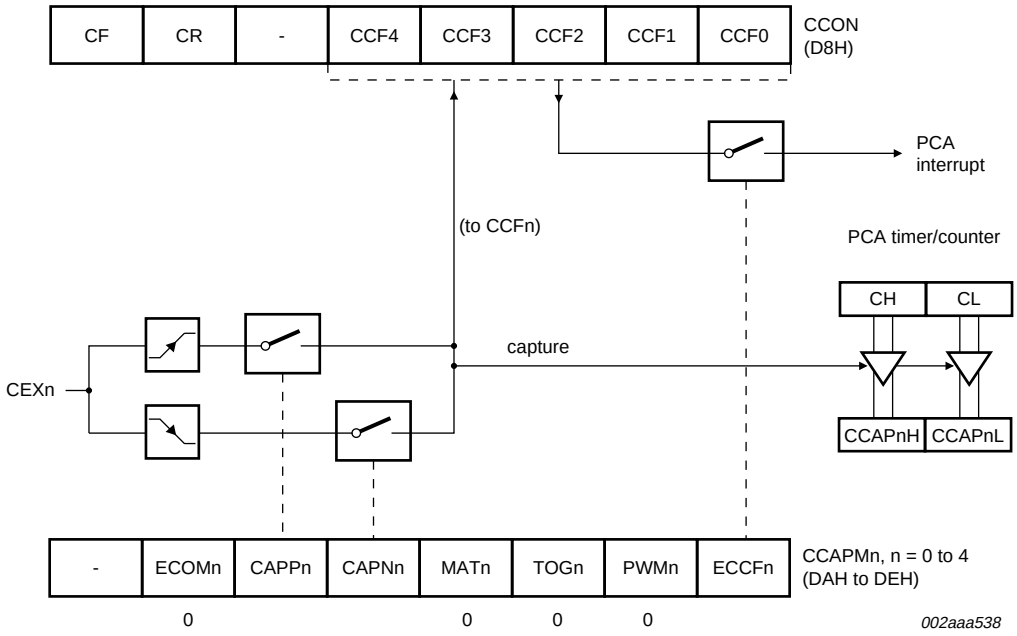


Fig 21. PCA Capture mode

If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated.

6.9.2 16-bit software timer mode

The PCA modules can be used as software timers (Figure 22) by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set.

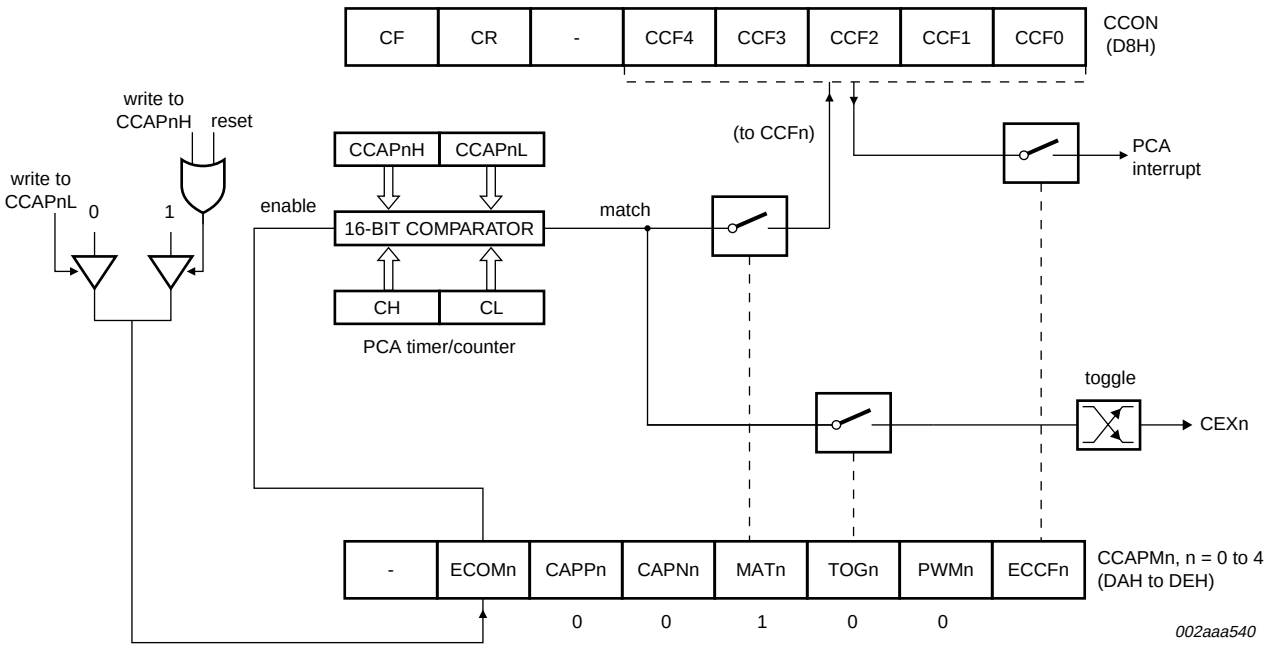


Fig 23. PCA High-speed output mode

6.9.4 Pulse width modulator mode

All of the PCA modules can be used as PWM outputs (Figure 24). Output frequency depends on the source for the PCA timer.

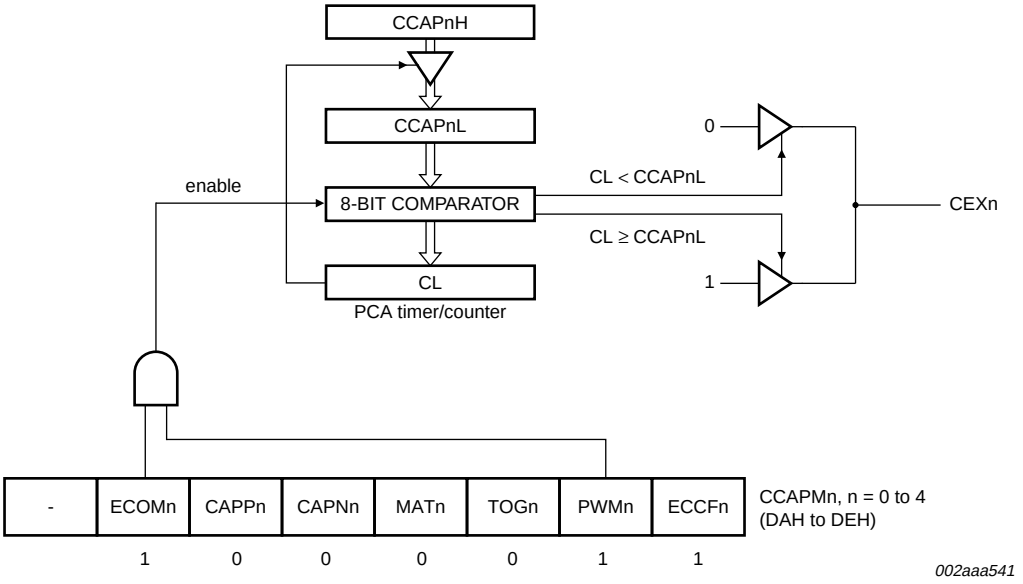


Fig 24. PCA PWM mode

All of the modules will have the same output frequency because they all share only one PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPnL. When the value of the PCA CL SFR is less than the value in the

module's CCAPnL SFR, the output will be LOW; when it is equal to, or greater, the output will be HIGH. When CL overflows from FFH to 00H, CCAPnL is reloaded with the value in CCAPnH. This allows the PWM to be updated without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable PWM mode.

6.9.5 PCA watchdog timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed. Figure 24 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven HIGH.

User's software then must periodically change (CCAP4H, CCAP4L) to keep a match from occurring with the PCA timer (CH, CL). This code is given in the subroutine WATCHDOG shown below.

In order to hold off the reset, the user has three options:

- Periodically change the compare value so it will never match the PCA timer.
- Periodically change the PCA timer value so it will never match the compare values.
- Disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in the third option. If the program counter ever reaches an undesired value, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember that the PCA timer is the time base for **all** modules; changing the time base for other modules is not recommended. Thus, in most applications the first option is best.

```
;CALL the following WATCHDOG subroutine periodically.
   CLR    EA           ;Hold off interrupts
   MOV    CCAP4L,#00   ;Next compare value is within 255 counts of
                        current PCA timer value
   MOV    CCAP4H,CH
   SETB   EA           ;Re-enable interrupts
   RET
```

Do not use this routine as part of an interrupt service routine, because if the program counter would enter an infinite loop, still interrupts will be serviced and the watchdog will continually keep getting reset. Because this would defeat the purpose of the watchdog, it is recommended that this subroutine is called from the main program within 2^{16} PCA timer counts.

6.10 Security bits

The security bits protect against software piracy and prevent the contents of the flash from being read by unauthorized parties in Parallel programmer mode and ISP mode. Since the end application might need to erase pages and read from the code memory, the security bits have no effect in IAP mode. However, the security bits' programmed/erased state may be read using IAP function calls allowing the end-user code to limit access, if desired. The security bits and their effects are shown in Table 40.

Note: On this device, MOVC instructions executed from external code memory are prevented from fetching code bytes from internal code memory.

Table 40. Security bit functions

Security bit	Description
1	Write protect. When programmed, prohibits further erasing or programming, except to program other security bits or a chip erase.
2	Read protect. When programmed, inhibits reading of user code memory.
3	External execution inhibit. When programmed, prevents any execution of instructions from external code memory.

6.11 Interrupt priority and polling sequence

The device supports eight interrupt sources under a four-level priority scheme. Table 41 summarizes the polling sequence of the supported interrupts. Note that the SPI serial interface and the UART share the same interrupt vector; see Figure 25.

Table 41. Interrupt polling sequence

Description	Interrupt flag	Vector address	Interrupt enable	Interrupt priority	Service priority	Wake-up Power-down
External Interrupt 0	IE0	0003H	EX0	PX0/PX0H	1 (highest)	yes
T0	TF0	000BH	ET0	PT0/PT0H	2	no
External Interrupt 1	IE1	0013H	EX1	PX1/PX1H	3	yes
T1	TF1	001BH	ET1	PT1/PT1H	4	no
UART	TI/RI	0023H	ES	PS/PSH	5	no
SPI	SPIF	0023H	ES	PS/PSH	5	no
PCA	CF/CCFn	0033H	EC	PPC/PPCH	7	no
T2	TF2, EXF2	003BH	ET2	PT2/PT2H	6	no

Table 43. IE - Interrupt enable register 0 (address A8H) bit description *...continued*

Bit	Symbol	Description
4	ES	Serial port interrupt Enable.
3	ET1	Timer 1 overflow interrupt Enable.
2	EX1	External interrupt 1 Enable.
1	ET0	Timer 0 overflow interrupt Enable.
0	EX0	External interrupt 0 Enable.

Table 44. IP - Interrupt priority low register (address B8H) bit allocation

Bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Table 45. IP - Interrupt priority low register (address B8H) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to 0 by user programs.
6	PPC	PCA interrupt Priority Low.
5	PT2	Timer 2 interrupt Priority Low.
4	PS	Serial Port interrupt Priority Low.
3	PT1	Timer 1 interrupt Priority Low.
2	PX1	External interrupt 1 Priority Low.
1	PT0	Timer 0 interrupt Priority Low.
0	PX0	External interrupt 0 Priority Low.

Table 46. IPH - Interrupt priority high register (address B7H) bit allocation

Not bit addressable; reset value: 00H.

Bit	7	6	5	4	3	2	1	0
Symbol	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Table 47. IPH - Interrupt priority high register (address B7H) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to 0 by user programs.
6	PPCH	PCA interrupt Priority High.
5	PT2H	Timer 2 interrupt Priority High.
4	PSH	Serial Port interrupt Priority High.
3	PT1H	Timer 1 interrupt Priority High.
2	PX1H	External interrupt 1 Priority High.
1	PT0H	Timer 0 interrupt Priority High.
0	PX0H	External interrupt 0 Priority High.

7. Limiting values

Table 53. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Parameters are valid over operating temperature range unless otherwise specified; all voltages are with respect to V_{SS} unless otherwise noted.

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
V_I	input voltage	on $\overline{EA}$ pin to V_{SS}	–0.5	+14	V
V_n	voltage on any other pin	except V_{SS}; with respect to V_{DD}	–0.5	V_{DD} + 0.5	V
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	15	mA
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W

8. Static characteristics

Table 54. Static characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$n_{endu(fl)}$	endurance of flash memory	JEDEC Standard A117	[1]	10000	-	-	cycles
$t_{ret(fl)}$	flash memory retention time	JEDEC Standard A103	[1]	100	-	-	years
I_{latch}	I/O latch-up current	JEDEC Standard 78	[1]	100 + I_{DD}	-	-	mA
$V_{th(HL)}$	HIGH-LOW threshold voltage			–0.5	-	+0.2V_{DD} – 0.1	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except XTAL1, RST		0.2V_{DD} + 0.9	-	V_{DD} + 0.5	V
V_{OL}	LOW-level output voltage	V_{DD} = 4.5 V; except $\overline{PSEN}$, ALE	[2][3][4]				
		I_{OL} = 1.6 mA		-	-	0.4	V
		V_{DD} = 4.5 V; ALE, $\overline{PSEN}$					
		I_{OL} = 3.2 mA		-	-	0.45	V
V_{OH}	HIGH-level output voltage	V_{DD} = 4.5 V; ports 1, 2, 3, 4	[5]				
		I_{OH} = –30 µA		V_{DD} – 0.7	-	-	V
		V_{DD} = 4.5 V; port 0 in External bus mode, ALE, $\overline{PSEN}$					
		I_{OH} = –3.2 mA		V_{DD} – 0.7	-	-	V
I_{IL}	LOW-level input current	V_I = 0.4 V; ports 1, 2, 3, 4		–1	-	–75	µA
I_{THL}	HIGH-LOW transition current	V_I = 2 V; ports 1, 2, 3, 4	[6]	-	-	–650	µA
I_{LI}	input leakage current	0.45 V < V_I < V_{DD} – 0.3 V; port 0		-	-	±10	µA
		0 V < V_I < 6 V		-	-	10	µA

Table 54. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{pd}	pull-down resistance	on pin RST		40	-	225	kΩ
C_{iss}	input capacitance	1 MHz; T_{amb} = 25 °C; V_I = 0 V	[7]	-	-	15	pF
$I_{DD(oper)}$	operating supply current	f_{osc} = 12 MHz		-	-	11.5	mA
		f_{osc} = 40 MHz		-	-	50	mA
		Programming and erase mode		-	-	70	mA
$I_{DD(idle)}$	Idle mode supply current	f_{osc} = 12 MHz		-	-	8.5	mA
		f_{osc} = 40 MHz		-	-	42	mA
$I_{DD(pd)}$	Power-down mode supply current	minimum V_{DD} = 4.5 V		-	-	90	µA

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2] Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

a) Maximum I_{OL} per 8-bit port: 26 mA

b) Maximum I_{OL} total for all outputs: 71 mA

c) If I_{OL} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[3] Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

[4] Load capacitance for Port 0, ALE and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

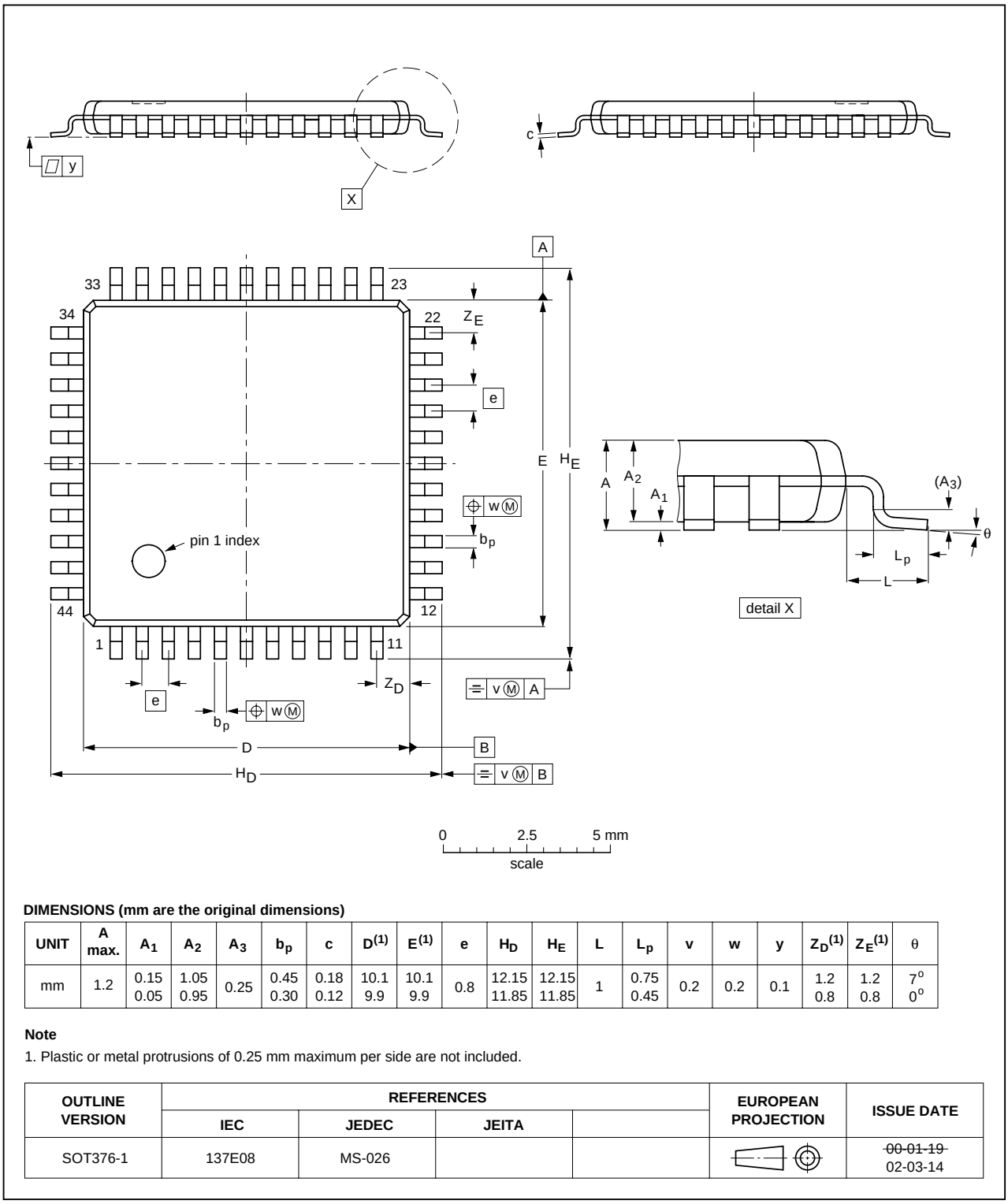
[5] Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{DD} − 0.7 V specification when the address bits are stabilizing.

[6] Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_I is approximately 2 V.

[7] Pin capacitance is characterized but not tested. Capacitance on pin $\overline{EA}$ = 25 pF (max.).

10. Package outline

TQFP44: plastic thin quad flat package; 44 leads; body 10 x 10 x 1.0 mm **SOT376-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.45 0.30	0.18 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT376-1	137E08	MS-026				~~00-01-19~~ 02-03-14

Fig 42. Package outline SOT376-1 (TQFP44)