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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	20
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32jg1b100f256im32-c0

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32JG1. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M3 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 256 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.3\text{ V}$, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to [Table 4.2 General Operating Conditions on page 11](#) for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	$^{\circ}\text{C}$
External main supply voltage	V_{DDMAX}		0	—	3.8	V
External main supply voltage ramp rate	$V_{DDRAMP MAX}$		—	—	1	V / μs
Voltage on any 5V tolerant GPIO pin ¹	V_{DIGPIN}		-0.3	—	Min of 5.25 and IOVDD +2	V
Voltage on non-5V tolerant GPIO pins			-0.3	—	IOVDD+0.3	V
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
Total current into VDD power lines (source)	I_{VDDMAX}		—	—	200	mA
Total current into VSS ground lines (sink)	I_{VSSMAX}		—	—	200	mA
Current per I/O pin (sink)	I_{IOMAX}		—	—	50	mA
Current per I/O pin (source)			—	—	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		—	—	200	mA
Current for all I/O pins (source)			—	—	200	mA
Voltage difference between AVDD and VREGVDD	ΔV_{DD}		—	—	0.3	V
Junction Temperature for -G grade devices	T_J		-40	—	105	$^{\circ}\text{C}$
Junction Temperature for -I grade devices			-40	—	125	$^{\circ}\text{C}$

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	THETA _{JA}	QFN32 Package, 2-Layer PCB, Air velocity = 0 m/s	—	79	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 1 m/s	—	62.2	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 2 m/s	—	54.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 0 m/s	—	32	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 1 m/s	—	28.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 2 m/s	—	26.9	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 0 m/s	—	64.5	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 1 m/s	—	51.6	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 2 m/s	—	47.7	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 0 m/s	—	26.2	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 1 m/s	—	23.1	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 2 m/s	—	22.1	—	°C/W

4.1.5 Current Consumption

4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T_{OP} = 25 °C. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See [Figure 5.1 EFM32JG1 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 48](#).

Table 4.5. Current Consumption 3.3V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled	I _{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash ¹	—	127	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	88	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	100	105	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	106	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	222	350	μA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled	I _{EM1}	38.4 MHz crystal ¹	—	61	—	μA/MHz
		38 MHz HFRCO	—	35	38	μA/MHz
		26 MHz HFRCO	—	37	41	μA/MHz
		1 MHz HFRCO	—	157	275	μA/MHz
Current consumption in EM2 Deep Sleep mode.	I _{EM2}	Full RAM retention and RTCC running from LFXO	—	3.3	—	μA
		4 kB RAM retention and RTCC running from LFRCO	—	3	6.3	μA
Current consumption in EM3 Stop mode	I _{EM3}	Full RAM retention and CRYO-TIMER running from ULFRCO	—	2.8	6	μA
Current consumption in EM4H Hibernate mode	I _{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1.1	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.65	—	μA
		128 byte RAM retention, no RTCC	—	0.65	1.3	μA
Current consumption in EM4S Shutoff mode	I _{EM4S}	no RAM retention, no RTCC	—	0.04	0.11	μA

Note:

1. CMU_HFXOCTRL_LOWPOWER=1

4.1.8.2 HFXO

Table 4.11. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{HFXO}		38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 38.4 MHz	—	—	60	Ω
Supported range of crystal load capacitance ¹	$C_{\text{HFXO_CL}}$		6	—	12	pF
On-chip tuning cap range ²	$C_{\text{HFXO_T}}$	On each of HFXTAL_N and HFXTAL_P pins	9	20	25	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.04	—	pF
Startup time	t_{HFXO}	38.4 MHz, ESR = 50 Ω , C_L = 10 pF	—	300	—	μs
Frequency Tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ω , C_L = 10 pF	-40	—	40	ppm

Note:

1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be $C_{\text{HFXO_T}}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.1.8.3 LFRCO

Table 4.12. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL, $T_{\text{AMB}} \leq 85^\circ\text{C}$	30.474	32.768	34.243	kHz
		ENVREF = 1 in CMU_LFRCOCTRL, $T_{\text{AMB}} > 85^\circ\text{C}$	30.474	—	39.7	kHz
		ENVREF = 0 in CMU_LFRCOCTRL	30.474	32.768	33.915	kHz
Startup time	t_{LFRCO}		—	500	—	μs
Current consumption ¹	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:

1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE ² = NORMAL	I _{ADC_NORMAL_HP}	35 ksp/s / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ₃	—	102	—	μA
		5 ksp/s / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 ₃	—	17	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ² = KEEPINSTANDBY or KEEPINSLOWACC	I _{ADC_STANDBY_HP}	125 ksp/s / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ₃	—	162	—	μA
		35 ksp/s / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ₃	—	123	—	μA
Current from HFPERCLK	I _{ADC_CLK}	HFPERCLK = 16 MHz	—	140	—	μA
ADC Clock Frequency	f _{ADCCLK}		—	—	16	MHz
Throughput rate	f _{ADCRATE}		—	—	1	Msp/s
Conversion time ⁴	t _{ADCCONV}	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	t _{ADCSTART}	WARMUPMODE ² = NORMAL	—	—	5	μs
		WARMUPMODE ² = KEEPINSTANDBY	—	—	2	μs
		WARMUPMODE ² = KEEPINSLOWACC	—	—	1	μs
SNDR at 1Msp/s and f _{in} = 10kHz	SNDR _{ADC}	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	58	67	—	dB
		v _{refp_in} = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-Free Dynamic Range (SFDR)	SFDR _{ADC}	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Input referred ADC noise, rms	V _{REF_NOISE}	Including quantization noise and distortion	—	380	—	μV
Offset Error	V _{ADCOFFSETERR}		-3	0.25	3	LSB
Gain error in ADC	V _{ADC_GAIN}	Using internal reference	—	-0.2	5	%
		Using external reference	—	-1	—	%
Differential non-linearity (DNL)	DNL _{ADC}	12 bit resolution, No Missing Codes	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL _{ADC}	12 bit resolution	-6	—	6	LSB
Temperature Sensor Slope	V _{TS_SLOPE}		—	-1.84	—	mV/°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value)	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	μs
		Step value is changed	—	1	—	μs
Current consumption in EM0 or EM1 ²	I_{IDAC}	Source mode, excluding output current	—	8.9	13	μA
		Sink mode, excluding output current	—	12	16	μA
Current consumption in EM2 or EM3 ²	I_{IDAC}	Source mode, excluding output current, duty cycle mode, $T = 25^{\circ}C$	—	1.04	—	μA
		Sink mode, excluding output current, duty cycle mode, $T = 25^{\circ}C$	—	1.08	—	μA
		Source mode, excluding output current, duty cycle mode, $T \geq 85^{\circ}C$	—	8.9	—	μA
		Sink mode, excluding output current, duty cycle mode, $T \geq 85^{\circ}C$	—	12	—	μA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.04	—	%
		RANGESEL1=1, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.02	—	%
		RANGESEL1=2, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 150 \text{ mV})$	—	0.02	—	%
		RANGESEL1=3, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 250 \text{ mV})$	—	0.02	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.18	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.08	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.02	—	%

Note:

1. In IDAC_CURPROG register
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.16 USART SPI

SPI Master Timing

Table 4.24. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2}	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI ^{1 2}	t_{CS_MO}		0	—	8	ns
SCLK to MOSI ^{1 2}	t_{SCLK_MO}		3	—	20	ns
MISO setup time ^{1 2}	t_{SU_MI}	IOVDD = 1.62 V	56	—	—	ns
		IOVDD = 3.0 V	37	—	—	ns
MISO hold time ^{1 2}	t_{H_MI}		6	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

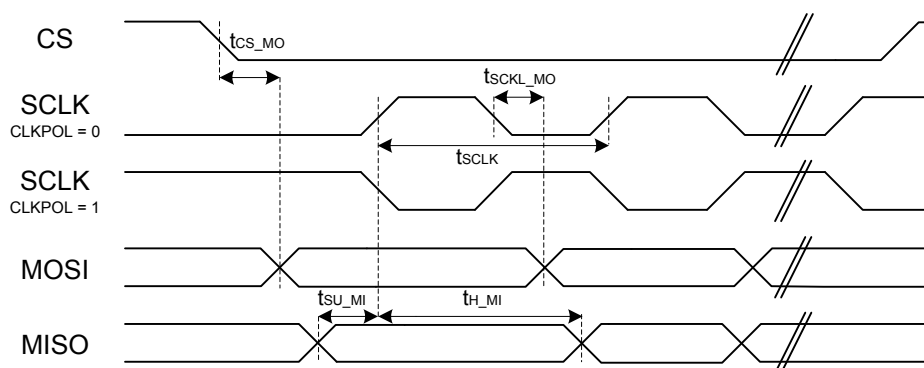


Figure 4.1. SPI Master Timing Diagram

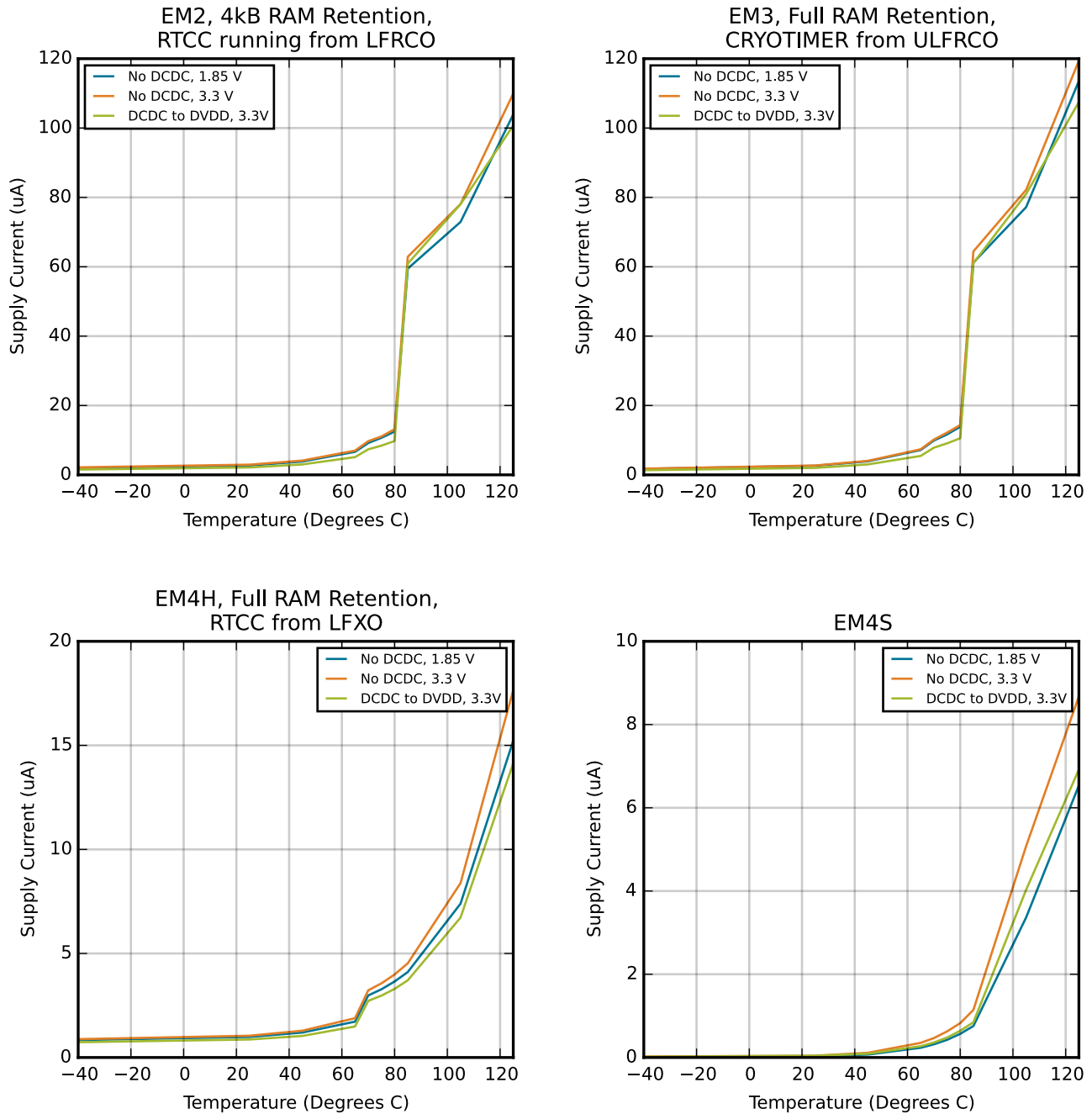


Figure 4.5. EM2, EM3, EM4H and EM4S Typical Supply Current

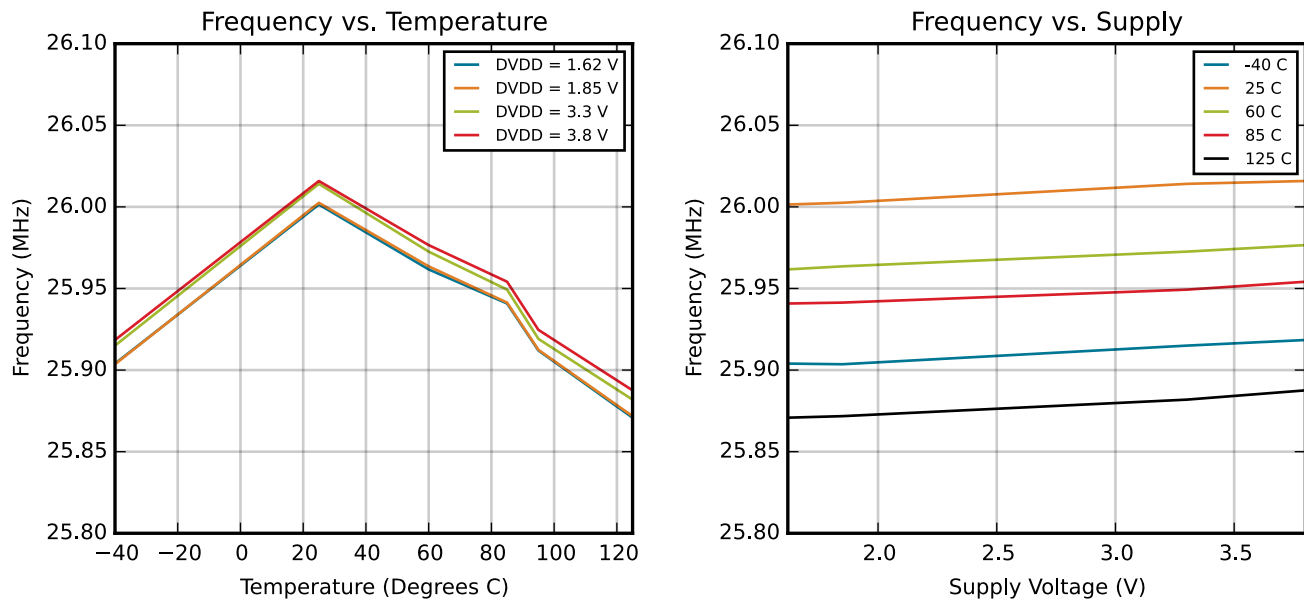


Figure 4.10. HFCO and AUXHFCO Typical Performance at 26 MHz

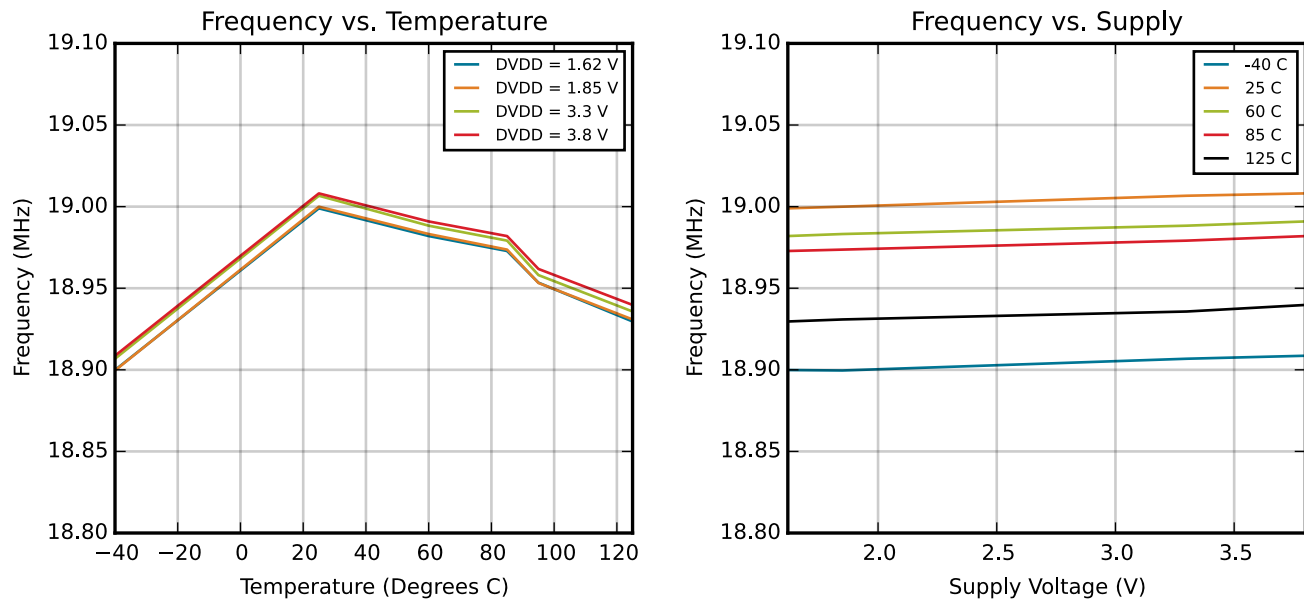


Figure 4.11. HFCO and AUXHFCO Typical Performance at 19 MHz

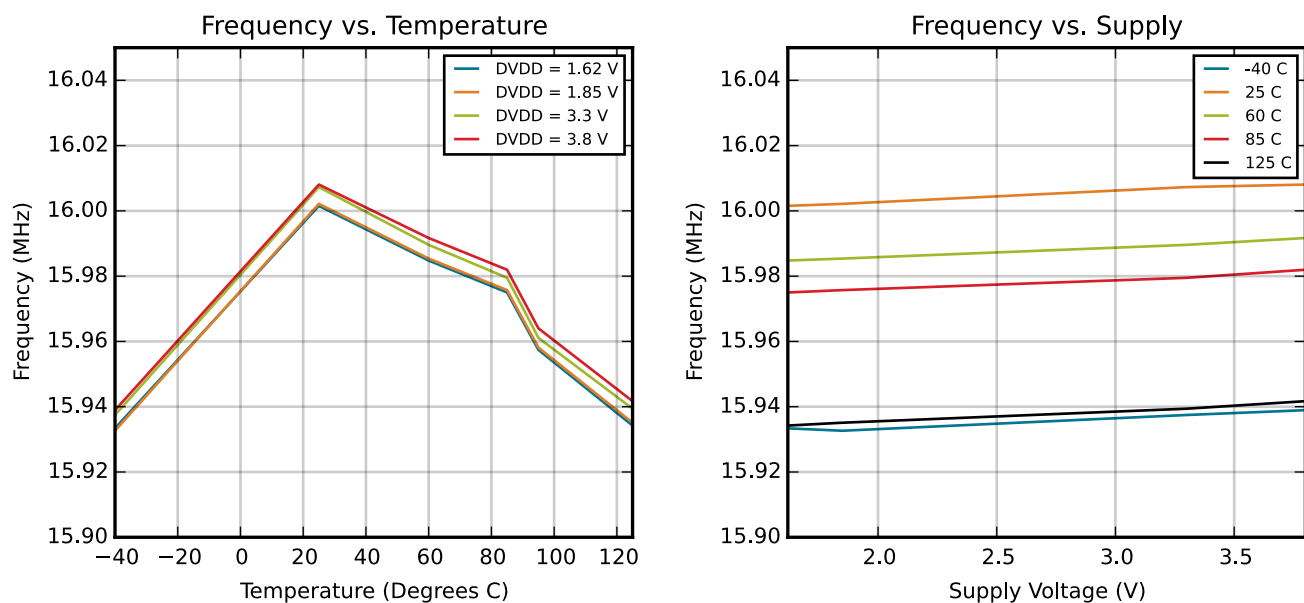


Figure 4.12. HFCO and AUXHFCO Typical Performance at 16 MHz

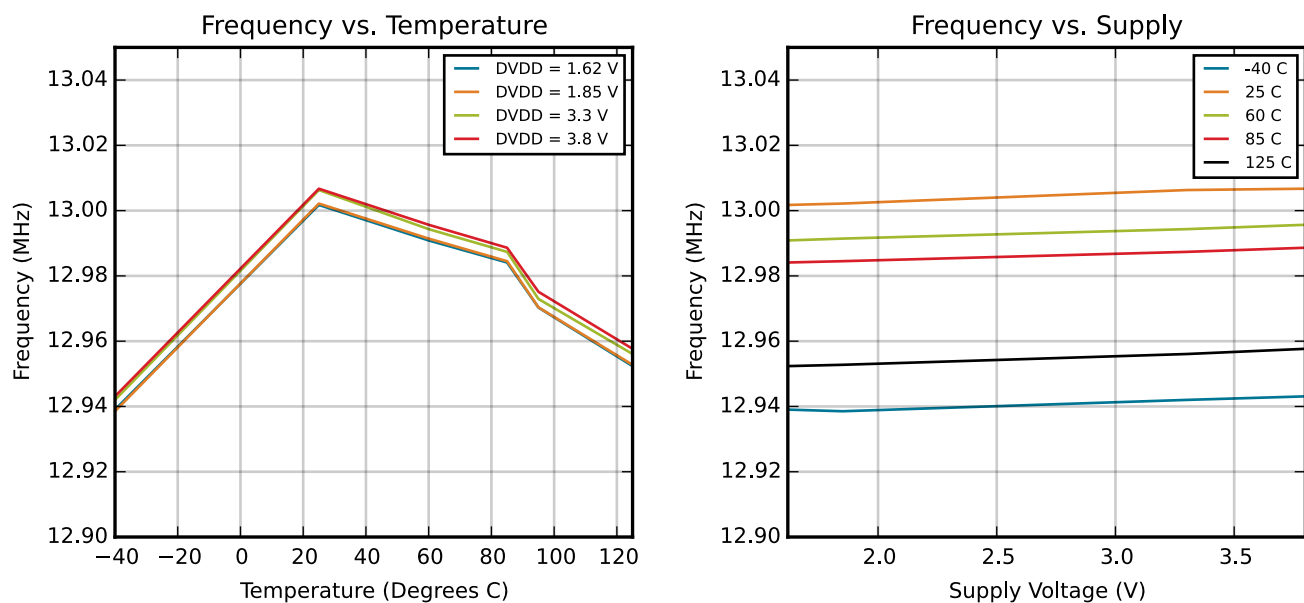


Figure 4.13. HFCO and AUXHFCO Typical Performance at 13 MHz

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
20	PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE- TIM0_OUT0 #19 LE- TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19
21	PD12	BUSCX BUSDY	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE- TIM0_OUT0 #20 LE- TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20
22	PD13	BUSCY BUSDX	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE- TIM0_OUT0 #21 LE- TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21
23	PD14	BUSCX BUSDY	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
28	PA3	BUSCY BUSDX	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 LE- TIM0_OUT0 #3 LE- TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 GPIO_EM4WU8
29	PA4	BUSCX BUSDY	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 LE- TIM0_OUT0 #4 LE- TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4
30	PA5	BUSCY BUSDX	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 LE- TIM0_OUT0 #5 LE- TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5
31	PB11	BUSCY BUSDX	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE- TIM0_OUT0 #6 LE- TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6

6.1.1 EFM32JG1 QFN48 with DC-DC GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), and the individual pins on each port are indicated by a number from 15 down to 0.

Table 6.2. QFN48 with DC-DC GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	PA5 (5V)	PA4 (5V)	PA3 (5V)	PA2 (5V)	PA1	PA0
Port B	PB15	PB14	PB13 (5V)	PB12 (5V)	PB11 (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	PC9 (5V)	PC8 (5V)	PC7 (5V)	PC6 (5V)	-	-	-	-	-	-
Port D	PD15 (5V)	PD14 (5V)	PD13 (5V)	PD12 (5V)	PD11 (5V)	PD10 (5V)	PD9 (5V)	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	PF7 (5V)	PF6 (5V)	PF5 (5V)	PF4 (5V)	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PA4, PA3, PA2, PB13, PB12, PB11, PD15, PD14, and PD13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Table 6.3. QFN32 without DC-DC Device Pinout

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VREGVSS	Voltage regulator VSS			
1	PF0	BUSAX BUSBY	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0 BOOT_TX
2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0 BOOT_RX
3	PF2	BUSAX BUSBY	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0

6.3 EFM32JG1 QFN32 with DC-DC Definition

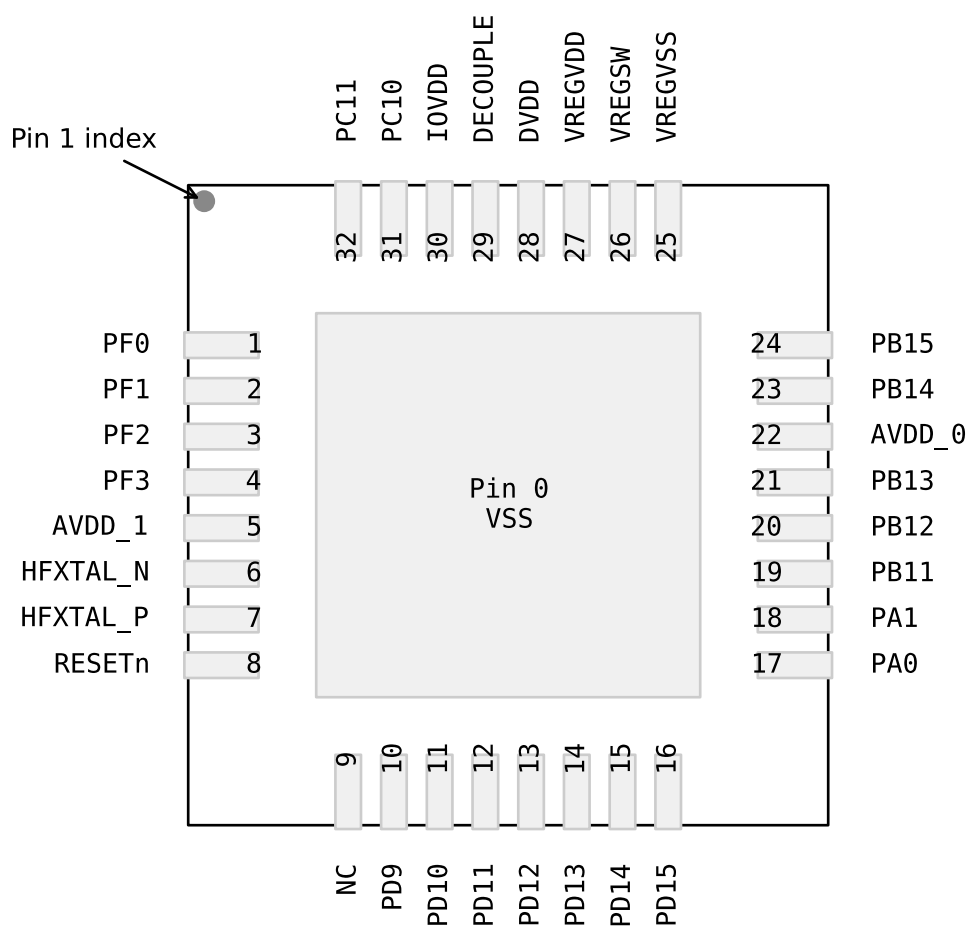


Figure 6.3. EFM32JG1 QFN32 with DC-DC Pinout

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
12	PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE- TIM0_OUT0 #19 LE- TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19
13	PD12	BUSCX BUSDY	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE- TIM0_OUT0 #20 LE- TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20
14	PD13	BUSCY BUSDX	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE- TIM0_OUT0 #21 LE- TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21
15	PD14	BUSCX BUSDY	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
25	VREGVSS	Voltage regulator VSS			
26	VREGSW	DCDC regulator switching node			
27	VREGVDD	Voltage regulator VDD input			
28	DVDD	Digital power supply .			
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.			
30	IOVDD	Digital IO power supply .			
31	PC10	BUSAX BUSBY	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LE- TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
32	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

7. QFN48 Package Specifications

7.1 QFN48 Package Dimensions

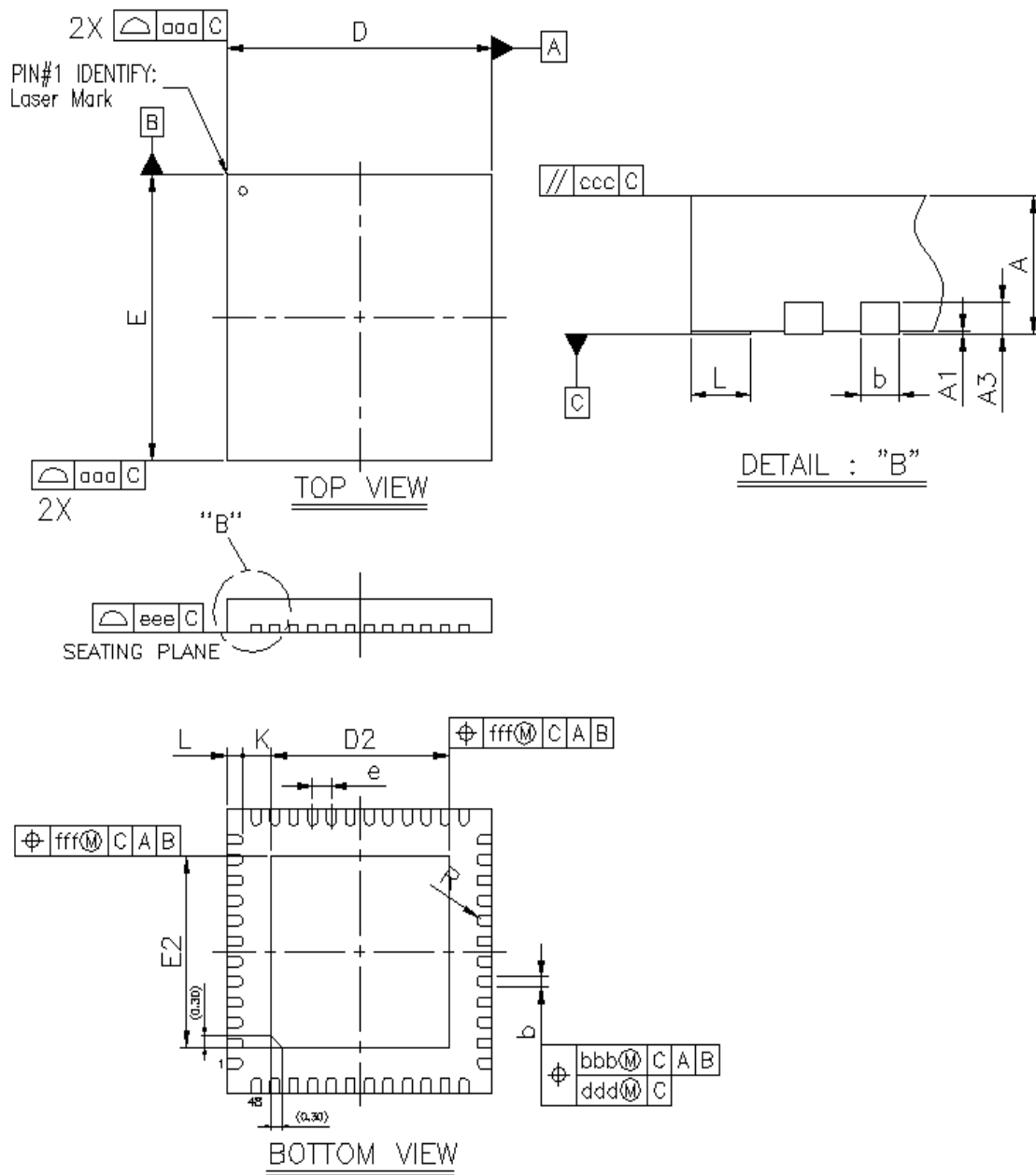


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