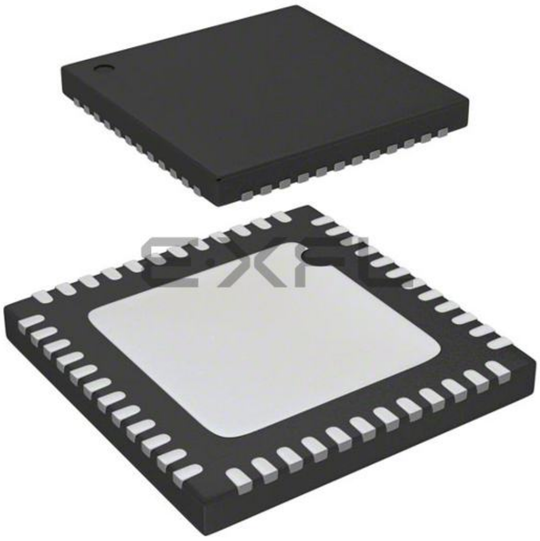
Silicon Labs - EFM32JG1B200F128GM48-B0R Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32jg1b200f128gm48-b0r

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be the highest voltage in the system
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_{OP}	-G temperature grade, Ambient Temperature	-40	25	85	°C
		-I temperature grade, Junction Temperature	-40	25	125	°C
AVDD Supply voltage[1]	V_{AVDD}		1.85	3.3	3.8	V
VREGVDD Operating supply voltage[1] [2]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.85	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.85	3.3	3.8	V
VREGVDD Current	$I_{VREGVDD}$	DCDC in bypass, $T_{amb} \le 85$ °C	—	—	200	mA
		DCDC in bypass, $T_{amb} > 85$ °C	—	—	100	mA
DVDD Operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD Operating supply voltage	V_{IOVDD}		1.62	—	$V_{VREGVDD}$	V
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)	dV_{DD}		—	—	0.1	V
HFCLK frequency	f_{CORE}	0 wait-states (MODE = WS0) [3]	—	—	26	MHz
		1 wait-states (MODE = WS1) [3]	—	—	40	MHz

Note:

1. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
2. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$
3. In MSC_READCTRL register

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	$THETA_{JA}$	QFN32 Package, 2-Layer PCB, Air velocity = 0 m/s	—	79	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 1 m/s	—	62.2	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 2 m/s	—	54.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 0 m/s	—	32	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 1 m/s	—	28.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 2 m/s	—	26.9	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 0 m/s	—	64.5	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 1 m/s	—	51.6	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 2 m/s	—	47.7	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 0 m/s	—	26.2	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 1 m/s	—	23.1	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 2 m/s	—	22.1	—	°C/W

4.1.8.2 HFXO

Table 4.11. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{HFXO}		38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 38.4 MHz	—	—	60	Ω
Supported range of crystal load capacitance [1]	C_{HFXO_CL}		6	—	12	pF
On-chip tuning cap range [2]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	9	20	25	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.04	—	pF
Startup time	t_{HFXO}	38.4 MHz, ESR = 50 Ω, C_L = 10 pF	—	300	—	µs
Frequency Tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ω, CL = 10 pF	-40	—	40	ppm

Note:

1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.1.8.3 LFRCO

Table 4.12. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL, $T_{AMB} \leq 85$ °C	30.474	32.768	34.243	kHz
		ENVREF = 1 in CMU_LFRCOCTRL, $T_{AMB} > 85$ °C	30.474	—	39.7	kHz
		ENVREF = 0 in CMU_LFRCOCTRL	30.474	32.768	33.915	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:

1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register

4.1.8.4 HFRCO and AUXHFRCO

Table 4.13. HFRCO and AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	f_{HFRCO_ACC}	Any frequency band, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	μs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	μs
Current consumption on all supplies	I_{HFRCO}	$f_{HFRCO} = 38$ MHz	—	204	228	μA
		$f_{HFRCO} = 32$ MHz	—	171	190	μA
		$f_{HFRCO} = 26$ MHz	—	147	164	μA
		$f_{HFRCO} = 19$ MHz	—	126	138	μA
		$f_{HFRCO} = 16$ MHz	—	110	120	μA
		$f_{HFRCO} = 13$ MHz	—	100	110	μA
		$f_{HFRCO} = 7$ MHz	—	81	91	μA
		$f_{HFRCO} = 4$ MHz	—	33	35	μA
		$f_{HFRCO} = 2$ MHz	—	31	35	μA
		$f_{HFRCO} = 1$ MHz	—	30	35	μA
Step size	SS_{HFRCO}	Coarse (% of period)	—	0.8	—	%
		Fine (% of period)	—	0.1	—	%
Period Jitter	PJ_{HFRCO}		—	0.2	—	% RMS

4.1.8.5 ULFRCO

Table 4.14. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		0.95	1	1.07	kHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	102	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	17	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	162	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	123	—	μA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	140	—	μA
ADC Clock Frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[4]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[2] = NORMAL	—	—	5	μs
		WARMUPMODE[2] = KEEPINSTANDBY	—	—	2	μs
		WARMUPMODE[2] = KEEPINSLOWACC	—	—	1	μs
SNDR at 1Msps and f_{in} = 10kHz	$SNDR_{ADC}$	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	58	67	—	dB
		vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Input referred ADC noise, rms	V_{REF_NOISE}	Including quantization noise and distortion	—	380	—	μV
Offset Error	$V_{ADCOFFSETERR}$		-3	0.25	3	LSB
Gain error in ADC	V_{ADC_GAIN}	Using internal reference	—	-0.2	5	%
		Using external reference	—	-1	—	%
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No Missing Codes	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	-6	—	6	LSB
Temperature Sensor Slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

4.1.13 IDAC

Table 4.19. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of Ranges	N_{IDAC_RANGES}		—	4	—	-
Output Current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	μA
		RANGSEL[1] = RANGE1	1.6	—	4.7	μA
		RANGSEL[1] = RANGE2	0.5	—	16	μA
		RANGSEL[1] = RANGE3	2	—	64	μA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	μA
Total Accuracy, STEPSEL[1] = 0x10	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	-2	—	2	%
		EM0 or EM1	-18	—	22	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	μs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value)	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption in EM0 or EM1 [2]	I_{IDAC}	Source mode, excluding output current	—	8.9	13	µA
		Sink mode, excluding output current	—	12	16	µA
Current consumption in EM2 or EM3[2]		Source mode, excluding output current, duty cycle mode, T = 25 °C	—	1.04	—	µA
		Sink mode, excluding output current, duty cycle mode, T = 25 °C	—	1.08	—	µA
		Source mode, excluding output current, duty cycle mode, T ≥ 85 °C	—	8.9	—	µA
		Sink mode, excluding output current, duty cycle mode, T ≥ 85 °C	—	12	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.04	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.02	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.02	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.02	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.18	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.08	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.02	—	%

Note:

1. In IDAC_CURPROG register
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.15 I2C

I2C Standard-mode (Sm)

Table 4.21. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	$t_{SU,DAT}$		250	—	—	ns
SDA hold time[3]	$t_{HD,DAT}$		100	—	3450	ns
Repeated START condition set-up time	$t_{SU,STA}$		4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		4	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

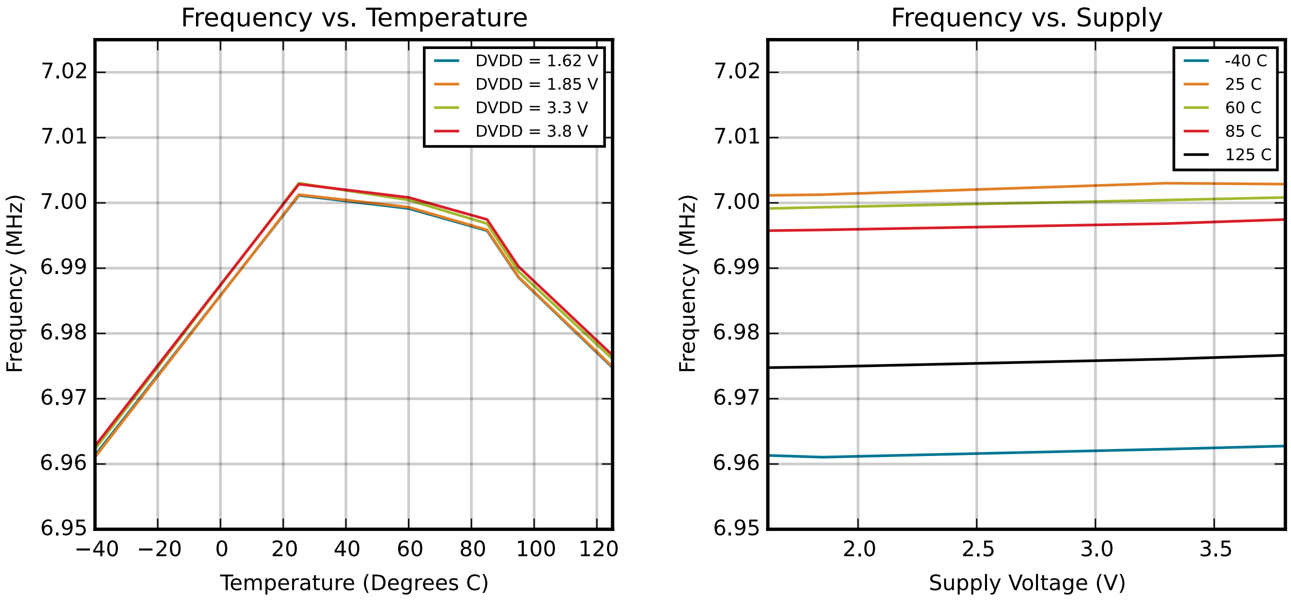

Figure 4.14. HFRCO and AUXHFRCO Typical Performance at 7 MHz

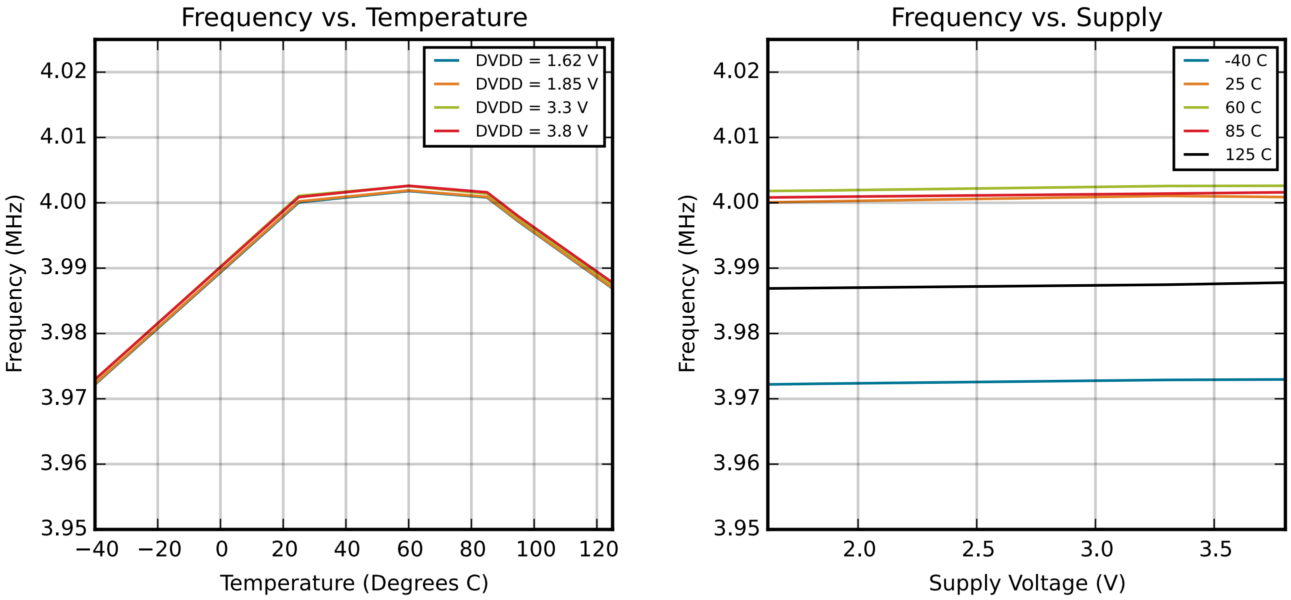

Figure 4.15. HFRCO and AUXHFRCO Typical Performance at 4 MHz

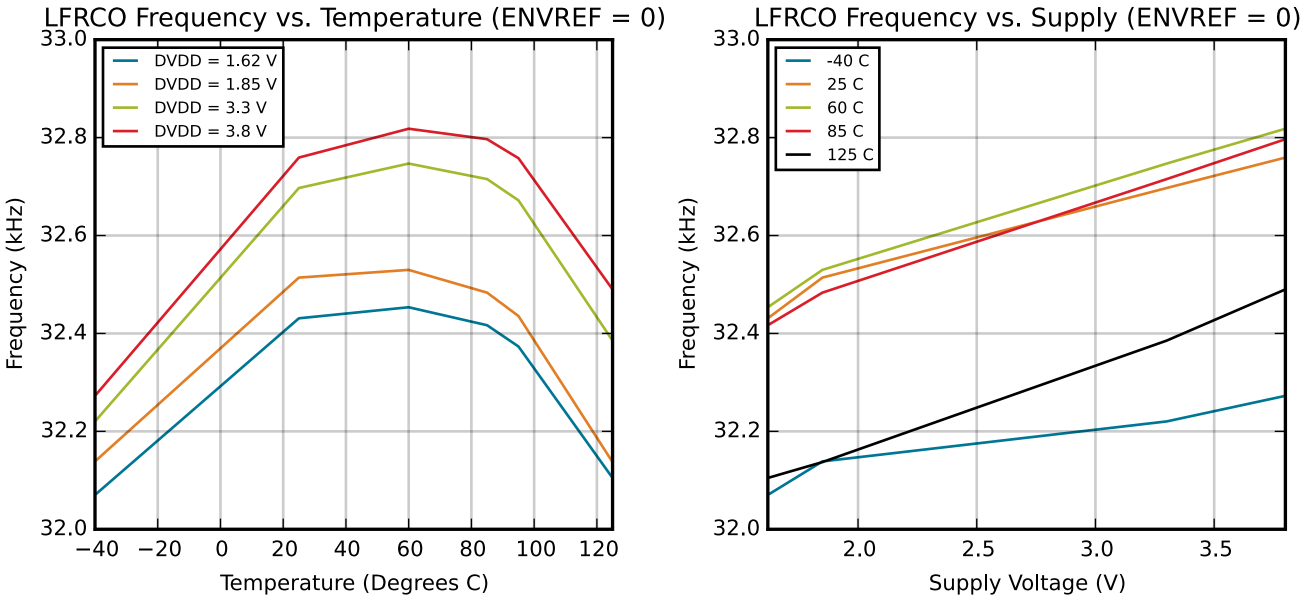

Figure 4.18. LFRCO Typical Performance at 32.768 kHz

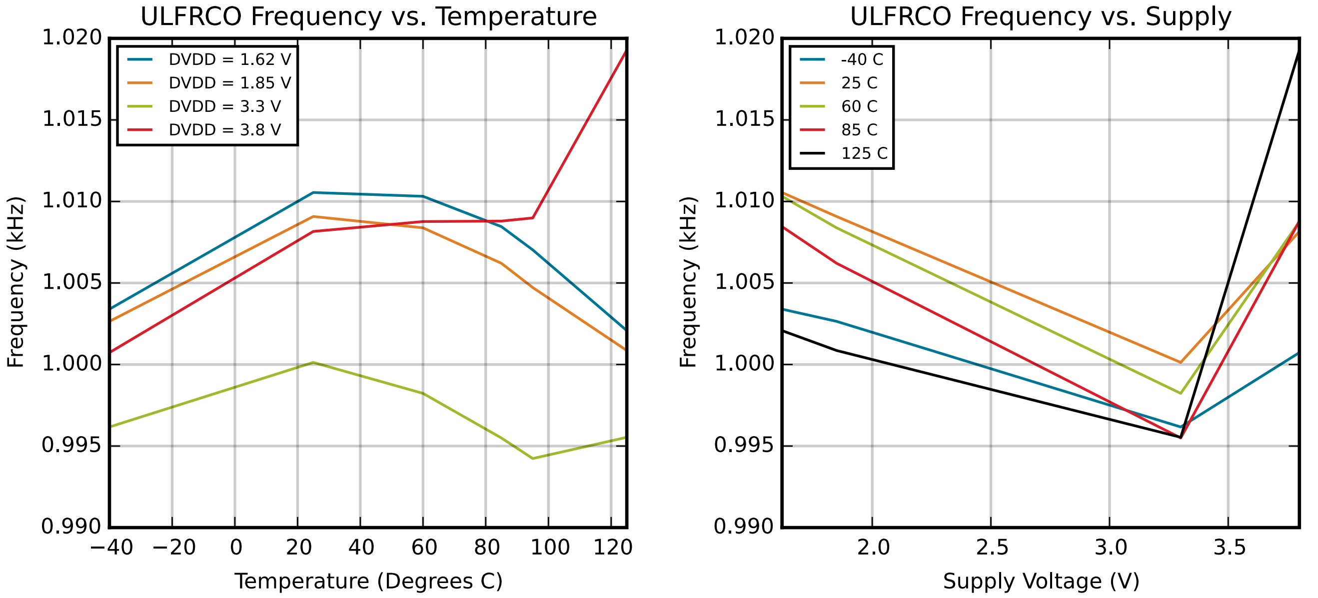

Figure 4.19. ULFRCO Typical Performance at 1 kHz

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal dc-dc converter, are shown in Figure 5.1 EFM32JG1 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 48.

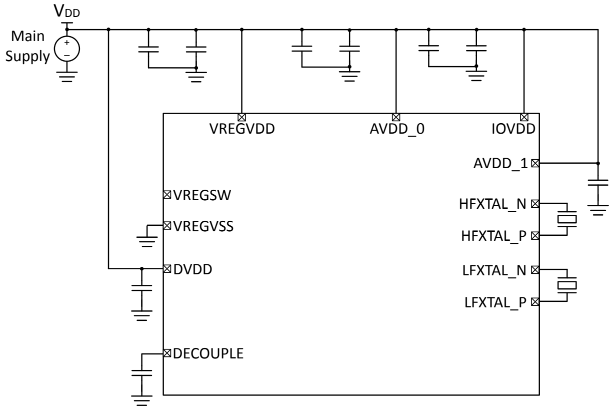

Figure 5.1. EFM32JG1 Typical Application Circuit, Direct Supply, No DC-DC Converter

A typical application circuit using the internal dc-dc converter is shown in Figure 5.2 EFM32JG1 Typical Application Circuit Using the DC-DC Converter on page 48. The MCU operates from the dc-dc converter supply.

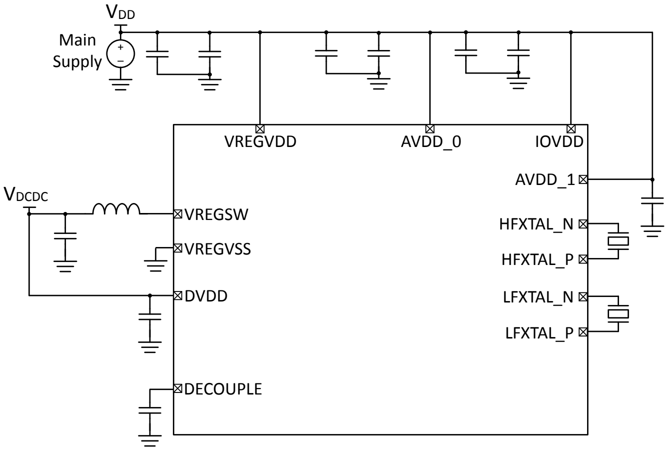

Figure 5.2. EFM32JG1 Typical Application Circuit Using the DC-DC Converter

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

Table 6.1. QFN48 with DC-DC Device Pinout

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	RFVSS	Radio Ground			
1	PF0	BUSAX BUSBY	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE-TIM0_OUT0 #24 LE-TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0 BOOT_TX
2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE-TIM0_OUT0 #25 LE-TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0 BOOT_RX
3	PF2	BUSAX BUSBY	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE-TIM0_OUT0 #26 LE-TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
37	VREGVSS	Voltage regulator VSS			
38	VREGSW	DCDC regulator switching node			
39	VREGVDD	Voltage regulator VDD input			
40	DVDD	Digital power supply .			
41	DECOUPLE	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.			
42	IOVDD	Digital IO power supply .			
43	PC6	BUSAX BUSBY	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 LETIM0_OUT0 #11 LETIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	CMU_CLK0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11
44	PC7	BUSAY BUSBX	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LETIM0_OUT0 #12 LETIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12
45	PC8	BUSAX BUSBY	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LETIM0_OUT0 #13 LETIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
4	PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE-TIM0_OUT0 #27 LE-TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
5	PF4	BUSAX BUSBY	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE-TIM0_OUT0 #28 LE-TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28
6	AVDD	Analog power supply .			
7	HFXTAL_N	High Frequency Crystal input pin.			
8	HFXTAL_P	High Frequency Crystal output pin.			
9	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
10	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LE-TIM0_OUT0 #17 LE-TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17

6.2.1 EFM32JG1 QFN32 without DC-DC GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), and the individual pins on each port are indicated by a number from 15 down to 0.

Table 6.4. QFN32 without DC-DC GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA1	PA0
Port B	PB15	PB14	PB13 (5V)	PB12 (5V)	PB11 (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	PC9 (5V)	PC8 (5V)	PC7 (5V)	-	-	-	-	-	-	-
Port D	PD15 (5V)	PD14 (5V)	PD13 (5V)	PD12 (5V)	PD11 (5V)	PD10 (5V)	PD9 (5V)	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	PF4 (5V)	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PB13, PB12, PB11, PD15, PD14, and PD13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
4	PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LETIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
5	AVDD	Analog power supply .			
6	HFXTAL_N	High Frequency Crystal input pin.			
7	HFXTAL_P	High Frequency Crystal output pin.			
8	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
9	NC	No Connect.			
10	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LETIM0_OUT0 #17 LETIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17
11	PD10	BUSCX BUSDY	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LETIM0_OUT0 #18 LETIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18

6.4 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.7. Alternate functionality overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin
BOOT_RX	0: PF1								Bootloader RX
BOOT_TX	0: PF0								Bootloader TX
CMU_CLK0	0: PA1 1: PB15 2: PC6 3: PC11	4: PD9 5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 1: PB14 2: PC7 3: PC10	4: PD10 5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.

7.3 QFN48 Package Marking

Figure 7.3. QFN48 Package Marking

The package marking consists of:

- PPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – Reserved for future use. Current value is 0.

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