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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18f2320-e-so">https://www.e-xfl.com/product-detail/microchip-technology/pic18f2320-e-so</a>

# PIC18F2220/2320/4220/4320

## REGISTER 2-3: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R <sup>(1)</sup>	R-0	R/W-0	R/W-0
IDLEN	IRCF2	IRCF1	IRCF0	OSTS	IOFS	SCS1	SCS0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7      **IDLEN:** Idle Enable bit  
             1 = Idle mode enabled; CPU core is not clocked in power-managed modes  
             0 = Run mode enabled; CPU core is clocked in power-managed modes
- bit 6-4    **IRCF2:IRCF0:** Internal Oscillator Frequency Select bits  
             111 = 8 MHz (8 MHz source drives clock directly)  
             110 = 4 MHz  
             101 = 2 MHz  
             100 = 1 MHz  
             011 = 500 kHz  
             010 = 250 kHz  
             001 = 125 kHz  
             000 = 31 kHz (INTRC source drives clock directly)
- bit 3      **OSTS:** Oscillator Start-up Time-out Status bit<sup>(1)</sup>  
             1 = Oscillator Start-up Timer time-out has expired; primary oscillator is running  
             0 = Oscillator Start-up Timer time-out is running; primary oscillator is not ready
- bit 2      **IOFS:** INTOSC Frequency Stable bit  
             1 = INTOSC frequency is stable  
             0 = INTOSC frequency is not stable
- bit 1-0    **SCS1:SCS0:** System Clock Select bits  
             1x = Internal oscillator block (RC modes)  
             01 = Timer1 oscillator (Secondary modes)<sup>(2)</sup>  
             00 = Primary oscillator (Sleep and PRI\_IDLE modes)

**Note 1:** Depends on state of IESO bit in Configuration Register 1H.

**2:** SCS0 may not be set while T1OSCEN (T1CON<3>) is clear.

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## 5.9.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 5-1 and Table 5-2.

The SFRs can be classified into two sets: those associated with the “core” function and those related to the peripheral functions. Those registers related to the

“core” are described in this section, while those related to the operation of the peripheral features are described in the section of that peripheral feature.

The SFRs are typically distributed among the peripherals whose functions they control.

The unused SFR locations will be unimplemented and read as ‘0’s.

**TABLE 5-1: SPECIAL FUNCTION REGISTER MAP FOR PIC18F2X20/4X20 DEVICES**

Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2 <sup>(2)</sup>	FBFh	CCPR1H	F9Fh	IPR1
FFEh	TOSH	FDEh	POSTINC2 <sup>(2)</sup>	FBEh	CCPR1L	F9Eh	PIR1
FFDh	TOSL	FDDh	POSTDEC2 <sup>(2)</sup>	FBDh	CCP1CON	F9Dh	PIE1
FFCh	STKPTR	FDCh	PREINC2 <sup>(2)</sup>	FBCh	CCPR2H	F9Ch	—
FFBh	PCLATU	FDBh	PLUSW2 <sup>(2)</sup>	FBHh	CCPR2L	F9Bh	OSCTUNE
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	OSCTUN2
FF9h	PCL	FD9h	FSR2L	FB9h	—	F99h	—
FF8h	TBLPTRU	FD8h	STATUS	FB8h	—	F98h	—
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	PWM1CON <sup>(1)</sup>	F97h	—
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	ECCPAS <sup>(1)</sup>	F96h	TRISE <sup>(1)</sup>
FF5h	TABLAT	FD5h	T0CON	FB5h	CVRCON	F95h	TRISD <sup>(1)</sup>
FF4h	PRODH	FD4h	—	FB4h	CMCON	F94h	TRISC
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB
FF2h	INTCON	FD2h	LVDCON	FB2h	TMR3L	F92h	TRISA
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	—
FF0h	INTCON3	FD0h	RCON	FB0h	—	F90h	—
FEFh	INDF0 <sup>(2)</sup>	FCFh	TMR1H	FAFh	SPBRG	F8Fh	—
FEeh	POSTINC0 <sup>(2)</sup>	FCEh	TMR1L	FAEh	RCREG	F8Eh	—
FEDh	POSTDEC0 <sup>(2)</sup>	FCDh	T1CON	FADh	TXREG	F8Dh	LATE <sup>(1)</sup>
FECh	PREINC0 <sup>(2)</sup>	FCCh	TMR2	FACH	TXSTA	F8Ch	LATD <sup>(1)</sup>
FEbh	PLUSW0 <sup>(2)</sup>	FCBh	PR2	FABh	RCSTA	F8Bh	LATC
FEAh	FSR0H	FCAh	T2CON	FAAh	—	F8Ah	LATB
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA
FE8h	WREG	FC8h	SSPADDD	FA8h	EEDATA	F88h	—
FE7h	INDF1 <sup>(2)</sup>	FC7h	SSPSTAT	FA7h	EECON2	F87h	—
FE6h	POSTINC1 <sup>(2)</sup>	FC6h	SSPCON1	FA6h	EECON1	F86h	—
FE5h	POSTDEC1 <sup>(2)</sup>	FC5h	SSPCON2	FA5h	—	F85h	—
FE4h	PREINC1 <sup>(2)</sup>	FC4h	ADRESH	FA4h	—	F84h	PORTE <sup>(1)</sup>
FE3h	PLUSW1 <sup>(2)</sup>	FC3h	ADRESL	FA3h	—	F83h	PORTD <sup>(1)</sup>
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA

**Legend:** — = Unimplemented registers, read as ‘0’.

**Note 1:** This register is not available on PIC18F2X20 devices.

**2:** This is not a physical register.

## 7.0 DATA EEPROM MEMORY

The data EEPROM is readable and writable during normal operation over the entire VDD range. The data memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (SFR).

There are four SFRs used to read and write the program and data EEPROM memory. These registers are:

- EECON1
- EECON2
- EEDATA
- EEADR

The EEPROM data memory allows byte read and write. When interfacing to the data memory block, EEDATA holds the 8-bit data for read/write and EEADR holds the address of the EEPROM location being accessed. These devices have 256 bytes of data EEPROM with an address range from 00h to FFh.

The EEPROM data memory is rated for high erase/write cycle endurance. A byte write automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature, as well as from chip to chip. Please refer to parameter D122 (Table 26-1 in **Section 26.0 “Electrical Characteristics”**) for exact limits.

### 7.1 EEADR

The address register can address 256 bytes of data EEPROM.

### 7.2 EECON1 and EECON2 Registers

EECON1 is the control register for memory accesses.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the memory write and erase sequences.

Control bit EEPGD determines if the access will be to program or data EEPROM memory. When clear, operations will access the data EEPROM memory. When set, program memory is accessed.

Control bit, CFGS, determines if the access will be to the Configuration registers or to program memory/data EEPROM memory. When set, subsequent operations access Configuration registers. When CFGS is clear, the EEPGD bit selects either Flash program or data EEPROM memory.

The WREN bit enables and disables erase and write operations. When set, erase and write operations are allowed. When clear, erase and write operations are disabled; the WR bit cannot be set while the WREN bit is clear. This mechanism helps to prevent accidental writes to memory due to errant (unexpected) code execution.

Firmware should keep the WREN bit clear at all times except when starting erase or write operations. Once firmware has set the WR bit, the WREN bit may be cleared. Clearing the WREN bit will not affect the operation in progress.

The WRERR bit is set when a write operation is interrupted by a Reset. In these situations, the user can check the WRERR bit and rewrite the location. It is necessary to reload the data and address registers (EEDATA and EEADR), as these registers have cleared as a result of the Reset.

Control bits, RD and WR, start read and erase/write operations, respectively. These bits are set by firmware and cleared by hardware at the completion of the operation.

The RD bit cannot be set when accessing program memory (EEPGD = 1). Program memory is read using table read instructions. See **Section 6.1 “Table Reads and Table Writes”** regarding table reads.

<b>Note:</b> Interrupt flag bit, EEIF in the PIR2 register, is set when write is complete. It must be cleared in software.
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## 16.0 ENHANCED CAPTURE/COMPARE/PWM (ECCP) MODULE

**Note:** The ECCP (Enhanced Capture/ Compare/ PWM) module is only available on PIC18F4X20 devices.

In 40 and 44-pin devices, the CCP1 module is implemented as a standard CCP module with enhanced PWM capabilities. Operation of the Capture, Compare and standard single output PWM modes is described in **Section 15.0 “Capture/Compare/PWM (CCP) Modules”**. Discussion in that section relating to PWM frequency and duty cycle also apply to the enhanced PWM mode.

The ECCP module differs from the CCP with the addition of an enhanced PWM mode which allows for 2 or 4 output channels, user-selectable polarity, dead band control and automatic shutdown and restart. These features are discussed in detail in **Section 16.4 “Enhanced PWM Mode”**.

The control register for CCP1 is shown in Register 16-1. It differs from the CCP1CON register of PIC18F2X20 devices in that the two Most Significant bits are implemented to control enhanced PWM functionality.

**REGISTER 16-1: CCP1CON: ECCP CONTROL REGISTER (40/44-PIN DEVICES)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

-n = Value at POR

‘1’ = Bit is set

‘0’ = Bit is cleared

x = Bit is unknown

bit 7-6

**P1M1:P1M0:** PWM Output Configuration bits

If CCP1M3:CCP1M2 = 00, 01, 10 (Capture, Compare or disabled):

xx = P1A assigned as Capture/Compare input; P1B, P1C, P1D assigned as port pins

If CCP1M3:CCP1M2 = 11 (PWM modes):

00 = Single output: P1A modulated; P1B, P1C, P1D assigned as port pins

01 = Full-bridge output forward: P1D modulated; P1A active; P1B, P1C inactive

10 = Half-bridge output: P1A, P1B modulated with dead-band control; P1C, P1D assigned as port pins

11 = Full-bridge output reverse: P1B modulated; P1C active; P1A, P1D inactive

bit 5-4

**DC1B1:DC1B0:** PWM Duty Cycle Least Significant bits

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSBs of the 10-bit PWM duty cycle. The eight MSBs of the duty cycle are found in CCPR1L.

## 17.4.6 MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON1 and by setting the SSPEN bit. In Master mode, the SCL and SDA lines are manipulated by the MSSP hardware.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I<sup>2</sup>C bus may be taken when the P bit is set or the bus is Idle, with both the S and P bits clear.

In Firmware Controlled Master mode, user code conducts all I<sup>2</sup>C bus operations based on Start and Stop bit conditions.

Once Master mode is enabled, the user has six options.

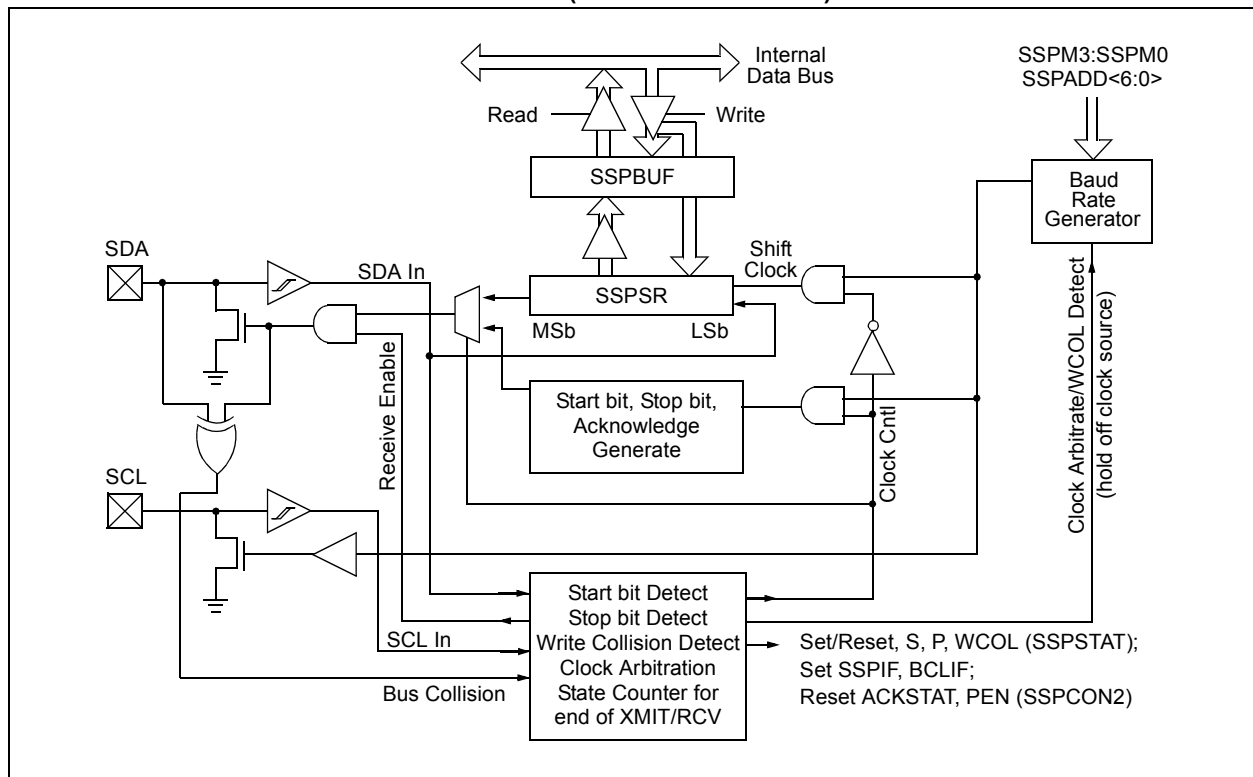
1. Assert a Start condition on SDA and SCL.
2. Assert a Repeated Start condition on SDA and SCL.
3. Write to the SSPBUF register initiating transmission of data/address.
4. Configure the I<sup>2</sup>C port to receive data.
5. Generate an Acknowledge condition at the end of a received byte of data.
6. Generate a Stop condition on SDA and SCL.

**Note:** The MSSP module, when configured in I<sup>2</sup>C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPBUF register to initiate transmission before the Start condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

The following events will cause MSSP Interrupt Flag bit, SSPIF, to be set (MSSP interrupt if enabled):

- Start Condition
- Stop Condition
- Data Transfer Byte Transmitted/Received
- Acknowledge Transmit
- Repeated Start

**FIGURE 17-16: MSSP BLOCK DIAGRAM (I<sup>2</sup>C MASTER MODE)**



## 17.4.8 I<sup>2</sup>C MASTER MODE START CONDITION TIMING

To initiate a Start condition, the user sets the Start Condition Enable bit, SEN (SSPCON2<0>). If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the Start condition and causes the S bit (SSPSTAT<3>) to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit (SSPCON2<0>) will be automatically cleared by hardware, the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

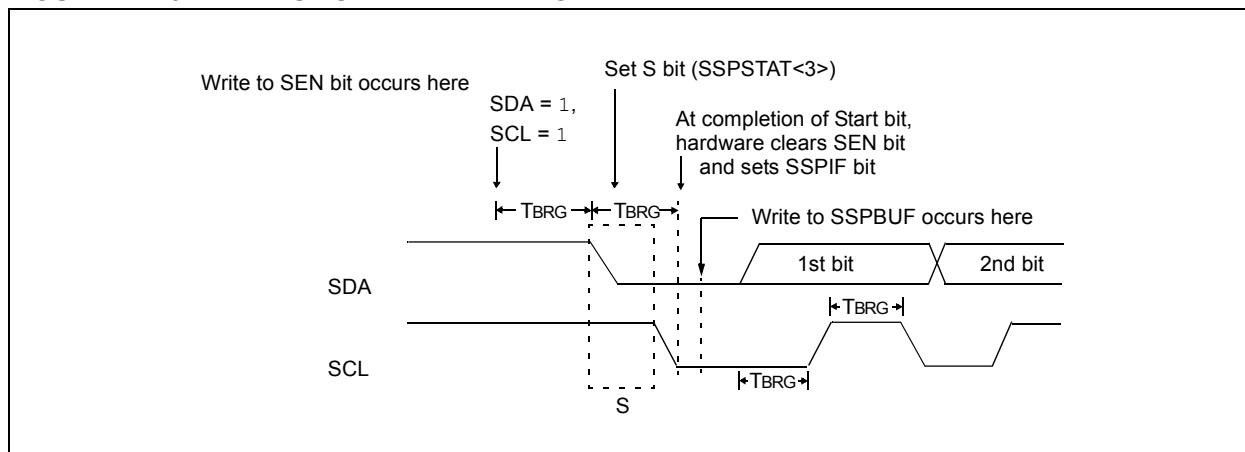
**Note:** If, at the beginning of the Start condition, the SDA and SCL pins are already sampled low or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLIF, is set, the Start condition is aborted and the I<sup>2</sup>C module is reset into its Idle state.

### 17.4.8.1 WCOL Status Flag

If the user writes the SSPBUF when a Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

**Note:** Because queueing of events is not allowed, writing to the lower 5 bits of SSPCON2 is disabled until the Start condition is complete.

**FIGURE 17-19: FIRST START BIT TIMING**



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## 18.2 USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit Baud Rate Generator. The SPBRG register controls the period of a free-running 8-bit timer. In Asynchronous mode, bit BRGH (TXSTA<2>) also controls the baud rate. In Synchronous mode, bit BRGH is ignored. Table 18-1 shows the formula for computation of the baud rate for different USART modes which only apply in Master mode (internal clock).

Given the desired baud rate and FOSC, the nearest integer value for the SPBRG register can be calculated using the formula in Table 18-1. From this, the error in baud rate can be determined.

Example 18-1 shows the calculation of the baud rate error for the following conditions:

- FOSC = 16 MHz
- Desired Baud Rate = 9600
- BRGH = 0
- SYNC = 0

It may be advantageous to use the high baud rate (BRGH = 1), even for slower baud clocks, because the  $F_{OSC}/(16(X + 1))$  equation can reduce the baud rate error in some cases.

Writing a new value to the SPBRG register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

### 18.2.1 POWER-MANAGED MODE OPERATION

The system clock is used to generate the desired baud rate; however, when a power-managed mode is entered, the clock source may be operating at a different frequency than in PRI\_RUN mode. In Sleep mode, no clocks are present and in PRI\_IDLE, the primary clock source continues to provide clocks to the baud rate generator; however, in other power-managed modes, the clock frequency will probably change. This may require the value in SPBRG to be adjusted.

### 18.2.2 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin.

### EXAMPLE 18-1: CALCULATING BAUD RATE ERROR

Desired Baud Rate	=	$F_{OSC}/(64(X + 1))$
Solving for X:		
X	=	$((F_{OSC}/\text{Desired Baud Rate})/64) - 1$
X	=	$((16000000/9600)/64) - 1$
X	=	$[25.042] = 25$
Calculated Baud Rate	=	$16000000/(64(25 + 1))$
	=	9615
Error	=	(Calculated Baud Rate – Desired Baud Rate)
Desired Baud Rate		
	=	$(9615 - 9600)/9600$
	=	0.16%

TABLE 18-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0 (Asynchronous)	Baud Rate = $F_{OSC}/(64(X + 1))$	Baud Rate = $F_{OSC}/(16(X + 1))$
1 (Synchronous)	Baud Rate = $F_{OSC}/(4(X + 1))$	N/A

**Legend:** X = value in SPBRG (0 to 255)

TABLE 18-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

**Legend:** x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.



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**TABLE 18-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1, HIGH SPEED)**

BAUD RATE (K)	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 16.000 MHz			Fosc = 10.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
2.4	—	—	—	4.88	103.45	255	3.91	62.76	255	2.44	1.73	255
9.6	9.77	1.73	255	9.62	0.16	129	9.62	0.16	103	9.63	0.16	64
19.2	19.23	0.16	129	19.23	0.16	64	19.23	0.16	51	18.94	-1.36	32
38.4	38.46	0.16	64	37.88	-1.36	32	38.46	0.16	25	39.06	1.73	15
57.6	58.14	0.94	42	56.82	-1.36	21	58.82	2.12	16	56.82	-1.36	10
76.8	75.76	-1.36	32	78.13	1.73	15	76.92	0.16	12	78.13	1.73	7
96.0	96.15	0.16	25	96.15	0.16	12	100.00	4.17	9	89.29	-6.99	6
115.2	113.64	-1.36	21	113.64	-1.36	10	111.11	-3.55	8	125.00	8.51	4
250.0	250.00	0.00	9	250.00	0.00	4	250.00	0.00	3	208.33	-16.67	2
300.0	312.50	4.17	7	312.50	4.17	3	333.33	11.11	2	312.50	4.17	1
500.0	500.00	0.00	4	416.67	-16.67	2	500.00	0.00	1	—	—	—
625.0	625.00	0.00	3	625.00	0.00	1	—	—	—	625.00	0.00	0
1000.0	833.33	-16.67	2	—	—	—	1000.00	0.00	0	—	—	—
1250.0	1250.00	0.00	1	1250.00	0.00	0	—	—	—	—	—	—

BAUD RATE (K)	Fosc = 8.000000 MHz			Fosc = 7.159090 MHz			Fosc = 5.068800 MHz			Fosc = 4.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—	0.98	225.52	255
1.2	1.95	62.76	255	1.75	45.65	255	1.24	3.13	255	1.20	0.16	207
2.4	2.40	0.16	207	2.41	0.23	185	2.40	0.00	131	2.40	0.16	103
9.6	9.62	0.16	51	9.52	-0.83	46	9.60	0.00	32	9.62	0.16	25
19.2	19.23	0.16	25	19.45	1.32	22	18.64	-2.94	16	19.23	0.16	12
38.4	38.46	0.16	12	37.29	-2.90	11	39.60	3.13	7	35.71	-6.99	6
57.6	55.56	-3.55	8	55.93	-2.90	7	52.80	-8.33	5	62.50	8.51	3
76.8	71.43	-6.99	6	74.57	-2.90	5	79.20	3.13	3	83.33	8.51	2
96.0	100.00	4.17	4	89.49	-6.78	4	—	—	—	—	—	—
115.2	125.00	8.51	3	111.86	-2.90	3	105.60	-8.33	2	125.00	8.51	1
250.0	250.00	0.00	1	223.72	-10.51	1	—	—	—	250.00	0.00	0
300.0	—	—	—	—	—	—	316.80	5.60	0	—	—	—
500.0	500.00	0.00	0	447.44	-10.51	0	—	—	—	—	—	—

BAUD RATE (K)	Fosc = 3.579545 MHz			Fosc = 2.000000 MHz			Fosc = 1.000000 MHz			Fosc = 0.032768 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.87	191.30	255	0.49	62.76	255	0.30	0.16	207	0.29	-2.48	6
1.2	1.20	0.23	185	1.20	0.16	103	1.20	0.16	51	1.02	-14.67	1
2.4	2.41	0.23	92	2.40	0.16	51	2.40	0.16	25	2.05	-14.67	0
9.6	9.73	1.32	22	9.62	0.16	12	8.93	-6.99	6	—	—	—
19.2	18.64	-2.90	11	17.86	-6.99	6	20.83	8.51	2	—	—	—
38.4	37.29	-2.90	5	41.67	8.51	2	31.25	-18.62	1	—	—	—
57.6	55.93	-2.90	3	62.50	8.51	1	62.50	8.51	0	—	—	—
76.8	74.57	-2.90	2	—	—	—	—	—	—	—	—	—
115.2	111.86	-2.90	1	125.00	8.51	0	—	—	—	—	—	—
250.0	223.72	-10.51	0	—	—	—	—	—	—	—	—	—

# PIC18F2220/2320/4220/4320

**TABLE 18-5: BAUD RATES FOR SYNCHRONOUS MODE (SYNC = 1)**

BAUD RATE (K)	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 16.000 MHz			Fosc = 10.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
9.6	—	—	—	—	—	—	15.63	62.76	255	9.77	1.73	255
19.2	—	—	—	19.53	1.73	255	19.23	0.16	207	19.23	0.16	129
38.4	39.06	1.73	255	38.46	0.16	129	38.46	0.16	103	38.46	0.16	64
57.6	57.47	-0.22	173	57.47	-0.22	86	57.97	0.64	68	58.14	0.94	42
76.8	76.92	0.16	129	76.92	0.16	64	76.92	0.16	51	75.76	-1.36	32
96.0	96.15	0.16	103	96.15	0.16	51	95.24	-0.79	41	96.15	0.16	25
250.0	250.00	0.00	39	250.00	0.00	19	250.00	0.00	15	250.00	0.00	9
300.0	303.03	1.01	32	294.12	-1.96	16	307.69	2.56	12	312.50	4.17	7
500.0	500.00	0.00	19	500.00	0.00	9	500.00	0.00	7	500.00	0.00	4
625.0	625.00	0.00	15	625.00	0.00	7	666.67	6.67	5	625.00	0.00	3
1000.0	1000.00	0.00	9	1000.00	0.00	4	1000.00	0.00	3	833.33	-16.67	2
1250.0	1250.00	0.00	7	1250.00	0.00	3	1333.33	6.67	2	1250.00	0.00	1

BAUD RATE (K)	Fosc = 8.000000 MHz			Fosc = 7.159090 MHz			Fosc = 5.068800 MHz			Fosc = 4.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
2.4	7.81	225.52	255	6.99	191.30	255	4.95	106.25	255	3.91	62.76	255
9.6	9.62	0.16	207	9.62	0.23	185	9.60	0.00	131	9.62	0.16	103
19.2	19.23	0.16	103	19.24	0.23	92	19.20	0.00	65	19.23	0.16	51
38.4	38.46	0.16	51	38.08	-0.83	46	38.40	0.00	32	38.46	0.16	25
57.6	57.14	-0.79	34	57.73	0.23	30	57.60	0.00	21	58.82	2.12	16
76.8	76.92	0.16	25	77.82	1.32	22	74.54	-2.94	16	76.92	0.16	12
96.0	95.24	-0.79	20	94.20	-1.88	18	97.48	1.54	12	100.00	4.17	9
250.0	250.00	0.00	7	255.68	2.27	6	253.44	1.38	4	250.00	0.00	3
300.0	285.71	-4.76	6	298.30	-0.57	5	316.80	5.60	3	333.33	11.11	2
500.0	500.00	0.00	3	447.44	-10.51	3	422.40	-15.52	2	500.00	0.00	1
625.0	666.67	6.67	2	596.59	-4.55	2	633.60	1.38	1	—	—	—
1000.0	1000.00	0.00	1	894.89	-10.51	1	—	—	—	1000.00	0.00	0
1250.0	—	—	—	1789.77	43.18	0	1267.20	1.38	0	—	—	—

BAUD RATE (K)	Fosc = 3.579545 MHz			Fosc = 2.000000 MHz			Fosc = 1.000000 MHz			Fosc = 0.032768 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	0.98	225.52	255	0.30	1.14	26
1.2	—	—	—	1.95	62.76	255	1.20	0.16	207	1.17	-2.48	6
2.4	3.50	45.65	255	2.40	0.16	207	2.40	0.16	103	2.73	13.78	2
9.6	9.62	0.23	92	9.62	0.16	51	9.62	0.16	25	8.19	-14.67	0
19.2	19.04	-0.83	46	19.23	0.16	25	19.23	0.16	12	—	—	—
38.4	38.91	1.32	22	38.46	0.16	12	35.71	-6.99	6	—	—	—
57.6	55.93	-2.90	15	55.56	-3.55	8	62.50	8.51	3	—	—	—
76.8	74.57	-2.90	11	71.43	-6.99	6	83.33	8.51	2	—	—	—
96.0	99.43	3.57	8	100.00	4.17	4	—	—	—	—	—	—
250.0	223.72	-10.51	3	250.00	0.00	1	250.00	0.00	0	—	—	—
500.0	447.44	-10.51	1	500.00	0.00	0	—	—	—	—	—	—

# PIC18F2220/2320/4220/4320

## 18.3.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 18-4. The data is received on the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter, operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at Fosc. This mode would typically be used in RS-232 systems.

To set up an Asynchronous Reception:

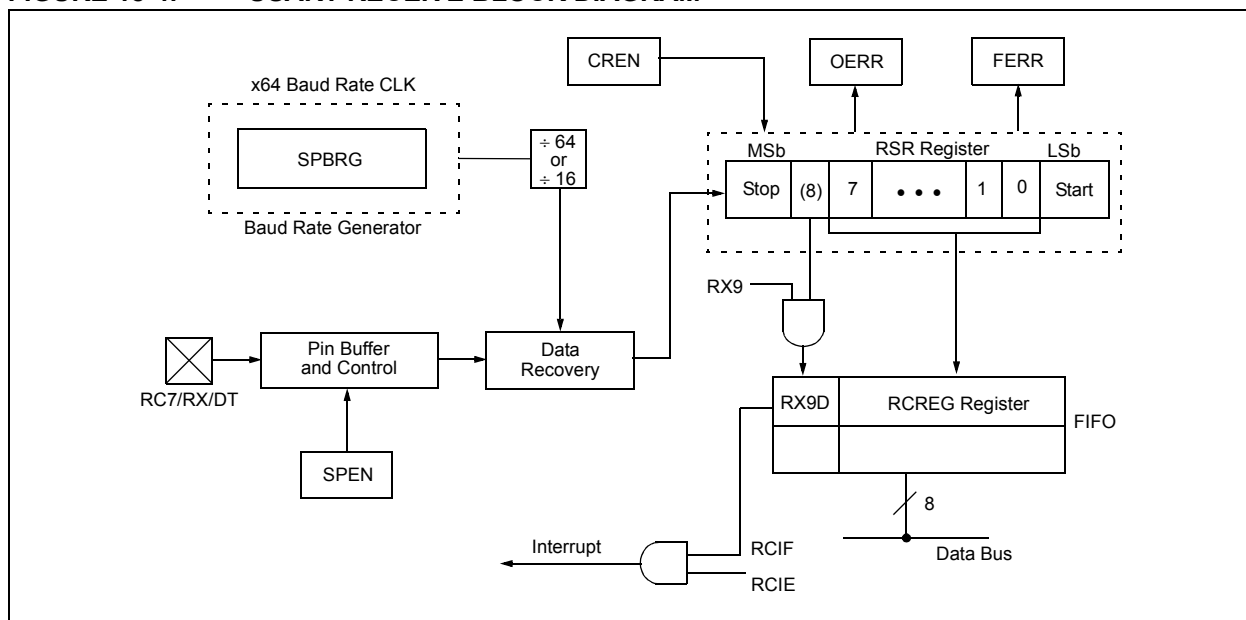
1. Initialize the SPBRG register for the appropriate baud rate. If a high-speed baud rate is desired, set bit BRGH (Section 18.2 “USART Baud Rate Generator (BRG)”).
2. Enable the asynchronous serial port by clearing bit, SYNC, and setting bit, SPEN.
3. If interrupts are desired, set enable bit, RCIE.
4. If 9-bit reception is desired, set bit, RX9.
5. Enable the reception by setting bit, CREN.
6. Flag bit, RCIF, will be set when reception is complete and an interrupt will be generated if enable bit, RCIE, was set.
7. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading the RCREG register.
9. If any error occurred, clear the error by clearing enable bit, CREN.
10. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

## 18.3.3 SETTING UP 9-BIT MODE WITH ADDRESS DETECT

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with address detect enable:

1. Initialize the SPBRG register for the appropriate baud rate. If a high-speed baud rate is required, set the BRGH bit.
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If interrupts are required, set the RCEN bit and select the desired priority level with the RCIP bit.
4. Set the RX9 bit to enable 9-bit reception.
5. Set the ADDEN bit to enable address detect.
6. Enable reception by setting the CREN bit.
7. The RCIF bit will be set when reception is complete. The interrupt will be Acknowledged if the RCIE and GIE bits are set.
8. Read the RCSTA register to determine if any error occurred during reception, as well as read bit 9 of data (if applicable).
9. Read RCREG to determine if the device is being addressed.
10. If any error occurred, clear the CREN bit.
11. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and interrupt the CPU.

**FIGURE 18-4: USART RECEIVE BLOCK DIAGRAM**



## 19.7 A/D Conversions

Figure 19-3 shows the operation of the A/D converter after the  $\overline{\text{GO/DONE}}$  bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

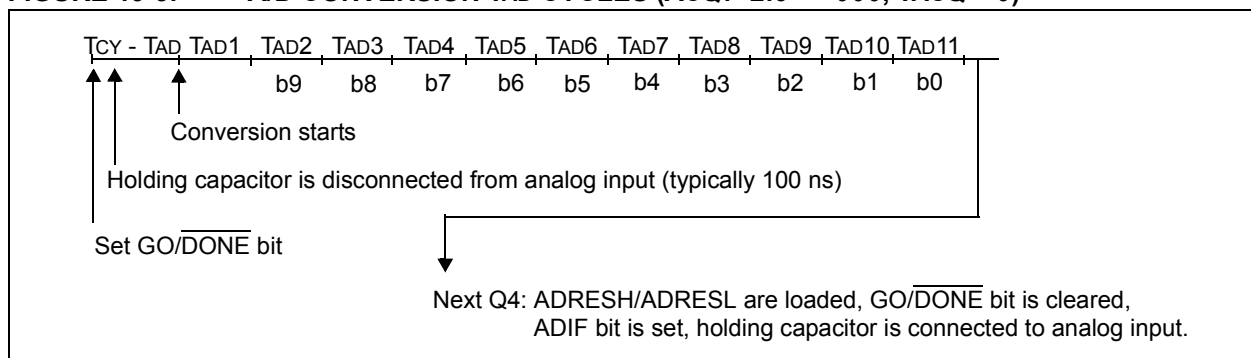
Figure 19-4 shows the operation of the A/D converter after the  $\overline{\text{GO/DONE}}$  bit has been set and the ACQT2:ACQT0 bits are set to '010' and selecting a 4 TAD acquisition time before the conversion starts.

Clearing the  $\overline{\text{GO/DONE}}$  bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

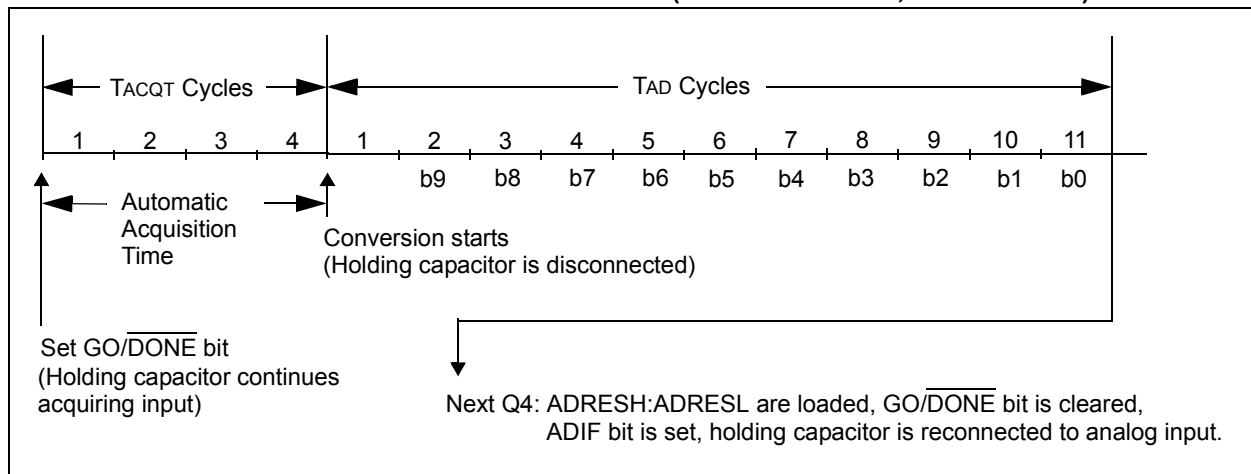
After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

**Note:** The  $\overline{\text{GO/DONE}}$  bit should **NOT** be set in the same instruction that turns on the A/D.

**FIGURE 19-3: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)**



**FIGURE 19-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)**



# PIC18F2220/2320/4220/4320

## 22.2 Operation

Depending on the power source for the device voltage, the voltage normally decreases relatively slowly. This means that the LVD module does not need to be constantly operating. To decrease the current requirements, the LVD circuitry only needs to be enabled for short periods where the voltage is checked. After doing the check, the LVD module may be disabled.

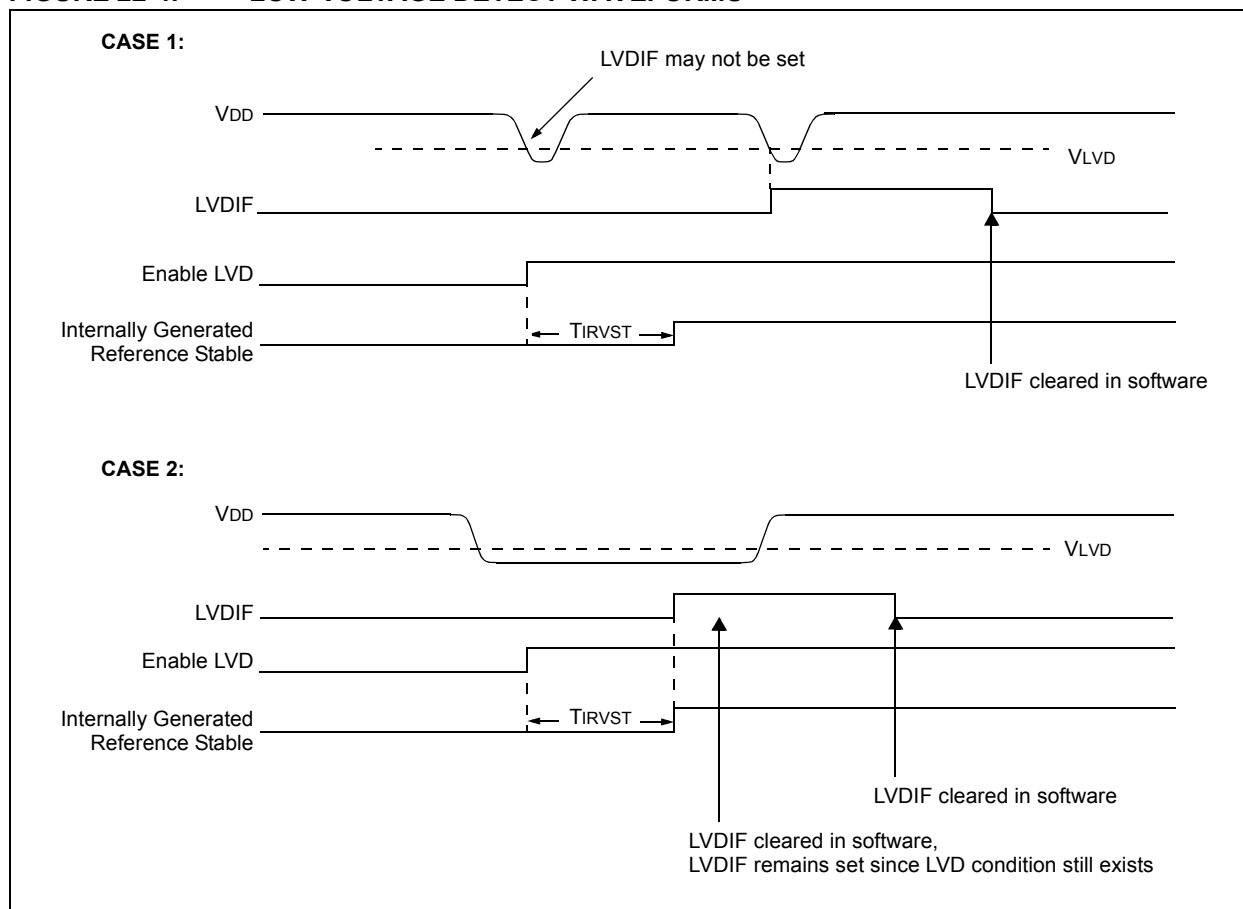
Each time that the LVD module is enabled, the circuitry requires some time to stabilize. After the circuitry has stabilized, all status flags may be cleared. The module will then indicate the proper state of the system.

The following steps are needed to set up the LVD module:

1. Write the value to the LVDL3:LVDL0 bits (LVDCON register) which selects the desired LVD trip point.
2. Ensure that LVD interrupts are disabled (the LVDIE bit is cleared or the GIE bit is cleared).
3. Enable the LVD module (set the LVDEN bit in the LVDCON register).
4. Wait for the LVD module to stabilize (the IRVST bit to become set).
5. Clear the LVD interrupt flag, which may have falsely become set, until the LVD module has stabilized (clear the LVDIF bit).
6. Enable the LVD interrupt (set the LVDIE and the GIE bits).

Figure 22-4 shows typical waveforms that the LVD module may be used to detect.

**FIGURE 22-4: LOW-VOLTAGE DETECT WAVEFORMS**



# PIC18F2220/2320/4220/4320

ADDWFC	ADD W and Carry bit to f				
Syntax:	[ <i>label</i> ] ADDWFC    f [,d [,a]]				
Operands:	$0 \leq f \leq 255$ $d \in [0,1]$ $a \in [0,1]$				
Operation:	$(W) + (f) + (C) \rightarrow \text{dest}$				
Status Affected:	N, OV, C, DC, Z				
Encoding:	<table><tr><td>0010</td><td>00da</td><td>ffff</td><td>ffff</td></tr></table>	0010	00da	ffff	ffff
0010	00da	ffff	ffff		
Description:	Add W, the Carry flag and data memory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'. If 'a' is '0', the Access Bank will be selected. If 'a' is '1', the BSR will not be overridden.				
Words:	1				
Cycles:	1				

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

**Example:**            ADDWFC    REG, W

Before Instruction

Carry bit = 1  
REG = 0x02  
W = 0x4D

After Instruction

Carry bit = 0  
REG = 0x02  
W = 0x50

ANDLW	AND Literal with W				
Syntax:	[ <i>label</i> ] ANDLW    k				
Operands:	$0 \leq k \leq 255$				
Operation:	(W) .AND. k $\rightarrow$ W				
Status Affected:	N, Z				
Encoding:	<table><tr><td>0000</td><td>1011</td><td>kkkk</td><td>kkkk</td></tr></table>	0000	1011	kkkk	kkkk
0000	1011	kkkk	kkkk		
Description:	The contents of W are ANDed with the 8-bit literal 'k'. The result is placed in W.				
Words:	1				
Cycles:	1				

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

**Example:**            ANDLW    0x5F

Before Instruction

W = 0xA3

After Instruction

W = 0x03

# PIC18F2220/2320/4220/4320

## 26.2 DC Characteristics: Power-Down and Supply Current

PIC18F2220/2320/4220/4320 (Industrial)

PIC18LF2220/2320/4220/4320 (Industrial) (Continued)

PIC18LF2220/2320/4220/4320 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial						
PIC18F2220/2320/4220/4320 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended						
Param No.	Device	Typ	Max	Units	Conditions			
	Supply Current (IDD) <sup>(2,3)</sup>							
	PIC18LF2X20/4X20	37	50	μA	-40°C	VDD = 2.0V	FOSC = 1 MHz (PRI_IDLE mode, EC oscillator)	
		37	50	μA	+25°C			
		38	60	μA	+85°C			
	PIC18LF2X20/4X20	58	80	μA	-40°C	VDD = 3.0V		
		59	80	μA	+25°C			
		60	100	μA	+85°C			
	All devices	110	180	μA	-40°C	VDD = 5.0V		
		110	180	μA	+25°C			
		110	180	μA	+85°C			
	Extended devices	125	300	μA	+125°C			
	PIC18LF2X20/4X20	140	180	μA	-40°C	VDD = 2.0V		FOSC = 4 MHz (PRI_IDLE mode, EC oscillator)
		140	180	μA	+25°C			
		140	180	μA	+85°C			
	PIC18LF2X20/4X20	220	280	μA	-40°C	VDD = 3.0V		
		230	280	μA	+25°C			
		230	280	μA	+85°C			
	All devices	410	525	μA	-40°C	VDD = 5.0V		
		420	525	μA	+25°C			
		430	525	μA	+85°C			
	Extended devices	450	800	μA	+125°C			
	Extended devices	2.2	3.0	mA	+125°C	VDD = 4.2V	FOSC = 25 MHz (PRI_IDLE, EC oscillator)	
2.7		3.5	mA	+125°C	VDD = 5.0V			

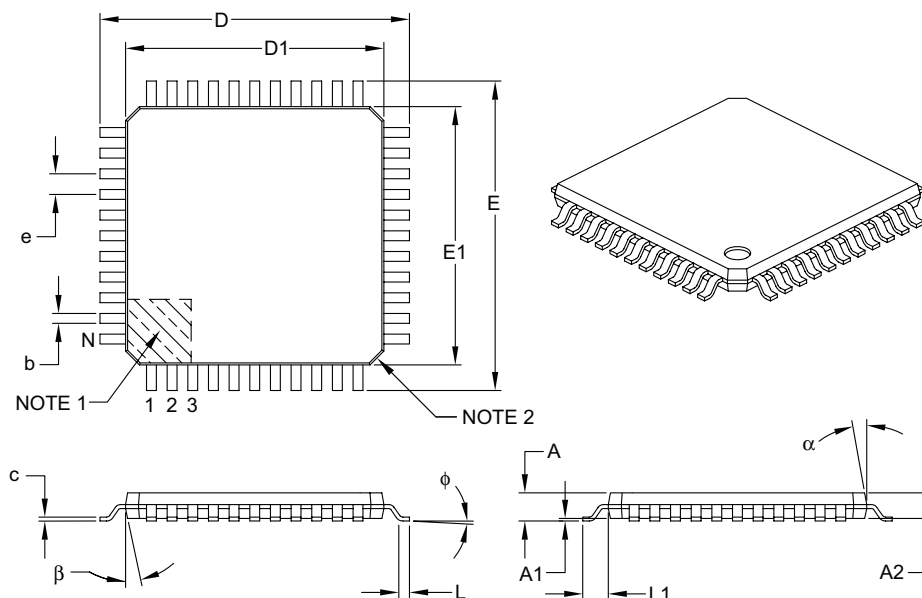
**Legend:** Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.  
The test conditions for all I<sub>DD</sub> measurements in active operation mode are:  
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;  
MCLR = VDD; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula  $I_r = V_{DD}/2R_{EXT}$  (mA) with REXT in kΩ.
- 4:** Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

# PIC18F2220/2320/4220/4320

## 44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packages>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	$\phi$	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	$\alpha$	11°	12°	13°
Mold Draft Angle Bottom	$\beta$	11°	12°	13°

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

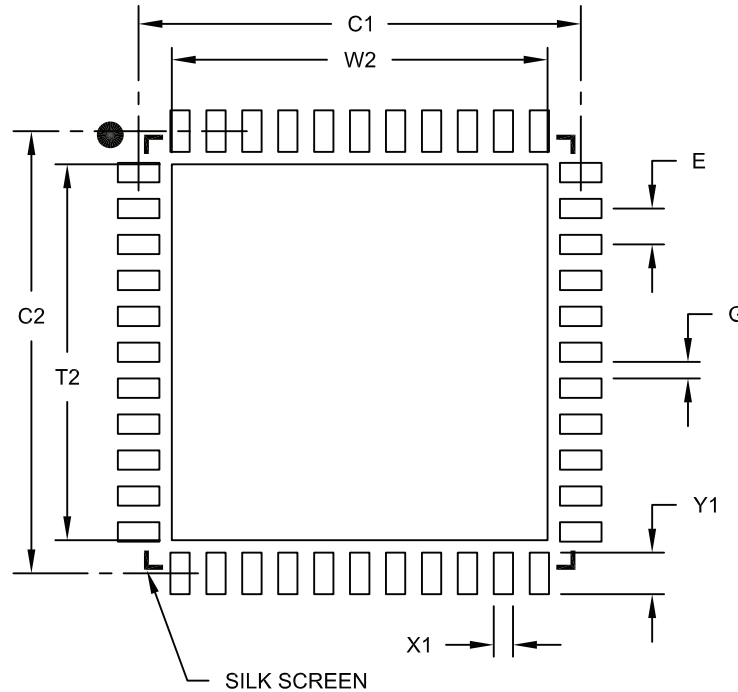
Microchip Technology Drawing C04-076B



# PIC18F2220/2320/4220/4320

## 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

## APPENDIX A: REVISION HISTORY

### Revision A (June 2002)

Original data sheet for PIC18F2X20/4X20 devices.

### Revision B (October 2002)

This revision includes major changes to **Section 2.0 “Oscillator Configurations”** and **Section 3.0 “Power-Managed Modes”**, updates to the Electrical Specifications in **Section 26.0 “Electrical Characteristics”** and minor corrections to the data sheet text.

### Revision C (October 2003)

This revision includes updates to the Electrical Specifications in **Section 26.0 “Electrical Characteristics”** and to the DC Characteristics Graphs and Charts in **Section 27.0 “DC and AC Characteristics Graphs and Tables”** and minor corrections to the data sheet text.

### Revision D (October 2006)

This revision includes updates to the packaging diagrams.

### Revision E (January 2007)

This revision includes updates to the packaging diagrams.

### Revision F (February 2007)

This revision includes updates to the packaging diagrams.

### Revision G (December 2007)

- Modified OSCTUNE register data and added OSCTUN2 register data to **Section 2.6 “Internal Oscillator Block”** and Table 4-3 and Table 5-1.
- Changed Brown-out Voltage values in **Section 26.1 “DC Characteristics: Supply Voltage PIC18F2220/2320/4220/4320 (Industrial) PIC18LF2220/2320/4220/4320 (Industrial)”**.
- Updated low-voltage detect values in Table 26-4.
- Removed RE3 pin references for PIC18F2220/2320 devices in **Section 1.0 “Device Overview”**, **Section 5.0 “Memory Organization”**, **Section 10.0 “I/O Ports”**, **Section 19.0 “10-bit Analog-to-Digital Converter (A/D) Module”** and **Section 23.0 “Special Features of the CPU”**.
- Made minor changes to **Section 17.3.3 “Enabling SPI I/O”**; Table 1-2, Table 1-3, Table 3-3, Table 12-1 and Table 26-2; Figure 12-3 and Figure 16-1; Example 10-1 and Example 10-2; and Table 21-1 and Table 23-1.

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