



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f4320-e-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Din Nomo	Pi	n Numl	ber	Pin Buffer	Description	
Pin Name	PDIP	TQFP	QFN	Туре	Туре	Description
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI RC0 T1OSO T1CKI	15	32	34	I/O O I	ST — ST	Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2 ⁽²⁾	16	35	35	I/O I I/O	ST CMOS ST	Digital I/O. Timer1 oscillator input. Capture 2 input, Compare 2 output, PWM2 output.
RC2/CCP1/P1A RC2 CCP1 P1A	17	36	36	I/O I/O O	ST ST	Digital I/O. Capture 1 input/Compare 1 output/PWM1 output. Enhanced CCP1 output.
RC3/SCK/SCL RC3 SCK SCL	18	37	37	I/O I/O I/O	ST ST ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C™ mode.
RC4/SDI/SDA RC4 SDI SDA	23	42	42	I/O I I/O	ST ST ST	Digital I/O. SPI data in. I ² C data I/O.
RC5/SDO RC5 SDO	24	43	43	I/O O	ST —	Digital I/O. SPI data out.
RC6/TX/CK RC6 TX CK	25	44	44	I/O O I/O	ST — ST	Digital I/O. USART asynchronous transmit. USART synchronous clock (see related RX/DT).
RC7/RX/DT RC7 RX DT	26	1	1	I/O I I/O	ST ST ST	Digital I/O. USART asynchronous receive. USART synchronous data (see related TX/CK).
Legend: TTL = TTL ST = Sch O = Out	mitt Trig put	gger inp	out with		evels	CMOS = CMOS compatible input or output I = Input P = Power

TABLE 1-3: PIC18F4220/4320 PINOUT I/O DESCRIPTIONS (CONTINUED)

OD = Open-drain (no diode to VDD) **Note 1:** Alternate assignment for CCP2 when CCP2MX is cleared.

2: Default assignment for CCP2 when CCP2MX (CONFIG3H<0>) is set.

Pin Name	Pi	n Numl	ber	Pin	Buffer	Description			
	PDIP	TQFP	QFN	Туре	Туре	Description			
RE0/AN5/RD	8	25	25			PORTE is a bidirectional I/O port.			
RE0 AN5 RD				I/O I I	ST Analog TTL	Digital I/O. Analog input 5. Read control for Parallel Slave Port (see also WR and CS pins).			
RE1/AN6/WR RE1 AN6 WR	9	26	26	I/O I I	ST Analog TTL	Digital I/O. Analog input 6. Write <u>control for</u> Parallel Slave Port (see CS and RD pins).			
RE2/AN7/CS RE2 AN7 CS	10	27	27	I/O I I	ST Analog TTL	Digital I/O. Analog input 7. Chip select control fo <u>r P</u> arallel Slave Port (see related RD and WR).			
RE3	1	18	18		_	See MCLR/VPP/RE3 pin.			
Vss	12, 31	6, 29	6, 30, 31	Ρ		Ground reference for logic and I/O pins.			
Vdd	11, 32	7, 28	7, 8 29	Ρ		Positive supply for logic and I/O pins.			
NC			13, 28	NC	NC	No connect.			
Legend: TTL = TTL ST = Schr		tible inp ger inp		CMOS	6 levels	CMOS = CMOS compatible input or output I = Input			

TABLE 1-3: PIC18F4220/4320 PINOUT I/O DESCRIPTIONS (CONTINUED)

O = Output

Ρ = Power

OD = Open-drain (no diode to VDD)

Note 1: Alternate assignment for CCP2 when CCP2MX is cleared.

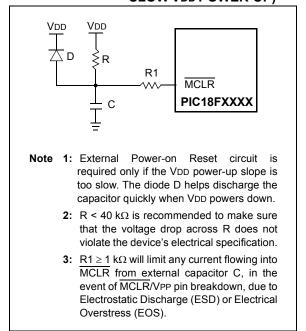
2: Default assignment for CCP2 when CCP2MX (CONFIG3H<0>) is set.

4.1 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected. To take advantage of the POR circuitry, just tie the MCLR pin through a resistor (1k to 10 k Ω) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004). For a slow rise time, see Figure 4-2.

When the device starts normal operation (i.e., exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

FIGURE 4-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



4.2 Power-up Timer (PWRT)

The Power-up Timer (PWRT) of the PIC18F2X20/4X20 devices is an 11-bit counter, which uses the INTRC source as the clock input. This yields a count of 2048 x 32 μ s = 65.6 ms. While the PWRT is counting, the device is held in Reset.

The power-up time delay depends on the INTRC clock and will vary from chip-to-chip due to temperature and process variation. See DC parameter #33 for details.

The PWRT is enabled by clearing Configuration bit, PWRTEN.

4.3 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over (parameter #33). This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP, HS and HSPLL modes and only on Power-on Reset, or on exit from most power-managed modes.

4.4 PLL Lock Time-out

With the PLL enabled in its PLL mode, the time-out sequence following a Power-on Reset is slightly different from other oscillator modes. A portion of the Power-up Timer is used to provide a fixed time-out that is sufficient for the PLL to lock to the main oscillator frequency. This PLL lock time-out (TPLL) is typically 2 ms and follows the oscillator start-up time-out.

4.5 Brown-out Reset (BOR)

A Configuration bit, BOREN, can disable (if clear/ programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below VBOR (parameter D005) for greater than TBOR (parameter #35), the brown-out situation will reset the chip. A Reset may not occur if VDD falls below VBOR for less than TBOR. The chip will remain in Brown-out Reset until VDD rises above VBOR. If the Power-up Timer is enabled, it will be invoked after VDD rises above VBOR; it then will keep the chip in Reset for an additional time delay TPWRT (parameter #33). If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above VBOR, the Power-up Timer will execute the additional time delay. Enabling BOR Reset does not automatically enable the PWRT.

4.6 Time-out Sequence

On power-up, the time-out sequence is as follows: First, after the POR pulse has cleared, PWRT time-out is invoked (if enabled). Then, the OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 4-3, Figure 4-4, Figure 4-5, Figure 4-6 and Figure 4-7 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, all time-outs will expire. Bringing $\overline{\text{MCLR}}$ high will begin execution immediately (Figure 4-5). This is useful for testing purposes or to synchronize more than one PIC18FXXXX device operating in parallel.

Table 4-2 shows the Reset conditions for some Special Function Registers, while Table 4-3 shows the Reset conditions for all the registers.

5.3 Fast Register Stack

A "fast return" option is available for interrupts. A Fast Register Stack is provided for the STATUS, WREG and BSR registers and are only one in depth. The stack is not readable or writable and is loaded with the current value of the corresponding register when the processor vectors for an interrupt. The values in the registers are then loaded back into the working registers if the RETFIE, FAST instruction is used to return from the interrupt.

All interrupt sources will push values into the stack registers. If both low and high-priority interrupts are enabled, the stack registers cannot be used reliably to return from low-priority interrupts. If a high-priority interrupt occurs while servicing a low-priority interrupt, the stack register values stored by the low-priority interrupt will be overwritten. Users must save the key registers in software during a low-priority interrupt.

If interrupt priority is not used, all interrupts may use the Fast Register Stack for returns from interrupt.

If no interrupts are used, the Fast Register Stack can be used to restore the STATUS, WREG and BSR registers at the end of a subroutine call. To use the Fast Register Stack for a subroutine call, a CALL label, FAST instruction must be executed to save the STATUS, WREG and BSR registers to the Fast Register Stack. A RETURN, FAST instruction is then executed to restore these registers from the Fast Register Stack.

Example 5-1 shows a source code example that uses the Fast Register Stack during a subroutine call and return.

EXAMPLE 5-1: FAST REGISTER STACK CODE EXAMPLE

	-
CALL SUB1, FAST	;STATUS, WREG, BSR
	;SAVED IN FAST REGISTER
	;STACK
•	
•	
SUB1 •	
•	
RETURN FAST	;RESTORE VALUES SAVED
	;IN FAST REGISTER STACK

5.4 PCL, PCLATH and PCLATU

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21-bits wide. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits and is not directly readable or writable. Updates to the PCH register may be performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits and is not directly readable or writable. Updates to the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits and is not directly readable or writable. Updates to the PCU register may be performed through the PCLATU register.

The contents of PCLATH and PCLATU will be transferred to the program counter by any operation that writes PCL. Similarly, the upper two bytes of the program counter will be transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see **Section 5.8.1** "**Computed** GOTO").

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the LSB of PCL is fixed to a value of '0'. The PC increments by 2 to address sequential instructions in the program memory.

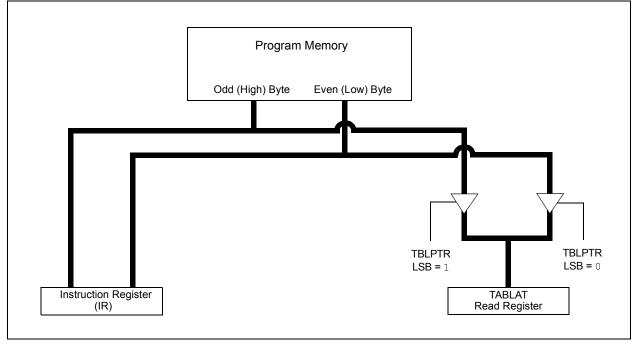
The CALL, RCALL, GOTO and program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

6.3 Reading the Flash Program Memory

The TBLRD instruction is used to retrieve data from program memory and place it into data RAM. Table reads from program memory are performed one byte at a time.

TBLPTR points to a byte address in program space. Executing a TBLRD instruction places the byte pointed to into TABLAT. In addition, TBLPTR can be modified automatically for the next table read operation. The internal program memory is typically organized by words. The Least Significant bit of the address selects between the high and low bytes of the word. Figure 6-4 shows the interface between the internal program memory and the TABLAT.

FIGURE 6-4: READS FROM FLASH PROGRAM MEMORY



EXAMPLE 6-1: READING A FLASH PROGRAM MEMORY WORD

	MOVLW	CODE_ADDR_UPPER	;	Load TBLPTR with the base
	MOVWF	TBLPTRU	;	address of the word
	MOVLW	CODE_ADDR_HIGH		
	MOVWF	TBLPTRH		
	MOVLW	CODE ADDR LOW		
	MOVWF	TBLPTRL		
READ_WORD				
	TBLRD*+		;	read into TABLAT and increment TBLPTR
	MOVFW	TABLAT	;	get data
	MOVWF	WORD EVEN		
	TBLRD*+	_	;	read into TABLAT and increment TBLPTR
	MOVFW	TABLAT	;	get data
	MOVWF	WORD_ODD		

9.2 PIR Registers

The PIR registers contain the individual flag bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are two Peripheral Interrupt Flag registers (PIR1, PIR2).

- **Note 1:** Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).
 - 2: User software should ensure the appropriate interrupt flag bits are cleared prior to enabling an interrupt and after servicing that interrupt.

REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7				•			bit 0
Legend:	- F.H		L :4			l (0)	
R = Readable		W = Writable		•	mented bit, read		
-n = Value at	PUR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	lown
bit 7	PSPIF: Para	llel Slave Port F	Read/Write Inf	terrupt Flag bit ⁽	(1)		
	1 = A read o		ion has taken		e cleared in sof	tware)	
bit 6	ADIF: A/D C	onverter Interru	pt Flag bit				
		conversion com		be cleared in s	oftware)		
6.4 F		conversion is r	•				
bit 5		T Receive Inter		is full (cleared	when RCREG i	s read)	
		ART receive but				51000	
bit 4	TXIF: USAR	T Transmit Inter	rupt Flag bit				
		ART transmit bu ART transmit bu		is empty (clear	red when TXRE	G is written)	
bit 3	SSPIF: Mast	er Synchronous	Serial Port I	nterrupt Flag b	it		
		smission/recept o transmit/recei		te (must be cle	ared in software	e)	
bit 2	CCP1IF: CC	P1 Interrupt Fla	g bit				
		<u>le:</u> register capture 1 register captu		ust be cleared	in software)		
					cleared in softw	/are)	
	<u>PWM mode:</u> Unused in th						
bit 1	TMR2IF: TM	R2 to PR2 Mate	ch Interrupt F	lag bit			
		PR2 match oc 2 to PR2 match	•	be cleared in s	oftware)		
bit 0	TMR1IF: TM	R1 Overflow Int	terrupt Flag b	it			
		egister overflow egister did not o		leared in softw	vare)		

Note 1: This bit is reserved on PIC18F2X20 devices; always maintain this bit clear.

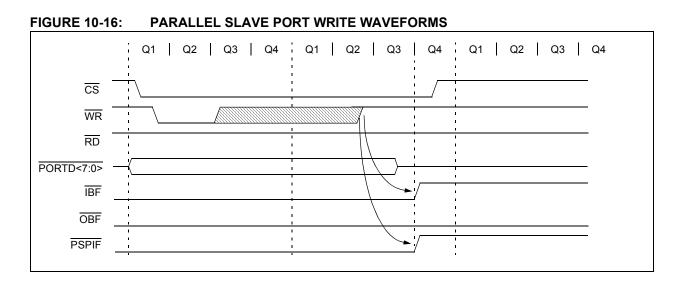


FIGURE 10-17: PARALLEL SLAVE PORT READ WAVEFORMS

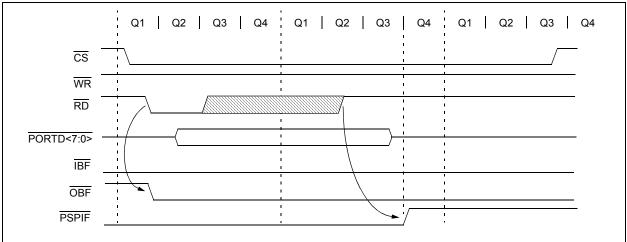


TABLE 10-11: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
PORTD	Port Data Latch when written; Port pins when read									uuuu uuuu
LATD	LATD Data	a Latch bit	s						XXXX XXXX	uuuu uuuu
TRISD	PORTD D	ata Directi	on bits						1111 1111	1111 1111
PORTE	_	_	_	_	RE3	RE2	RE1	RE0	qxxx	quuu
LATE	_	_	_	_	_	LATE Data	a Latch bits		xxx	uuu
TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE D	ata Directio	n bits	0000 -111	0000 -111
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IF	INTOIE	RBIE	TMR0IF	INTOIF	RBIF	0000 000x	0000 000u
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	1111 1111	1111 1111
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	00 0000	00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Parallel Slave Port.

14.0 TIMER3 MODULE

The Timer3 module timer/counter has the following features:

- 16-bit timer/counter (two 8-bit registers: TMR3H and TMR3L)
- Readable and writable (both registers)
- · Internal or external clock select
- Interrupt-on-overflow from FFFFh to 0000h
- · Reset from CCP module trigger

Figure 14-1 is a simplified block diagram of the Timer3 module.

Register 14-1 shows the Timer3 Control register. This register controls the operating mode of the Timer3 module and sets the CCP clock source.

Register 12-1 shows the Timer1 Control register. This register controls the operating mode of the Timer1 module, as well as contains the Timer1 Oscillator Enable bit (T1OSCEN) which can be a clock source for Timer3.

REGISTER 14-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON
bit 7							bit 0

Legend:				
R = Readal	ole bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value a	at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 7	RD16 : 16	-Bit Read/Write Mode Enab	le bit	
		oles register read/write of Tin oles register read/write of Tin		
bit 6, 3	T3CCP2:	T3CCP1: Timer3 and Timer	1 to CCPx Enable bits	
	01 = Tim Tim	er3 is the capture/compare o er1 is the capture/compare o		
bit 5-4	T3CKPS	1:T3CKPS0: Timer3 Input C	lock Prescale Select bits	
		Prescale value		
		Prescale value Prescale value		
		Prescale value		
bit 2		: Timer3 External Clock Inpu le if the device clock comes	t Synchronization Control bit from Timer1/Timer3.)	
	1 = Do no	I <u>R3CS = 1:</u> ot synchronize external clock nronize external clock input	(input	
		I <u>R3CS = 0:</u> ignored. Timer3 uses the in	ternal clock when TMR3CS =	= 0.
bit 1	TMR3CS	: Timer3 Clock Source Selec	ct bit	
		rnal clock input from Timer1 o nal clock (Fosc/4)	oscillator or T13CKI (on the ris	sing edge after the first falling edge
bit 0	TMR3ON	: Timer3 On bit		
	1 = Enat 0 = Stop	oles Timer3 s Timer3		

17.4.9 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit (SSPCON2<1>) is programmed high and the I²C logic module is in the Idle state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded with the contents of SSPADD<5:0> and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. Following this, the RSEN bit (SSPCON2<1>) will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. The SSPIF bit will not be set until the Baud Rate Generator has timed out.

- Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.
 - A bus collision during the Repeated Start condition occurs if:
 - SDA is sampled low when SCL goes from low-to-high.
 - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

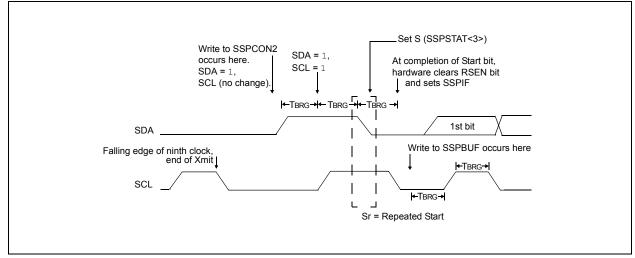
Immediately following the SSPIF bit getting set, the user may write the SSPBUF with the 7-bit address in 7-bit mode, or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then transmit an additional eight bits of address (10-bit mode) or eight bits of data (7-bit mode).

17.4.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Repeated Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queueing of events is not allowed, writing of the lower 5 bits of SSPCON2 is disabled until the Repeated Start condition is complete.

FIGURE 17-20: REPEAT START CONDITION WAVEFORM



REGISTER 18-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7		L					bit
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 7	SPEN: Seria	al Port Enable bi	t				
		ort enabled (con		and TX/CK pir	ns as serial por	t pins)	
	•	ort disabled (hel	•	·		. ,	
bit 6	RX9: 9-Bit F	Receive Enable I	oit				
		9-bit reception 8-bit reception					
bit 5	SREN: Sing	le Receive Enat	ole bit				
	<u>Asynchrono</u> Don't care.	<u>us mode:</u>					
	1 = Enable 0 = Disable	<u>is mode – Maste</u> s single receive s single receive eared after rece		ete			
		s mode – Slave:					
bit 4	CREN: Con	tinuous Receive	Enable bit				
	Asynchrono 1 = Enables 0 = Disables Synchronou 1 = Enables	s receiver s receiver	eive until enab	ble bit, CREN, is	s cleared (CRE	N overrides SR	EN)
	0 = Disables	s continuous rec	eive				
bit 3		Idress Detect En					
	1 = Enables	<u>us mode 9-bit (F</u> s address detect s address detec	ion, enables i				
bit 2	FERR: Fran	ning Error bit					
	1 = Framing 0 = No fram	ı error (can be u ing error	odated by rea	ding RCREG re	egister and rece	eiving next valio	l byte)
bit 1	OERR: Ove	rrun Error bit					
	1 = Overrun 0 = No over	error (can be cl run error	eared by clea	ring bit CREN)			
bit 0	RX9D: 9th b	oit of Received D)ata				

REGISTER 23-12: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2220/2320/4220/4320 DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is un	programmed	u = Unchanged from programmed state

bit 7-5	DEV2:DEV0: Device ID bits
	000 = PIC18F2320
	001 = PIC18F4320
	100 = PIC18F2220
	101 = PIC18F4220
bit 4-0	REV3:REV0: Revision ID bits
	These bits are used to indicate the device revision.

REGISTER 23-13: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2220/2320/4220/4320 DEVICES

R	R	R	R	R	R	R	R
DEV10 ⁽¹⁾	DEV9 ⁽¹⁾	DEV8 ⁽¹⁾	DEV7 ⁽¹⁾	DEV6 ⁽¹⁾	DEV5 ⁽¹⁾	DEV4 ⁽¹⁾	DEV3 ⁽¹⁾
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is un	programmed	u = Unchanged from programmed state

bit 7-0 **DEV10:DEV3:** Device ID bits These bits are used with the DEV2:DEV0 bits in the Device ID Register 1 to identify the part number. 0000 0101 = PIC18F2220/2320/4220/4320 devices

Note 1: These values for DEV10:DEV3 may be shared with other devices. The specific device is always identified by using the entire DEV10:DEV0 bit sequence.

After Instruction

If Carry PC If Carry PC

= = =

ANDWF	AND W with f		BC	Branch if	Carry	
Syntax:	[label] ANDWF f	,d [,a]]	Syntax:	[<i>label</i>] E	BC n	
Operands:	$0 \leq f \leq 255$		Operands:	-128 ≤ n ≤	≤ 12 7	
	d ∈ [0,1] a ∈ [0,1]		Operation:	if Carry bi (PC) + 2 ·	t is '1', + 2n → PC	
Operation:	(W) .AND. (f) \rightarrow dest		Status Affect	ed: None		
Status Affected:	N, Z		Encoding:	1110	0010 nn	nn nnnn
Encoding:	0001 01da ff	ff ffff	Description:	If the Car	ry bit is '1', th	ien the
Description: The contents of W are AND'ed with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank will be selected. If 'a' is '1', the BSR will not be overridden (default).			The 2's co added to have incre instruction PC + 2 +	the PC. Sinc emented to fe		
Words:	1		Words:	1		
Cycles:	1		Cycles:	1(2)		
Q Cycle Activity:			Q Cycle Act	ivity:		
Q1	Q2 Q3	Q4	If Jump:			_
Decode	Read Process	Write to	Q1	Q2	Q3	Q4
	register 'f' Data	destination	Decod	e Read literal 'n'	Process Data	Write to PC
Example:	ANDWF REG, W		No operati	No on operation	No operation	No operation
Before Instru			If No Jump:			
W REG	= 0x17 = 0xC2		Q1	Q2	Q3	Q4
After Instruct	ion		Decod	e Read literal	Process Data	No operation
W REG	= 0x02 = 0xC2				Dulu	operation
REG	= 0xC2		Example:	HERE	BC JUMP)
			Before I PC	nstruction = ac	Idress (HERE)

1; address (JUMP) 0; address (HERE + 2)

BTG	Bit Toggle	e f			BO	/	Branch if	Overflow	
Syntax:	[<i>label</i>] B	TG f,b[,a]			Synt	Syntax: [<i>label</i>] BOV n		OV n	
Operands:	0 ≤ f ≤ 255	5			Ope	rands:	-128 ≤ n ≤	127	
	0 ≤ b < 7 a ∈ [0,1]				Ope	ration:	if Overflow (PC) + 2 +		
Operation:	$(\overline{f} < b >) \to f$				State	us Affected:	None		
Status Affected:	None				Enc	odina:	1110	0100 nn	nn nnnn
Encoding:	0111	bbba	ffff	ffff		cription:	-	flow bit is '1	
Description:	Bit 'b' in da inverted. I' will be sele value. If 'a selected a (default).	f 'a' is '0', ' ected, ove ' = 1, ther	the Acces erriding the the bank	s Bank e BSR will be			added to t have incre instruction PC + 2 + 2	mplement n he PC. Sinc mented to f	
Words:	1				Wor	de	1		
Cycles:	1	1				-			
Q Cycle Activity:					Cyc		1(2)		
Q1	Q2	Q3	Q			Q Cycle Activity: If Jump:			
Decode	Read register 'f'	Process Data	Wri regist		11 51	Q1	Q2	Q3	Q4
Example:	BTG F	PORTC, 4				Decode	Read literal 'n'	Process Data	Write to PC
Before Instru						No	No	No	No
PORTC		101 [0x75	5]		LE NI	operation	operation	operation	operation
After Instructi	ion:	-	-		IT N	o Jump:	00	00	<u></u>
PORTC = 0110 0101 [0x65]				Q1	Q2	Q3	Q4		
						Decode	Read literal 'n'	Process Data	No operation
						L		Data	operation
					Exa	<u>mple</u> :	HERE	BOV JUME	2
						Before Instr	uction		

PC

After Instruction

If Overflow = PC = If Overflow = PC =

=

1;

address (HERE)

address (JUMP) 0; address (HERE + 2)

Syntax: $[label]$ CPFSGT $f [a]$ Operands: $0 \le f \le 255$ $a \in [0,1]$ Operands: $0 \le f \le 255$ $a \in [0,1]$ Operands: $0 \le f \le 255$ Operands: $0 \le f \le 255$ $a \in [0,1]$ Operands: $0 \le f \le 255$ Description: $0 \ge f \le 255$ Compares the contents of data memory location 1 to the contents $0 \le f \le 255$ $a \in [0,1]$ Operands: $0 \le f \le 255$ Description:Compares the contents of data memory location 1 to the contentsIf the contents of V are greater than the contents of V REG, then the fetched instruction is discarded and a sof is executed instead, making its tis a two-cycle instruction. If a 's 's '', the Access Bank will be selected. coverding the DBR value, (default).Words:1Cycles:1(2) Note:Note:3 cycles if skip and followed by a 2-word instruction.Q 1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q1Q2Q3Q2Q3Q1Q2Q3Q2Q3Q1Q2Q3Q2Q3Q1Q2Q3Q2Q3Q1Q2Q3Q2Q3Q1Q2Q3Q2Q3Q1Q2Q3<	CPFSGT	Compare	f with W, Sk	tip if f > W	CPF	SLT	Compar	e f with W, Sl	kip if f < W	
$\begin{array}{ccccc} a \in [0,1] \\ Operation: (f) = (W), \\ (unsigned comparison) \\ Status Affected: None \\ Encoding: 0110 0104 rfff fff fff \\ Description: Compares the contents of data memory location if to the contents of the contents of the performing an unsigned subtraction. If a file contents of the greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If a file contents of the BSR value (default). \\ Words: 1 \\ Cycles: 1 (C) \\ Words: 1 \\ Cycles: 1 (C) \\ Words: 1 \\ Cycles: 1 (C) \\ Words: 3 cycles if skip and followed by a 2-word instruction. \\ Q Cycle Activity: Q1 Q2 Q3 Q4 \\ If skip in Q1 Q2 Q3 Q4 \\ If skip in to looperation operation o$	Syntax:	[label] (CPFSGT f[,a]	Syn	tax:	[label]	CPFSLT f[,a]	
skip if (f) > (W) (unsigned comparison)Status Affected:NoneEncoding:OlioOlioStatus Affected:NoneDescription:Compares the contents of data memory location ft to the contents of the W by performing an unsigned subtraction.Status Affected:NoneDescription:Compares the contents of the contents of WEEG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If a 's is the selected as per the BSR value (default).OutputUrdefault.Cycle instruction:Q Cycle Activity:Q Cycles if skip and followed by a 2-word instruction.Q Cycle Activity:Q C Cycle Activity:Q C Cycle Activity:Q C Cycle Activity:Q C C Cycle Activity: <th col<="" td=""><td>Operands:</td><td></td><td>5</td><td></td><td>Оре</td><td>rands:</td><td></td><td>55</td><td></td></th>	<td>Operands:</td> <td></td> <td>5</td> <td></td> <td>Оре</td> <td>rands:</td> <td></td> <td>55</td> <td></td>	Operands:		5		Оре	rands:		55	
Encoding:0110010arfrftrfrftDescription:Compares the contents of data memory location 'f to the contents of the W by performing an unsigned subtraction. If the contents of 'f are greater than the contents of 'f are greater than the contents of WREG, then the fetched instruction is discarded and a NO2 is executed instead, making this a two-cycle instruction. If 'a is '0', the Access Bank will be selected, overriding the BSR value. If are just the mether will be selected as per the BSR value. (default).Encoding:Compares the contents of f are less than the contents of 'f are less than the content o	Operation:	skip if (f) >		1	Ope	ration:	skip if (f)	< (W))	
Description:Compares the contents of data memory location 1' to the contents of the W by performing an unsigned subtraction.Description:Compares the contents of data memory location 1' to the contents of W by performing an unsigned subtraction.If the contents of Y are greater than the contents of Y are less than the selected, overriding the BSR value. (default).Words:1Cycles1(2)Words:1Cycles3 cycles if skip and followed by a 2-word instruction.Q Cycle Activity:Q1Q1Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q3Q4Q2Q4NoNoNoNooperationoperationoperationoperationQ cycle Activity:Q1Q1Q2Q3Q4Q4NoNoNoNoNoNoNoNoNoNo <t< td=""><td>Status Affected:</td><td>None</td><td></td><td></td><td>Stat</td><td>us Affected:</td><td>None</td><td></td><td></td></t<>	Status Affected:	None			Stat	us Affected:	None			
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	Encoding:	0110	010a ffi	ff ffff	Enc	oding:	0110	000a ff	ff ffff	
Words:1Note:3 cycles if skip and followe by a 2-word instruction.Q Cycle Activity:Q1Q2Q3Q4 $Q Cycle Activity:Q1Q2Q3Q4Q Cycle Activity:Q1Q2Q3Q4Q Cycle Activity:Q1Q2Q3Q4Q Cycle Activity:Q1Q2Q3Q4Q Cycle Activity:Q1Q2Q3Q4Q Cycle Activity:Q1Q2Q3Q4Q 1Q2Q3Q4NoNoQ 1Q2Q3Q4NoNoQ 1Q2Q3Q4NoNoQ 1Q2Q3Q4NoNoQ 1Q2Q3Q4NoNoQ 1Q2Q3Q4NoNoQ 1Q2Q3Q4NoNoQ 1Q2Q3Q4NoNoQ 1Q2Q3Q4NoQ 1Q2Q3Q4Q 1Q2Q3Q4Q 1Q2Q3Q4Q 1Q2Q3Q4Q 1Q2Q3Q4Q 2Q3Q4Q 1Q2Q3Q4Q 2Q3Q4Q 2Q3Q4Q 2Q3Q4Q 2Q3Q4Q 2Q3Q4Q 2NoNoQ 2$	Description:	memory lo of the W b unsigned If the conter fetched ins a NOP is e this a two- '0', the Ac selected, o If 'a' = 1, t selected a	bocation 'f' to t by performing subtraction. ents of 'f' are nts of WREG struction is di xecuted instruc cess Bank w boverriding the hen the bank	s of data the contents g an g greater than i, then the iscarded and ead, making ction. If 'a' is vill be e BSR value. k will be SR value		ds:	memory of W by subtracti If the conte instruction is execute two-cycle Access E is '1', the overridde	location 'f' to performing an on. Intents of 'f' are ents of W, the on is discarded red instead, m e instruction. I Bank will be se BSR will not	the contents unsigned e less than in the fetched d and a NOP aking this a f 'a' is '0', the elected. If 'a'	
Cycles:1(2)by a 2-word instruction.Note:3 cycles if skip and followed by a 2-word instruction.Q Cycle Activity:Q1Q2Q3Q4 $Q 1$ Q2Q3Q4 $Q1$ Q2Q3Q4 $Q 1$ Q2Q3Q4 $Q1$ Q2Q3Q4 No NoNoNoNoNoNo $operation$ operationoperationoperationoperationoperation $Q 1$ Q2Q3Q4 $Q1$ Q2Q3Q4 Mo NoNoNoNoNoNo $operation$ operationoperationoperationoperation $Q 1$ Q2Q3Q4 No NoNo No NoNoNoNoNoNo<	Words:	1			Cyc	165.		cycles if skip	and followed	
$\begin{array}{c c c c c c c c } Q C cycle Activity: \\ \hline Q 1 & Q 2 & Q 3 & Q 4 \\ \hline \hline Decode & Read & Process & No \\ \hline Decode & Read & Proces & No \\ \hline Decode & Read & Proce & Proce & Proce \\ \hline Decode & Readres & Proce & Proce \\ \hline $	Cycles:	Note: 3 d			Q		t :	y a 2-word in	struction.	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Q Cycle Activit	-					1		1	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Q1	Q2	Q3	Q4		Decode				
If skip: $\begin{array}{c c c c c c c c c c c c c c c c c c c $	Decode				lf s	kip:				
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	lf skin [.]	register t	Data	operation			1		1	
$\begin{tabular}{ c c c c c c } \hline No & No & No & operation & oper$	-	Q2	Q3	Q4						
If skip and followed by 2-word instruction:Q1Q2Q3Q4 \boxed{No} <td< td=""><td>No</td><td></td><td></td><td></td><td>lf s</td><td></td><td></td><td></td><td></td></td<>	No				lf s					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				· ·		Q1	Q2	Q3	Q4	
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	-	-								
operationoperationoperationoperationNoNoNoNooperationin the transformed equationoperationin the		-						· ·		
operationoperationoperationoperationoperationoperationoperationExample:HERECPFSLT REGExample:HERECPFSGT REGNLESS:LESS:MGREATER:MGREATER:LESS:GREATER:PC=Address (HERE)PC=PC=Address (HERE)W=?PC=Address (HERE)If REG<	operation	operation	operation	operation			operation	operation		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	operation	operation HERE	operation	operation	<u>Exa</u>		NLESS LESS	:		
PC=Address (HERE)After InstructionW=?If REG $<$ W;After InstructionIf REG>W;If REG>W;PC=Address (GREATER)If REG \geq W;If REG \leq W;PC=If REG \leq W;PC=		GREATER	:			PC	= A	ddress (HERE)	
$W = ?$ $After Instruction$ $If REG > W;$ $PC = Address (GREATER)$ $If REG \leq W;$ $PC = Address (MLESS)$ $If REG \geq W;$ $PC = Address (NLESS)$							•			
After InstructionPC=Address (LESS)If REG>W;If REG \geq W;PC=Address (GREATER)PC=Address (NLESS)If REG \leq W; $=$ Address (NLESS) \leq			dress (HERE)				٧·		
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	After Instru	ction				PC		,)	
	If REG PC If REG	> W; = Ad ≤ W;	dress (grea						S)	

MULLW	Multiply I	_iteral with \	v	MULWF	Multiply V	V with f	
Syntax:	[label]	MULLW k		Syntax:	[label]	MULWF f	[,a]
Operands:	$0 \le k \le 25$	5		Operands:	$0 \le f \le 258$	5	
Operation:	(W) x k \rightarrow PRODH:PRODL			a ∈ [0,1]			
Status Affected:	None			Operation:	(W) x (f) –	→ PRODH:P	RODL
Encoding:	0000	1101 kk	kk kkkk	Status Affected:	None		
Description:	An unsign	ed multiplica	tion is	Encoding:	0000	001a ffi	ff ffff
carried out between the conter of W and the 8-bit literal 'k'. Th 16-bit result is placed in PRODH:PRODL register pair. PRODH contains the high byte W is unchanged. None of the Status flags are		al 'k'. The n ter pair. ligh byte.	Description:	carried ou of W and t 'f'. The 16 the PROD pair. PRO byte.	ed multiplica t between th he register fi -bit result is H:PRODL re DH contains nd 'f' are unc	e contents le location stored in egister the high	
	carry is po	neither overf ossible in this ro result is po red.	opera-		None of th affected. Note that carry is po	ne Status flag neither overl ossible in this	gs are flow nor s opera-
Words:	1					o result is po ed. If 'a' is '0	
Cycles:	1					ank will be se	
Q Cycle Activity:					•	the BSR va	
Q1	Q2	Q3	Q4	1		n the bank v is per the BS	
Decode	Read literal 'k'	Process Data	Write registers		(default).	o por allo 20	
			PRODH:	Words:	1		
			PRODL	Cycles:	1		
Example:	MULLW	0xC4		Q Cycle Activity	:		
Before Instru		01101		Q1	Q2	Q3	Q4
W PRODH PRODL		E2		Decode	Read register 'f'	Process Data	Write registers PRODH:
After Instruct	ion						PRODL
W PRODH PRODL	= 0x	E2 AD 08		<u>Example</u> : Before Instru		REG	
				W REG PRODH PRODL	= 0x = 0x = ? = ?		
				After Instruc		C 4	

atter instruction		
W	=	0xC4
REG	=	0xB5
PRODH	=	0x8A
PRODL	=	0x94

TABLE 26-10:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER
AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Тур	Мах	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2	—	_	μS	
31	Twdt	Watchdog Timer Time-out Period (no postscaler)	3.48	4.00	4.71	ms	
32	Tost	Oscillation Start-up Timer Period	1024 Tosc		1024 Tosc	_	Tosc = OSC1 period
33	TPWRT	Power-up Timer Period	57.0	65.5	77.2	ms	
34	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	—	2	—	μS	
35	TBOR	Brown-out Reset Pulse Width	200	—	—	μS	$VDD \le BVDD$ (see D005A)
36	Tivrst	Time for Internal Reference Voltage to become stable	—	20	50	μS	
37	Tlvd	Low-Voltage Detect Pulse Width	200		_	μS	$VDD \leq VLVD$

FIGURE 26-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

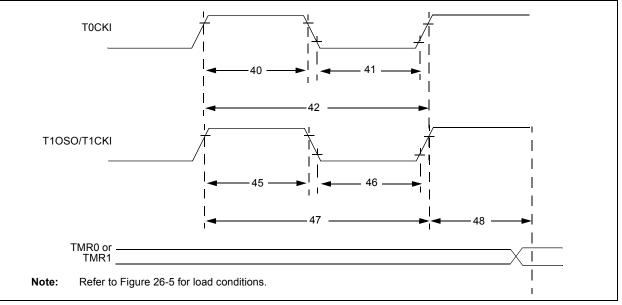


TABLE 26-24: A/D CONVERTER CHARACTERISTICS: PIC18F2220/2320/4220/4320 (INDUSTRIAL) PIC18F2220/2320/4220/4320 (EXTENDED) PIC18LF2220/2320/4220/4320 (INDUSTRIAL)

Param No.	Symbol	Charac	teristic	Min	Тур	Мах	Units	Conditions
A01	NR	Resolution				10	bit	$\Delta \text{VREF} \geq 3.0 \text{V}$
A03	EIL	Integral Linearit	y Error	_	_	<±1	LSb	$\Delta \text{VREF} \geq 3.0 \text{V}$
A04	Edl	Differential Line	arity Error	—	—	<±1	LSb	$\Delta V \text{REF} \geq 3.0 V$
A06	EOFF	Offset Error		—	_	<±1	LSb	$\Delta \text{VREF} \geq 3.0 \text{V}$
A07	Egn	Gain Error		—	—	<±1	LSb	$\Delta VREF \ge 3.0V$
A10	_	Monotonicity		gu	uarantee	d ⁽²⁾	_	
A20	$\Delta VREF$	Reference Voltage Range (VREFH – VREFL)		3	_	AVDD – AVSS	V	For 10-bit resolution
A21	Vrefh	Reference Volta	ige High	AVss + 3.0V	_	AVDD + 0.3V	V	For 10-bit resolution
A22	Vrefl	Reference Volta	ige Low	AVss – 0.3V	_	AVDD - 3.0V	V	For 10-bit resolution
A25	Vain	Analog Input Vo	ltage	VREFL	_	VREFH	V	
A28	AVdd	Analog Supply	Voltage	Vdd - 0.3	_	VDD + 0.3	V	Tie to VDD
A29	AVss	Analog Supply	Voltage	Vss – 0.3	_	Vss + 0.3	V	Tie to Vss
A30	ZAIN	Recommended Analog Voltage		—	_	2.5 ⁽⁴⁾	kΩ	
A40	IAD	A/D Current	PIC18 F XX20	—	_	180 ⁽⁵⁾	μA	Average current during
		from VDD	PIC18LFXX20	_		90 ⁽⁵⁾	μA	conversion ⁽¹⁾
A50	IREF	VREF Input Curr	ent ⁽³⁾	_	_	±5 ⁽⁵⁾ ±150 ⁽⁵⁾	μΑ μΑ	During VAIN acquisition. During A/D conversion cycle.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: VREFH current is from RA3/AN3/VREF+ pin or AVDD, whichever is selected as the VREFH source. VREFL current is from RA2/AN2/VREF- pin or AVSS, whichever is selected as the VREFL source.

4: Assume quiet environment. If adjacent pins have high-frequency signals (analog or digital), ZAIN may need to be reduced to as low as 1 k Ω to fight crosstalk effects.

5: For guidance only.

28.0 PACKAGING INFORMATION

28.1 Package Marking Information

28-Lead SPDIP

28-Lead SOIC



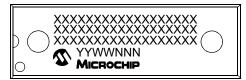
Example



Example



40-Lead PDIP



0

10710017

PIC18F2320-E/SO (e3)

Example



Legen	d: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	be carrie	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for customer-specific information.

INDEX

Α

A/D	211
A/D Converter Interrupt, Configuring	
Acquisition Requirements	
ADCON0 Register	
ADCON1 Register	
ADCON2 Register	
ADRESH Register21	
ADRESL Register	
Analog Port Pins, Configuring	218
Associated Registers	220
Automatic Acquisition Time	217
Configuring the Module	
Conversion Clock (Tad)	217
Conversion Status (GO/DONE Bit)	
Conversions	
Converter Characteristics	
Operation in Power-Managed Modes	
Special Event Trigger (CCP)13	
Use of the CCP2 Trigger	
Vref+ and Vref- References	
Absolute Maximum Ratings	
AC (Timing) Characteristics	326
Load Conditions for Device Timing	
Specifications	
Parameter Symbology	
Temperature and Voltage Specifications	
Timing Conditions	
Access Bank	
ACKSTAT Status Flag	
GO/DONE Bit	
ADCON1 Register ADCON2 Register	
ADDLW	
Addressable Universal Synchronous Asynchronous	205
Receiver Transmitter. See USART	
ADDWF	263
ADDWFC	
ADRESH Register	
ADRESL Register	
Analog-to-Digital Converter. See A/D.	,
ANDLW	264
ANDWF	
Assembler	
MPASM Assembler	302
В	
Bank Select Register (BSR)	65
Baud Rate Generator	181
PC	265

BC	
BCF	
BF Status Flag	185
Block Diagrams	
A/D	
Analog Input Model	
Baud Rate Generator	
Capture Mode Operation	135
Comparator I/O Operating Modes	
Comparator Output	
Comparator Voltage Reference	
Compare Mode Operation	136

External Power-on Reset Circuit	
(Slow VDD Power-up)	44
Fail-Safe Clock Monitor	249
Generic I/O Port Operation	
Interrupt Logic	. 88
Low-Voltage Detect (LVD)	232
Low-Voltage Detect (LVD) with External Input	232
MCLR/Vpp/RE3 Pin	
MSSP (I ² C Master Mode)	
MSSP (I ² C Mode)	164
MSSP (SPI Mode)	
On-Chip Reset Circuit	
PIC18F2220/2320	
PIC18F4220/4320	
PLL	
PORTC (Peripheral Output Override)	
PORTD and PORTE (Parallel Slave Port)	
PWM (Enhanced)	
PWM (Standard)	
RA3:RA0 and RA5 Pins	
RA4/T0CKI Pin	
RA6 Pin	
RA7 Pin	
RB2:RB0 Pins	
RB3/CCP2 Pin	
RB4 Pin	
RB7:RB5 Pins	
RD4:RD0 Pins	
RD7:RD5 Pins	
RE2:RE0 Pins	
Reads from Flash Program Memory	
System Clock	
Table Read Operation	
Table Write Operation	
Table Writes to Flash Program Memory	
Timer0 in 16-Bit Mode	
Timer0 in 8-Bit Mode	
Timero in 8-bit Mode	
Timer1 (16-Bit Read/Write Mode)	
Timer2	
Timer2	
Timer3 (16-Bit Read/Write Mode)	
USART Receive	
USART Transmit	
Watchdog Timer	
BN	240
BNC	
BNN	
BNN BNOV	
BNOV	
BOR. See Brown-out Reset.	200
BOV	271
BOV BRA	
BRG. See Baud Rate Generator.	209
Brown-out Reset (BOR)44,	727
BIOWII-OUL RESEL (BOR)	
BSFBTFSC	
BTFSC	
BTFSS	
BTGBTG	
	212

PORTD

Associated Registers	
LATD Register	
Parallel Slave Port (PSP) Function	
PORTD Register	
TRISD Register	
PORTE Analog Port Pins	110
-	
Associated Registers LATE Register	
PORTE Register	
PSP Mode Select (PSPMODE Bit)	
RE0/AN5/RD Pin	
RE1/AN6/WR Pin	
RE2/AN7/CS Pin	
TRISE Register	
Postscaler, WDT	
Assignment (PSA Bit)	
Rate Select (T0PS2:T0PS0 Bits)	119
Power-Managed Modes	
Entering	
Idle Modes	31
Run Modes	
Sleep Mode	31
Summary (table)	29
Wake from	
Power-on Reset (POR)	44, 237
Power-up Delays	
Power-up Timer (PWRT) 2	8, 44, 237
Prescaler, Capture	
Prescaler, Timer0	119
Assignment (PSA Bit)	119
Rate Select (T0PS2:T0PS0 Bits)	119
Prescaler, Timer2	119 139
Prescaler, Timer2 Product Identification System	119 139
Prescaler, Timer2 Product Identification System Program Counter	119 139 391
Prescaler, Timer2 Product Identification System Program Counter PCL Register	119 139 391 56
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory	119
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection	119 391 56 56 56 58 58 53 53 53 53 53 53 53 53
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification	119 391 56 56 56 58 58 53 53 53 53 53 53 53 53
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification Program Verification and Code Protection	119 391 56 56 56 56 58 53 53 53 53 53 53 53 253 252
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification Program Verification and Code Protection Associated Registers	119 391 391 56 56 56 58 53 53 53 53 53 53 53 53 53 53 53 53 53 53 52 54
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification and Code Protection Associated Registers Programming, Device Instructions	119 391 391 56 56 56 58 53 53 53 53 53 53 53 53 53 53 53 53 53 53 52 54
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification Program Verification and Code Protection Associated Registers Programming, Device Instructions PSP. See Parallel Slave Port.	119 391 391 56 56 56 58 53 53 53 53 53 53 53 53 53 53 53 53 53 53 52 54
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification and Code Protection Associated Registers Programming, Device Instructions PSP. See Parallel Slave Port. Pulse-Width Modulation. See PWM (CCP Module)	119 391 391 56 56 56 58 53 53 53 53 53 53 53 53 53 53 53 53 53 53 52 54
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification Program Verification and Code Protection Associated Registers Programming, Device Instructions PSP. See Parallel Slave Port.	119 391 391 56 56 56 58 53 53 53 53 53 53 53 252 252 252
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification Program Verification and Code Protection Associated Registers Programming, Device Instructions PSP. See Parallel Slave Port. Pulse-Width Modulation. See PWM (CCP Module) and PWM (ECCP Module).	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2220/4220 Program Memory Code Protection Program Memory Code Protection Program Verification and Code Protection Associated Registers Programming, Device Instructions PSP. See Parallel Slave Port. Pulse-Width Modulation. See PWM (CCP Module) and PWM (ECCP Module). PUSH PUSH and POP Instructions PWM (CCP Module)	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification and Code Protection Associated Registers Programming, Device Instructions PSP. See Parallel Slave Port. Pulse-Width Modulation. See PWM (CCP Module) and PWM (ECCP Module). PUSH PUSH and POP Instructions	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Memory Code Protection Program Verification and Code Protection Associated Registers PSP. See Parallel Slave Port. Pulse-Width Modulation. See PWM (CCP Module) and PWM (ECCP Module). PUSH PUSH and POP Instructions PWM (CCP Module) Associated Registers CCPR1H:CCPR1L Registers	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2220/4220 Reset Vector Program Memory Code Protection Program Memory Code Protection Program Verification and Code Protection Associated Registers PSP. See Parallel Slave Port. Pulse-Width Modulation. See PWM (CCP Module) and PWM (ECCP Module). PUSH PUSH and POP Instructions PWM (CCP Module) Associated Registers CCPR1H:CCPR1L Registers Duty Cycle	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification and Code Protection Associated Registers Programming, Device Instructions PSP. See Parallel Slave Port. Pulse-Width Modulation. See PWM (CCP Module) and PWM (ECCP Module). PUSH PUSH and POP Instructions PWM (CCP Module) Associated Registers CCPR1H:CCPR1L Registers Duty Cycle Example Frequencies/Resolutions	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification and Code Protection Associated Registers PSP. See Parallel Slave Port. Pulse-Width Modulation. See PWM (CCP Module) and PWM (ECCP Module). PUSH PUSH and POP Instructions PWM (CCP Module) Associated Registers CCPR1H:CCPR1L Registers Duty Cycle Example Frequencies/Resolutions Period	
Prescaler, Timer2 Product Identification System Program Counter PCL Register PCLATH Register PCLATU Register Program Memory Instructions Two-Word Interrupt Vector Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2220/4220 Map and Stack for PIC18F2320/4320 Reset Vector Program Memory Code Protection Program Verification and Code Protection Associated Registers Programming, Device Instructions PSP. See Parallel Slave Port. Pulse-Width Modulation. See PWM (CCP Module) and PWM (ECCP Module). PUSH PUSH and POP Instructions PWM (CCP Module) Associated Registers CCPR1H:CCPR1L Registers Duty Cycle Example Frequencies/Resolutions	

PWM (ECCP Module) Associated Registers	
Direction Change in Full-Bridge Output Mode	
Effects of a Reset Full-Bridge Application Example	147
Full-Bridge Mode Half-Bridge Mode	145
Half-Bridge Output Mode Applications Example Operation in Power-Managed Modes	152
Operation with Fail-Safe Clock Monitor Output Configurations	143
Output Relationships (Active-High State) Output Relationships (Active-Low State)	144
Programmable Dead-Band Delay Setup for Operation	152
Shoot-Through Current Start-up Considerations	

Q

Q Clock	139
Q Clock	139

R

RAM. See Data Memory.	
RC Oscillator	
RCIO Oscillator Mode	21
RCALL	287
RCON Register	
Bit Status During Initialization	45
Bits and Positions	45
RCSTA Register	
SPEN Bit	195
Reader Response	390
Register File	59
Registers	
ADCON0 (A/D Control 0)	211
ADCON1 (A/D Control 1)	212
ADCON2 (A/D Control 2)	213
CCP1CON (ECCP Control)	141
CCPxCON (CCPx Control)	133
CMCON (Comparator Control)	221
CONFIG1H (Configuration 1 High)	238
CONFIG2H (Configuration 2 High)	240
CONFIG2L (Configuration 2 Low)	
CONFIG3H (Configuration 3 High)	
CONFIG4L (Configuration 4 Low)	
CONFIG5H (Configuration 5 High)	
CONFIG5L (Configuration 5 Low)	242
CONFIG6H (Configuration 6 High)	
CONFIG6L (Configuration 6 Low)	
CONFIG7H (Configuration 7 High)	244
CONFIG7L (Configuration 7 Low)	244
CVRCON (Comparator Voltage	
Reference Control)	
DEVID1 (Device ID 1)	
DEVID2 (Device ID 2)	245
ECCPAS (Enhanced Capture/Compare/PWM	
Auto-Shutdown Control)	
EECON1 (Data EEPROM Control 1)	73, 82
INTCON (Interrupt Control)	89
INTCON2 (Interrupt Control 2)	90
INTCON3 (Interrupt Control 3)	
IPR1 (Peripheral Interrupt Priority 1)	
IPR2 (Peripheral Interrupt Priority 2)	97
LVDCON (Low-Voltage Detect Control)	233
OSCCON (Oscillator Control)	27