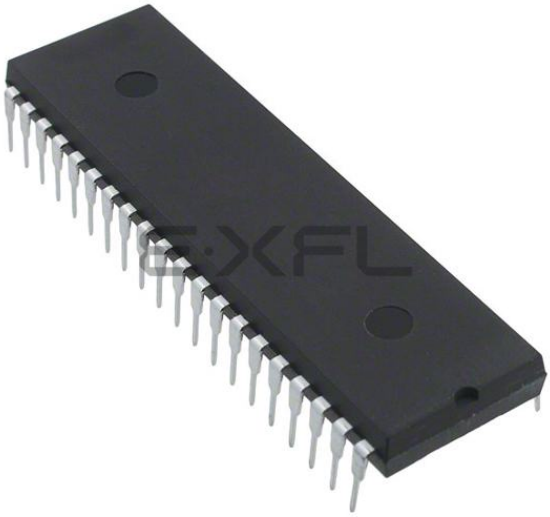

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f4320-i-p

NOTES:

TABLE 1-3: PIC18F4220/4320 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	TQFP	QFN			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0	33	8	9			
RB0				I/O	TTL	Digital I/O.
AN12				I	Analog	Analog input 12.
INT0				I	ST	External interrupt 0.
RB1/AN10/INT1	34	9	10			
RB1				I/O	TTL	Digital I/O.
AN10				I	Analog	Analog input 10.
INT1				I	ST	External interrupt 1.
RB2/AN8/INT2	35	10	11			
RB2				I/O	TTL	Digital I/O.
AN8				I	Analog	Analog input 8.
INT2				I	ST	External interrupt 2.
RB3/AN9/CCP2	36	11	12			
RB3				I/O	TTL	Digital I/O.
AN9				I	Analog	Analog input 9.
CCP2(1)				I/O	ST	Capture 2 input, Compare 2 output, PWM2 output.
RB4/AN11/KBI0	37	14	14			
RB4				I/O	TTL	Digital I/O.
AN11				I	Analog	Analog input 11.
KBI0				I	TTL	Interrupt-on-change pin.
RB5/KBI1/PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PGM				I/O	ST	Low-voltage ICSP™ programming enable pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power
OD = Open-drain (no diode to V_{DD})

Note 1: Alternate assignment for CCP2 when CCP2MX is cleared.
2: Default assignment for CCP2 when CCP2MX (CONFIG3H<0>) is set.

REGISTER 2-3: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R[(1)]	R-0	R/W-0	R/W-0
IDLEN	IRCF2	IRCF1	IRCF0	OSTS	IOFS	SCS1	SCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IDLEN:** Idle Enable bit
- 1 = Idle mode enabled; CPU core is not clocked in power-managed modes
- 0 = Run mode enabled; CPU core is clocked in power-managed modes

bit 6-4 **IRCF2:IRCF0:** Internal Oscillator Frequency Select bits
- 111 = 8 MHz (8 MHz source drives clock directly)
- 110 = 4 MHz
- 101 = 2 MHz
- 100 = 1 MHz
- 011 = 500 kHz
- 010 = 250 kHz
- 001 = 125 kHz
- 000 = 31 kHz (INTRC source drives clock directly)

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit[(1)]
- 1 = Oscillator Start-up Timer time-out has expired; primary oscillator is running
- 0 = Oscillator Start-up Timer time-out is running; primary oscillator is not ready

bit 2 **IOFS:** INTOSC Frequency Stable bit
- 1 = INTOSC frequency is stable
- 0 = INTOSC frequency is not stable

bit 1-0 **SCS1:SCS0:** System Clock Select bits
- 1x = Internal oscillator block (RC modes)
- 01 = Timer1 oscillator (Secondary modes)[(2)]
- 00 = Primary oscillator (Sleep and PRI_IDLE modes)

Note 1: Depends on state of IESO bit in Configuration Register 1H.

2: SCS0 may not be set while T1OSCEN (T1CON<3>) is clear.

3.0 POWER-MANAGED MODES

The PIC18F2X20 and PIC18F4X20 devices offer a total of six operating modes for more efficient power management (see Table 3-1). These operating modes provide a variety of options for selective power conservation in applications where resources may be limited (i.e., battery-powered devices).

There are three categories of power-managed modes:

- Sleep mode
- Idle modes
- Run modes

These categories define which portions of the device are clocked and sometimes, what speed. The Run and Idle modes may use any of the three available clock sources (primary, secondary or INTOSC multiplexer); the Sleep mode does not use a clock source.

The clock switching feature offered in other PIC18 devices (i.e., using the Timer1 oscillator in place of the primary oscillator) and the Sleep mode offered by all PIC® devices (where all system clocks are stopped) are both offered in the PIC18F2X20/4X20 devices (SEC_RUN and Sleep modes, respectively). However, additional power-managed modes are available that allow the user greater flexibility in determining what portions of the device are operating. The power-managed modes are event driven; that is, some specific event must occur for the device to enter or (more particularly) exit these operating modes.

For PIC18F2X20/4X20 devices, the power-managed modes are invoked by using the existing `SLEEP` instruction. All modes exit to PRI_RUN mode when triggered by an interrupt, a Reset, or a WDT time-out (PRI_RUN mode is the normal full-power execution mode; the CPU and peripherals are clocked by the primary oscillator source). In addition, power-managed Run modes may also exit to Sleep mode or their corresponding Idle mode.

3.1 Selecting Power-Managed Modes

Selecting a power-managed mode requires deciding if the CPU is to be clocked or not and selecting a clock source. The IDLEN bit controls CPU clocking while the SC1:SCS0 bits select a clock source. The individual modes, bit settings, clock sources and affected modules are summarized in Table 3-1.

3.1.1 CLOCK SOURCES

The clock source is selected by setting the SCS bits of the OSCCON register. Three clock sources are available for use in power-managed Idle modes: the primary clock (as configured in Configuration Register 1H), the secondary clock (Timer1 oscillator) and the internal oscillator block. The secondary and internal oscillator block sources are available for the power-managed modes (PRI_RUN mode is the normal full-power execution mode; the CPU and peripherals are clocked by the primary oscillator source).

TABLE 3-1: POWER-MANAGED MODES

Mode	OSCCON<7,1:0>		Module Clocking		Available Clock and Oscillator Source
	IDLEN	SCS1:SCS0	CPU	Peripherals	
Sleep	0	00	Off	Off	None – All clocks are disabled
PRI_RUN	0	00	Clocked	Clocked	Primary – LP, XT, HS, HSPLL, RC, EC, INTRC(1). This is the normal full-power execution mode.
SEC_RUN	0	01	Clocked	Clocked	Secondary – Timer1 Oscillator
RC_RUN	0	1x	Clocked	Clocked	Internal Oscillator Block(1)
PRI_IDLE	1	00	Off	Clocked	Primary – LP, XT, HS, HSPLL, RC, EC
SEC_IDLE	1	01	Off	Clocked	Secondary – Timer1 Oscillator
RC_IDLE	1	1x	Off	Clocked	Internal Oscillator Block(1)

Note 1: Includes INTOSC and INTOSC postscaler, as well as the INTRC source.

3.1.2 ENTERING POWER-MANAGED MODES

In general, entry, exit and switching between power-managed clock sources requires clock source switching. In each case, the sequence of events is the same.

Any change in the power-managed mode begins with loading the OSCCON register and executing a SLEEP instruction. The SCS1:SCS0 bits select one of three power-managed clock sources; the primary clock (as defined in Configuration Register 1H), the secondary clock (the Timer1 oscillator) and the internal oscillator block (used in RC modes). Modifying the SCS bits will have no effect until a SLEEP instruction is executed. Entry to the power-managed mode is triggered by the execution of a SLEEP instruction.

Figure 3-5 shows how the system is clocked while switching from the primary clock to the Timer1 oscillator. When the SLEEP instruction is executed, clocks to the device are stopped at the beginning of the next instruction cycle. Eight clock cycles from the new clock source are counted to synchronize with the new clock source. After eight clock pulses from the new clock source are counted, clocks from the new clock source resume clocking the system. The actual length of the pause is between eight and nine clock periods from the new clock source. This ensures that the new clock source is stable and that its pulse width will not be less than the shortest pulse width of the two clock sources.

Three bits indicate the current clock source: OSTS and IOFS in the OSCCON register and T1RUN in the T1CON register. Only one of these bits will be set while in a power-managed mode other than PRI_RUN. When the OSTS bit is set, the primary clock is providing the system clock. When the IOFS bit is set, the INTOSC output is providing a stable 8 MHz clock source and is providing the system clock. When the T1RUN bit is set, the Timer1 oscillator is providing the system clock. If none of these bits are set, then either the INTRC clock source is clocking the system or the INTOSC source is not yet stable.

If the internal oscillator block is configured as the primary clock source in Configuration Register 1H, then both the OSTS and IOFS bits may be set when in PRI_RUN or PRI_IDLE modes. This indicates that the primary clock (INTOSC output) is generating a stable 8 MHz output. Entering a power-managed RC mode (same frequency) would clear the OSTS bit.

Note 1: Caution should be used when modifying a single IRCF bit. If V_{DD} is less than 3V, it is possible to select a higher clock speed than is supported by the low V_{DD}. Improper device operation may result if the V_{DD}/F_{OSC} specifications are violated.

2: Executing a SLEEP instruction does not necessarily place the device into Sleep mode; executing a SLEEP instruction is simply a trigger to place the controller into a power-managed mode selected by the OSCCON register, one of which is Sleep mode.

3.1.3 MULTIPLE SLEEP COMMANDS

The power-managed mode that is invoked with the SLEEP instruction is determined by the settings of the IDLEN and SCS bits at the time the instruction is executed. If another SLEEP instruction is executed, the device will enter the power-managed mode specified by these same bits at that time. If the bits have changed, the device will enter the new power-managed mode specified by the new bit settings.

3.1.4 COMPARISONS BETWEEN RUN AND IDLE MODES

Clock source selection for the Run modes is identical to the corresponding Idle modes. When a SLEEP instruction is executed, the SCS bits in the OSCCON register are used to switch to a different clock source. As a result, if there is a change of clock source at the time a SLEEP instruction is executed, a clock switch will occur.

In Idle modes, the CPU is not clocked and is not running. In Run modes, the CPU is clocked and executing code. This difference modifies the operation of the WDT when it times out. In Idle modes, a WDT time-out results in a wake from power-managed modes. In Run modes, a WDT time-out results in a WDT Reset (see Table 3-2).

During a wake-up from an Idle mode, the CPU starts executing code by entering the corresponding Run mode until the primary clock becomes ready. When the primary clock becomes ready, the clock source is automatically switched to the primary clock. The IDLEN and SCS bits are unchanged during and after the wake-up.

Figure 3-2 shows how the system is clocked during the clock source switch. The example assumes the device was in SEC_IDLE or SEC_RUN mode when a wake is triggered (the primary clock was configured in HSPLL mode).

5.9.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 5-1 and Table 5-2.

The SFRs can be classified into two sets: those associated with the "core" function and those related to the peripheral functions. Those registers related to the "core" are described in this section, while those related to the operation of the peripheral features are described in the section of that peripheral feature.

The SFRs are typically distributed among the peripherals whose functions they control.

The unused SFR locations will be unimplemented and read as '0's.

TABLE 5-1: SPECIAL FUNCTION REGISTER MAP FOR PIC18F2X20/4X20 DEVICES

Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2(2)	FBFh	CCPR1H	F9Fh	IPR1
FFEh	TOSH	FDEh	POSTINC2(2)	FBEh	CCPR1L	F9Eh	PIR1
FFDh	TOSL	FDDh	POSTDEC2(2)	FBDh	CCP1CON	F9Dh	PIE1
FFCh	STKPTR	FDCh	PREINC2(2)	FBCh	CCPR2H	F9Ch	—
FFBh	PCLATU	FDBh	PLUSW2(2)	FBBh	CCPR2L	F9Bh	OSCTUNE
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	OSCTUN2
FF9h	PCL	FD9h	FSR2L	FB9h	—	F99h	—
FF8h	TBLPTRU	FD8h	STATUS	FB8h	—	F98h	—
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	PWM1CON(1)	F97h	—
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	ECCPAS(1)	F96h	TRISE(1)
FF5h	TABLAT	FD5h	T0CON	FB5h	CVRCON	F95h	TRISD(1)
FF4h	PRODH	FD4h	—	FB4h	CMCON	F94h	TRISC
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB
FF2h	INTCON	FD2h	LVDCON	FB2h	TMR3L	F92h	TRISA
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	—
FF0h	INTCON3	FD0h	RCON	FB0h	—	F90h	—
FEFh	INDF0(2)	FCFh	TMR1H	FAFh	SPBRG	F8Fh	—
FEEh	POSTINC0(2)	FCEh	TMR1L	FAEh	RCREG	F8Eh	—
FEDh	POSTDEC0(2)	FCDh	T1CON	FADh	TXREG	F8Dh	LATE(1)
FECh	PREINC0(2)	FCCh	TMR2	FACh	TXSTA	F8Ch	LATD(1)
FEBh	PLUSW0(2)	FCBh	PR2	FABh	RCSTA	F8Bh	LATC
FEAh	FSR0H	FCAh	T2CON	FAAh	—	F8Ah	LATB
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	—
FE7h	INDF1(2)	FC7h	SSPSTAT	FA7h	EECON2	F87h	—
FE6h	POSTINC1(2)	FC6h	SSPCON1	FA6h	EECON1	F86h	—
FE5h	POSTDEC1(2)	FC5h	SSPCON2	FA5h	—	F85h	—
FE4h	PREINC1(2)	FC4h	ADRESH	FA4h	—	F84h	PORTE(1)
FE3h	PLUSW1(2)	FC3h	ADRESL	FA3h	—	F83h	PORTD(1)
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA

Legend: — = Unimplemented registers, read as '0'.

Note 1: This register is not available on PIC18F2X20 devices.

2: This is not a physical register.

7.7 Operation During Code-Protect

Data EEPROM memory has its own code-protect bits in Configuration Words. External read and write operations are disabled if either of these mechanisms are enabled.

The microcontroller itself can both read and write to the internal Data EEPROM regardless of the state of the code-protect Configuration bit. Refer to **Section 23.0 "Special Features of the CPU"** for additional information.

7.8 Using the Data EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). Frequently changing values will typically be updated more often than specification D124 or D124A. If this is not the case, an array refresh must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

A simple data EEPROM refresh routine is shown in Example 7-3.

Note:	If data EEPROM is only used to store constants and/or data that changes rarely, an array refresh is likely not required. See specification D124 or D124A.

EXAMPLE 7-3: DATA EEPROM REFRESH ROUTINE

```
        CLRF    EEADR                   ; Start at address 0
        BCF     EECON1, CFGS            ; Set for memory
        BCF     EECON1, EEPGD           ; Set for Data EEPROM
        BCF     INTCON, GIE             ; Disable interrupts
        BSF     EECON1, WREN            ; Enable writes
LOOP                                    ; Loop to refresh array
        BSF     EECON1, RD              ; Read current address
        MOVLW   55h                     ;
        MOVWF   EECON2                  ; Write 55h
        MOVLW   AAh                     ;
        MOVWF   EECON2                  ; Write AAh
        BSF     EECON1, WR              ; Set WR bit to begin write
        BTFSC   EECON1, WR              ; Wait for write to complete
        BRA     $-2
        INCFSZ  EEADR, F                ; Increment address
        BRA     Loop                    ; Not zero, do it again

        BCF     EECON1, WREN            ; Disable writes
        BSF     INTCON, GIE             ; Enable interrupts
```

TABLE 7-1: REGISTERS ASSOCIATED WITH DATA EEPROM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
EEADR	EEPROM Address Register								0000 0000	0000 0000
EEDATA	EEPROM Data Register								0000 0000	0000 0000
EECON2	EEPROM Control Register 2 (not a physical register)								—	—
EECON1	EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD	xx-0 x000	uu-0 u000
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP	11-1 1111	---1 1111
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	LVDIF	TMR3IF	CCP2IF	00-0 0000	---0 0000
PIE2	OSCFIE	CMIE	—	EEIE	BCLIE	LVDIE	TMR3IE	CCP2IE	00-0 0000	---0 0000

Legend: x = unknown, u = unchanged, r = reserved, - = unimplemented, read as '0'.
Shaded cells are not used during Flash/EEPROM access.

14.2 Timer1 Oscillator

The Timer1 oscillator may be used as the clock source for Timer3. The Timer1 oscillator is enabled by setting the T1OSCEN (T1CON<3>) bit. The oscillator is a low-power oscillator rated for 32 kHz crystals. See **Section 12.2 "Timer1 Oscillator"** for further details.

14.3 Timer3 Interrupt

The TMR3 register pair (TMR3H:TMR3L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR3 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR3IF (PIR2<1>). This interrupt can be enabled/disabled by setting/clearing TMR3 Interrupt Enable bit, TMR3IE (PIE2<1>).

14.4 Resetting Timer3 Using a CCP Trigger Output

If the CCP module is configured in Compare mode to generate a "Special Event Trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer3. See **Section 15.4.4 "Special Event Trigger"** for more information.

Note:	The Special Event Triggers from the CCP module will not set interrupt flag bit, TMR3IF (PIR1<0>).

Timer3 must be configured for either Timer or Synchronized Counter mode to take advantage of this feature. If Timer3 is running in Asynchronous Counter mode, this Reset operation may not work. In the event that a write to Timer3 coincides with a Special Event Trigger from CCP1, the write will take precedence. In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer3.

TABLE 14-1: REGISTERS ASSOCIATED WITH TIMER3 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR2	OSCIF	CMIF	—	EEIF	BCLIF	LVDIF	TMR3IF	CCP2IF	00-0 0000	00-0 0000
PIE2	OSCIE	CMIE	—	EEIE	BCLIE	LVDIE	TMR3IE	CCP2IE	00-0 0000	00-0 0000
IPR2	OSCIP	CMIP	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP	11-1 1111	11-1 1111
TMR3L	Timer3 Low Byte Register								xxxx xxxx	uuuu uuuu
TMR3H	Timer3 High Byte Register								xxxx xxxx	uuuu uuuu
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	u0uu uuuu
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	$\overline{\text{T3SYNC}}$	TMR3CS	TMR3ON	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer3 module.

15.1 CCP1 Module

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

TABLE 15-1: CCP MODE - TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2

15.2 CCP2 Module

Capture/Compare/PWM Register 2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. All are readable and writable.

CCP2 functions identically to CCP1 except for the enhanced PWM modes offered by CCP2

TABLE 15-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	TMR1 or TMR3 time base. Time base can be different for each CCP.
Capture	Compare	The compare could be configured for the Special Event Trigger which clears either TMR1 or TMR3 depending upon which time base is used.
Compare	Compare	The compare(s) could be configured for the Special Event Trigger which clears TMR1 or TMR3 depending upon which time base is used.
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt).
PWM	Capture	None.
PWM	Compare	None.

REGISTER 17-3: SSPSTAT: MSSP STATUS REGISTER (I²C™ MODE)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P(1)	S(2)	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SMP:** Slew Rate Control bit

In Master or Slave mode:
1 = Slew rate control disabled
0 = Slew rate control enabled

bit 6 **CKE:** SMBus Select bit

In Master or Slave mode:
1 = Enable SMBus specific inputs
0 = Disable SMBus specific inputs

bit 5 **D/$\overline{A}$:** Data/$\overline{\text{Address}}$ bit

In Master mode:
Reserved.

In Slave mode:
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** Stop bit(1)

1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last

bit 3 **S:** Start bit(2)

1 = Indicates that a Start bit has been detected last
0 = Start bit was not detected last

bit 2 **R/$\overline{W}$:** Read/$\overline{\text{Write}}$ bit Information (I²C mode only)

In Slave mode:(3)
1 = Read
0 = Write

In Master mode:(4)
1 = Transmit is in progress
0 = Transmit is not in progress

bit 1 **UA:** Update Address bit (10-Bit Slave mode only)

1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0 **BF:** Buffer Full Status bit

In Transmit mode:
1 = Data transmit in progress (does not include the $\overline{\text{ACK}}$ and Stop bits), SSPBUF is full
0 = Data transmit complete (does not include the $\overline{\text{ACK}}$ and Stop bits), SSPBUF is empty

In Receive mode:
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

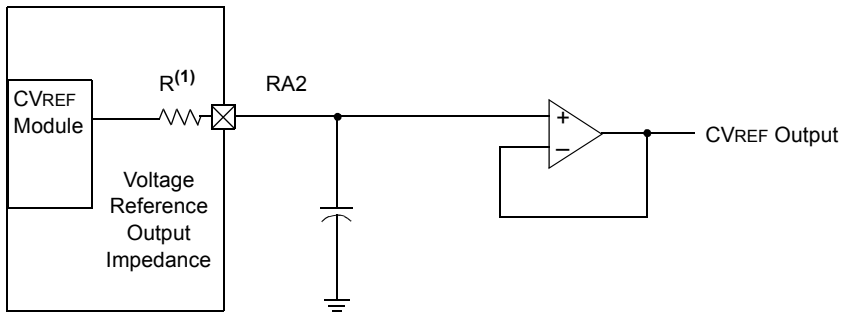
Note 1: This bit is cleared on Reset when SSPEN is cleared or a Start bit has been detected.

2: This bit is cleared on Reset when SSPEN is cleared or a Stop bit has been detected.

3: This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not $\overline{\text{ACK}}$ bit.

4: ORing this bit with the SSPCON2 bits, SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.

FIGURE 21-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



Note 1: R is dependent upon the voltage reference configuration bits (CVRCON<3:0> and CVRCON<5>).

TABLE 21-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111
TRISA	RA7(1)	RA6(1)	RA5	RA4	RA3	RA2	RA1	RA0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'.
Shaded cells are not used with the comparator voltage reference.

Note 1: These pins are enabled based on oscillator configuration (see Configuration Register 1H).

TABLE 24-2: PIC18FXXX INSTRUCTION SET (CONTINUED)

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word MSb LSb	Status Affected	Notes
LITERAL OPERATIONS						
ADDLW	k	Add Literal and WREG	1	0000 1111 kkkk kkkk	C, DC, Z, OV, N	
ANDLW	k	AND Literal with WREG	1	0000 1011 kkkk kkkk	Z, N	
IORLW	k	Inclusive OR Literal with WREG	1	0000 1001 kkkk kkkk	Z, N	
LFSR	f, k	Move Literal (12-bit) 2nd word to FSRx 1st word	2	1110 1110 00ff kkkk 1111 0000 kkkk kkkk	None	
MOVLB	k	Move Literal to BSR<3:0>	1	0000 0001 0000 kkkk	None	
MOVLW	k	Move Literal to WREG	1	0000 1110 kkkk kkkk	None	
MULLW	k	Multiply Literal with WREG	1	0000 1101 kkkk kkkk	None	
RETLW	k	Return with Literal in WREG	2	0000 1100 kkkk kkkk	None	
SUBLW	k	Subtract WREG from Literal	1	0000 1000 kkkk kkkk	C, DC, Z, OV, N	
XORLW	k	Exclusive OR Literal with WREG	1	0000 1010 kkkk kkkk	Z, N	
DATA MEMORY ↔ PROGRAM MEMORY OPERATIONS						
TBLRD*		Table Read	2	0000 0000 0000 1000	None	
TBLRD*+		Table Read with Post-Increment		0000 0000 0000 1001	None	
TBLRD*-		Table Read with Post-Decrement		0000 0000 0000 1010	None	
TBLRD+*		Table Read with Pre-Increment		0000 0000 0000 1011	None	
TBLWT*		Table Write	2 (5)	0000 0000 0000 1100	None	
TBLWT*+		Table Write with Post-Increment		0000 0000 0000 1101	None	
TBLWT*-		Table Write with Post-Decrement		0000 0000 0000 1110	None	
TBLWT+*		Table Write with Pre-Increment		0000 0000 0000 1111	None	

Note 1: When a PORT register is modified as a function of itself (e.g., `MOVF PORTB, 1, 0`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

4: Some instructions are 2-word instructions. The second word of these instructions will be executed as a `NOP` unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

5: If the table write starts the write cycle to internal memory, the write will continue until terminated.

INCFSZ **Increment f, Skip if 0**

Syntax: [*label*] INCFSZ f [,d [,a]]

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) + 1 → dest,
skip if result = 0

Status Affected: None

Encoding:

0011	11da	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default).
If the result is '0', the next instruction which is already fetched is discarded and a NOP is executed instead, making it a two-cycle instruction. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    INCFSZ   CNT
NZERO   :
ZERO    :
```

Before Instruction
PC = Address (HERE)

After Instruction
CNT = CNT + 1
If CNT = 0;
PC = Address (ZERO)
If CNT ≠ 0;
PC = Address (NZERO)

INFSNZ **Increment f, Skip if Not 0**

Syntax: [*label*] INFSNZ f [,d [,a]]

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f) + 1 → dest,
skip if result ≠ 0

Status Affected: None

Encoding:

0100	10da	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default).
If the result is not '0', the next instruction which is already fetched is discarded and a NOP is executed instead, making it a two-cycle instruction. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    INFSNZ   REG
ZERO
NZERO
```

Before Instruction
PC = Address (HERE)

After Instruction
REG = REG + 1
If REG ≠ 0;
PC = Address (NZERO)
If REG = 0;
PC = Address (ZERO)

RCALL **Relative Call**

Syntax: [*label*] RCALL n

Operands: $-1024 \le n \le 1023$

Operation: $(PC) + 2 \rightarrow TOS$,
$(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding:

1101	1nnn	nnnn	nnnn

Description: Subroutine call with a jump up to 1K from the current location. First, return address (PC+2) is pushed onto the stack. Then, add the 2's complement number '2n' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is a two-cycle instruction.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'n' Push PC to stack	Process Data	Write to PC
No operation	No operation	No operation	No operation

Example: `HERE RCALL Jump`

Before Instruction
PC = Address `(HERE)`

After Instruction
PC = Address `(Jump)`
TOS = Address `(HERE + 2)`

RESET **Reset**

Syntax: [*label*] RESET

Operands: None

Operation: Reset all registers and flags that are affected by a $\overline{\text{MCLR}}$ Reset.

Status Affected: All

Encoding:

0000	0000	1111	1111

Description: This instruction provides a way to execute a $\overline{\text{MCLR}}$ Reset in software.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Start reset	No operation	No operation

Example: `RESET`

After Instruction
Registers = Reset Value
Flags* = Reset Value

TSTFSZ **Test f, Skip if 0**

Syntax: [*label*] TSTFSZ f [,a]

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: skip if f = 0

Status Affected: None

Encoding:

0110	011a	ffff	ffff

Description: If 'f' = 0, the next instruction, fetched during the current instruction execution is discarded and a NOP is executed, making this a two-cycle instruction. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value (default).

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    TSTFSZ  CNT
NZERO     :
ZERO    :
```

Before Instruction
PC = Address (HERE)

After Instruction
If CNT = 0x00,
PC = Address (ZERO)
If CNT ≠ 0x00,
PC = Address (NZERO)

XORLW **Exclusive OR Literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → W

Status Affected: N, Z

Encoding:

0000	1010	kkkk	kkkk

Description: The contents of W are XOR'ed with the 8-bit literal 'k'. The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

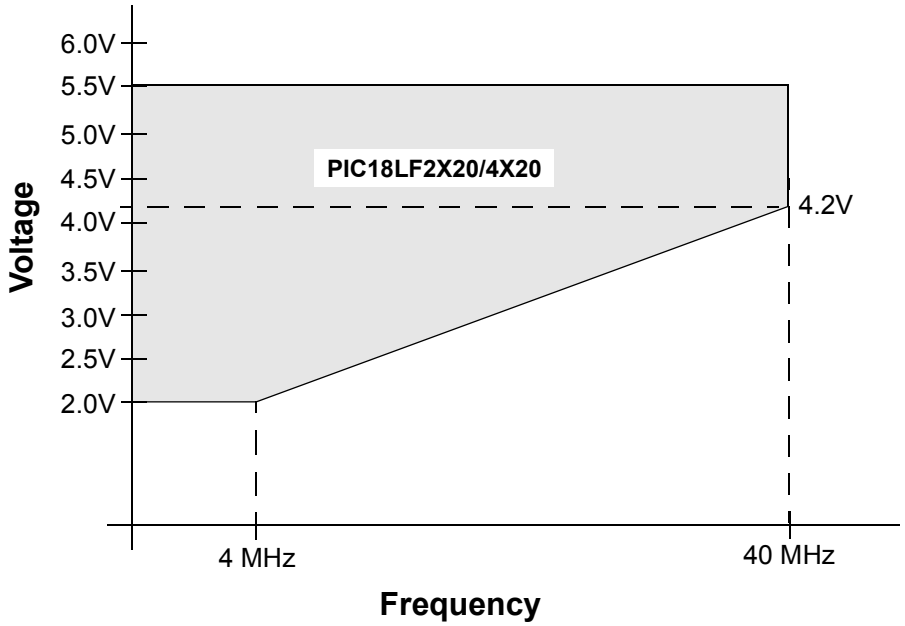
Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example:
```
XORLW 0xAF
```

Before Instruction
W = 0xB5

After Instruction
W = 0x1A

FIGURE 26-3: PIC18LF2220/2320/4220/4320 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



FMAX = (16.36 MHz/V) (VDDAPPMIN – 2.0V) + 4 MHz

Note: VDDAPPMIN is the minimum voltage of the PIC® device in the application.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2220/2320/4220/4320 (Industrial) PIC18LF2220/2320/4220/4320 (Industrial) (Continued)

PIC18LF2220/2320/4220/4320 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2220/2320/4220/4320 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD)(2,3)						
	All devices	3.1	4.1	mA	-40°C	VDD = 4.2 V	FOSC = 40 MHz (**PRI_IDLE** mode, EC oscillator)
		3.2	4.1	mA	+25°C		
		3.3	4.1	mA	+85°C		
	All devices	4.4	5.1	mA	-40°C	VDD = 5.0V	
		4.6	5.1	mA	+25°C		
		4.6	5.1	mA	+85°C		
	PIC18LF2X20/4X20	9	15	µA	-40°C	VDD = 2.0V	FOSC = 32 kHz(4) (**SEC_RUN** mode, Timer1 as clock)
		10	15	µA	+25°C		
		13	18	µA	+85°C		
	PIC18LF2X20/4X20	22	30	µA	-40°C	VDD = 3.0V	
		21	30	µA	+25°C		
		20	35	µA	+85°C		
	All devices	50	80	µA	-40°C	VDD = 5.0V	
		50	80	µA	+25°C		
		45	85	µA	+85°C		
	PIC18LF2X20/4X20	5.1	9	µA	-40°C	VDD = 2.0V	FOSC = 32 kHz(4) (**SEC_IDLE** mode, Timer1 as clock)
		5.8	9	µA	+25°C		
		7.9	11	µA	+85°C		
	PIC18LF2X20/4X20	7.9	12	µA	-40°C	VDD = 3.0V	
		8.9	12	µA	+25°C		
		10.5	14	µA	+85°C		
	All devices	13	20	µA	-40°C	VDD = 5.0V	
		16	20	µA	+25°C		
		18	25	µA	+85°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

4: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

TABLE 26-4: LOW-VOLTAGE DETECT CHARACTERISTICS (CONTINUED)

PIC18LF2220/2320/4220/4320 (Industrial)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2220/2320/4220/4320 (Industrial, Extended)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VLVD	LVD Voltage on VDD Transition High-to-Low — **Date codes above 0417xxx**						
D420D		PIC18LF2X20/4X20		Industrial Low Voltage (-10°C to +85°C)				
			LVDL<3:0> = 0000	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0001	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0010	2.08	2.26	2.44	V	
			LVDL<3:0> = 0011	2.26	2.45	2.65	V	
			LVDL<3:0> = 0100	2.35	2.55	2.76	V	
			LVDL<3:0> = 0101	2.55	2.77	2.99	V	
			LVDL<3:0> = 0110	2.64	2.87	3.10	V	
			LVDL<3:0> = 0111	2.82	3.07	3.31	V	
			LVDL<3:0> = 1000	3.09	3.36	3.63	V	
			LVDL<3:0> = 1001	3.29	3.57	3.86	V	
			LVDL<3:0> = 1010	3.38	3.67	3.96	V	
			LVDL<3:0> = 1011	3.56	3.87	4.18	V	
			LVDL<3:0> = 1100	3.75	4.07	4.40	V	
			LVDL<3:0> = 1101	3.93	4.28	4.62	V	
			LVDL<3:0> = 1110	4.23	4.60	4.96	V	
D420F		PIC18LF2X20/4X20		Industrial Low Voltage (-40°C to -10°C)				
			LVDL<3:0> = 0000	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0001	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0010	1.99	2.26	2.53	V	
			LVDL<3:0> = 0011	2.16	2.45	2.75	V	
			LVDL<3:0> = 0100	2.25	2.55	2.86	V	
			LVDL<3:0> = 0101	2.43	2.77	3.10	V	
			LVDL<3:0> = 0110	2.53	2.87	3.21	V	
			LVDL<3:0> = 0111	2.70	3.07	3.43	V	
			LVDL<3:0> = 1000	2.96	3.36	3.77	V	
			LVDL<3:0> = 1001	3.14	3.57	4.00	V	
			LVDL<3:0> = 1010	3.23	3.67	4.11	V	
			LVDL<3:0> = 1011	3.41	3.87	4.34	V	
			LVDL<3:0> = 1100	3.58	4.07	4.56	V	
			LVDL<3:0> = 1101	3.76	4.28	4.79	V	
			LVDL<3:0> = 1110	4.04	4.60	5.15	V	

Legend: Shading of rows is to assist in readability of the table.

† Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

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Device: PIC18F2220/2320/4220/4320 Literature Number: DS39599G

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PIC18F2220/2320/4220/4320 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	X	/XX	XXX
Device		Temperature Range	Package	Pattern

Device	PIC18F2220/2320/4220/4320(1), PIC18F2220/2320/4220/4320T(1,2); VDD range 4.2V to 5.5V PIC18LF2220/2320/4220/4320(1), PIC18LF2220/2320/4220/4320T(1,2); VDD range 2.0V to 5.5V
Temperature Range	I = -40°C to +85°C (Industrial)
Package	PT = TQFP (Thin Quad Flatpack) SO = SOIC SP = Skinny Plastic DIP P = PDIP ML = QFN
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18LF4320-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.

b) PIC18LF2220-I/SO = Industrial temp., SOIC package, Extended VDD limits.

c) PIC18F4220-I/P = Industrial temp., PDIP package, normal VDD limits.

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range

2: T = in tape and reel – SOIC and TQFP packages only.