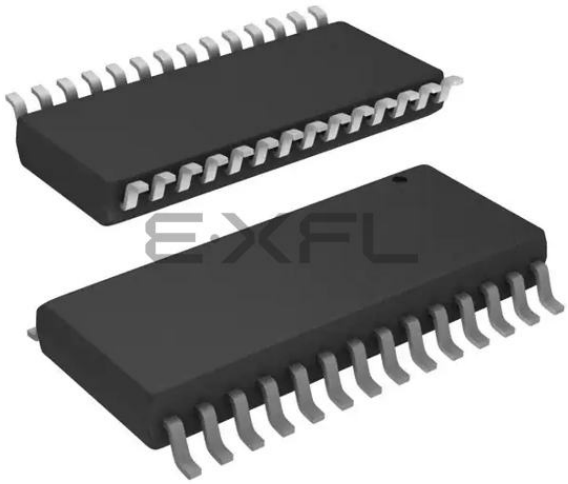

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf2320-i-so

TABLE 1-2: PIC18F2220/2320 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PDIP	SOIC			
					PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	11	11			
RC0			I/O	ST	Digital I/O.
T1OSO			O	—	Timer1 oscillator output.
T1CKI			I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	12	12			
RC1			I/O	ST	Digital I/O.
T1OSI			I	CMOS	Timer1 oscillator input.
CCP2(2)			I/O	ST	Capture 2 input, Compare 2 output, PWM2 output.
RC2/CCP1/P1A	13	13			
RC2			I/O	ST	Digital I/O.
CCP1			I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
P1A			O	—	Enhanced CCP1 output.
RC3/SCK/SCL	14	14			
RC3			I/O	ST	Digital I/O.
SCK			I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL			I/O	ST	Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI/SDA	15	15			
RC4			I/O	ST	Digital I/O.
SDI			I	ST	SPI data in.
SDA			I/O	ST	I^2C data I/O.
RC5/SDO	16	16			
RC5			I/O	ST	Digital I/O.
SDO			O	—	SPI data out.
RC6/TX/CK	17	17			
RC6			I/O	ST	Digital I/O.
TX			O	—	USART asynchronous transmit.
CK			I/O	ST	USART synchronous clock (see related RX/DT).
RC7/RX/DT	18	18			
RC7			I/O	ST	Digital I/O.
RX			I	ST	USART asynchronous receive.
DT			I/O	ST	USART synchronous data (see related TX/CK).
VSS	8, 19	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	20	P	—	Positive supply for logic and I/O pins.

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power
OD = Open-drain (no diode to VDD)

Note 1: Alternate assignment for CCP2 when CCP2MX is cleared.

2: Default assignment for CCP2 when CCP2MX (CONFIG3H<0>) is set.

3.4 Run Modes

If the IDLEN bit is clear when a SLEEP instruction is executed, the CPU and peripherals are both clocked from the source selected using the SCS1:SCS0 bits. While these operating modes may not afford the power conservation of Idle or Sleep modes, they do allow the device to continue executing instructions by using a lower frequency clock source. RC_RUN mode also offers the possibility of executing code at a frequency greater than the primary clock.

Wake-up from a power-managed Run mode can be triggered by an interrupt, or any Reset, to return to full-power operation. As the CPU is executing code in Run modes, several additional exits from Run modes are possible. They include exit to Sleep mode, exit to a corresponding Idle mode, and exit by executing a RESET instruction. While the device is in any of the power-managed Run modes, a WDT time-out will result in a WDT Reset.

3.4.1 PRI_RUN MODE

The PRI_RUN mode is the normal full-power execution mode. If the SLEEP instruction is never executed, the microcontroller operates in this mode (a SLEEP instruction is executed to enter all other power-managed modes). All other power-managed modes exit to PRI_RUN mode when an interrupt or WDT time-out occur.

There is no entry to PRI_RUN mode. The OSTS bit is set. The IOFS bit may be set if the internal oscillator block is the primary clock source (see **Section 2.7.1 "Oscillator Control Register"**).

3.4.2 SEC_RUN MODE

The SEC_RUN mode is the compatible mode to the "clock switching" feature offered in other PIC18 devices. In this mode, the CPU and peripherals are clocked from the Timer1 oscillator. This gives users the option of lower power consumption while still using a high-accuracy clock source.

SEC_RUN mode is entered by clearing the IDLEN bit, setting SCS1:SCS0 = 01 and executing a SLEEP instruction. The system clock source is switched to the Timer1 oscillator (see Figure 3-9), the primary oscillator is shut down, the T1RUN bit (T1CON<6>) is set and the OSTS bit is cleared.

Note:	The Timer1 oscillator should already be running prior to entering SEC_RUN mode. **If the T1OSCEN bit is not set when trying to set the SCS0 bit, the write to SCS0 will not occur.** If the Timer1 oscillator is enabled, but not yet running, system clocks will be delayed until the oscillator has started; in such situations, initial oscillator operation is far from stable and unpredictable operation may result.

When a wake-up event occurs, the peripherals and CPU continue to be clocked from the Timer1 oscillator while the primary clock is started. When the primary clock becomes ready, a clock switch back to the primary clock occurs (see Figure 3-6). When the clock switch is complete, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the system clock. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run.

Firmware can force an exit from SEC_RUN mode. By clearing the T1OSCEN bit (T1CON<3>), an exit from SEC_RUN back to normal full-power operation is triggered. The Timer1 oscillator will continue to run and provide the system clock even though the T1OSCEN bit is cleared. The primary clock is started. When the primary clock becomes ready, a clock switch back to the primary clock occurs (see Figure 3-6). When the clock switch is complete, the Timer1 oscillator is disabled, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the system clock. The IDLEN and SCS bits are not affected by the wake-up.

FIGURE 3-9: TIMING TRANSITION FOR ENTRY TO SEC_RUN MODE

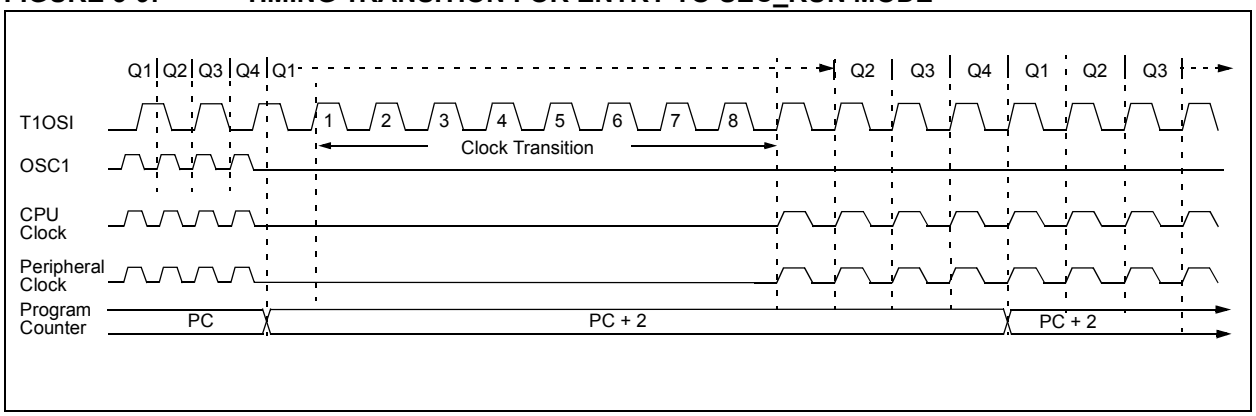


TABLE 4-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices				Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
TOSU	2220	2320	4220	4320	---0 0000	---0 0000	---0 uuuu(3)
TOSH	2220	2320	4220	4320	0000 0000	0000 0000	uuuu uuuu(3)
TOSL	2220	2320	4220	4320	0000 0000	0000 0000	uuuu uuuu(3)
STKPTR	2220	2320	4220	4320	uu-0 0000	00-0 0000	uu-u uuuu(3)
PCLATU	2220	2320	4220	4320	---0 0000	---0 0000	---u uuuu
PCLATH	2220	2320	4220	4320	0000 0000	0000 0000	uuuu uuuu
PCL	2220	2320	4220	4320	0000 0000	0000 0000	PC + 2(2)
TBLPTRU	2220	2320	4220	4320	--00 0000	--00 0000	--uu uuuu
TBLPTRH	2220	2320	4220	4320	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	2220	2320	4220	4320	0000 0000	0000 0000	uuuu uuuu
TABLAT	2220	2320	4220	4320	0000 0000	0000 0000	uuuu uuuu
PRODH	2220	2320	4220	4320	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODL	2220	2320	4220	4320	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTCON	2220	2320	4220	4320	0000 000x	0000 000u	uuuu uuuu(1)
INTCON2	2220	2320	4220	4320	1111 -1-1	1111 -1-1	uuuu -u-u(1)
INTCON3	2220	2320	4220	4320	11-0 0-00	11-0 0-00	uu-u u-uu(1)
INDF0	2220	2320	4220	4320	N/A	N/A	N/A
POSTINC0	2220	2320	4220	4320	N/A	N/A	N/A
POSTDEC0	2220	2320	4220	4320	N/A	N/A	N/A
PREINC0	2220	2320	4220	4320	N/A	N/A	N/A
PLUSW0	2220	2320	4220	4320	N/A	N/A	N/A
FSR0H	2220	2320	4220	4320	---- xxxx	---- uuuu	---- uuuu
FSR0L	2220	2320	4220	4320	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	2220	2320	4220	4320	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	2220	2320	4220	4320	N/A	N/A	N/A
POSTINC1	2220	2320	4220	4320	N/A	N/A	N/A
POSTDEC1	2220	2320	4220	4320	N/A	N/A	N/A
PREINC1	2220	2320	4220	4320	N/A	N/A	N/A
PLUSW1	2220	2320	4220	4320	N/A	N/A	N/A

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 4-2 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled, depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

REGISTER 5-1: STKPTR: STACK POINTER REGISTER

R/C-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STKFUL(1)	STKUNF(1)	—	SP4	SP3	SP2	SP1	SP0
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **STKFUL:** Stack Full Flag bit(1)
1 = Stack became full or overflowed
0 = Stack has not become full or overflowed

bit 6 **STKUNF:** Stack Underflow Flag bit(1)
1 = Stack underflow occurred
0 = Stack underflow did not occur

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **SP4:SP0:** Stack Pointer Location bits

Note 1: Bit 7 and bit 6 are cleared by user software or by a POR.

5.2.3 PUSH AND POP INSTRUCTIONS

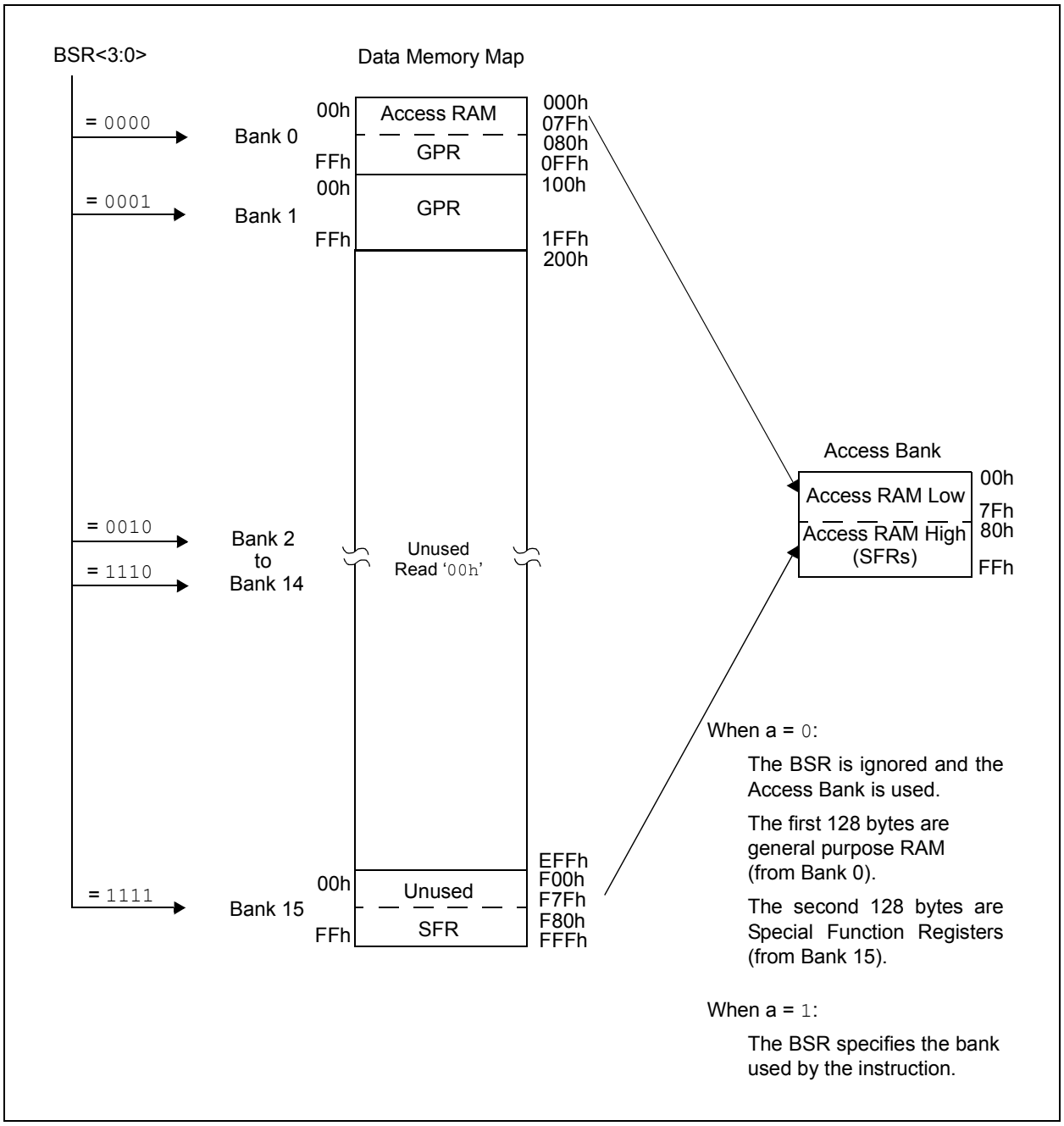
Since the Top-of-Stack (TOS) is readable and writable, the ability to push values onto the stack and pull values off the stack, without disturbing normal program execution, is a desirable option. To push the current PC value onto the stack, a PUSH instruction can be executed. This will increment the Stack Pointer and load the current PC value onto the stack. TOSU, TOSH and TOSL can then be modified to place data or a return address on the stack.

The ability to pull the TOS value off of the stack and replace it with the value that was previously pushed onto the stack, without disturbing normal execution, is achieved by using the POP instruction. The POP instruction discards the current TOS by decrementing the Stack Pointer. The previous value pushed onto the stack then becomes the TOS value.

5.2.4 STACK FULL/UNDERFLOW RESETS

These Resets are enabled by programming the STVREN bit in Configuration Register 4L. When the STVREN bit is cleared, a full or underflow condition will set the appropriate STKFUL or STKUNF bit but not cause a device Reset. When the STVREN bit is set, a full or underflow condition will set the appropriate STKFUL or STKUNF bit and then cause a device Reset. The STKFUL or STKUNF bits are cleared by the user software or a POR Reset.

FIGURE 5-6: DATA MEMORY MAP FOR PIC18F2X20/4X20 DEVICES



5.13 STATUS Register

The STATUS register, shown in Register 5-2, contains the arithmetic status of the ALU. The STATUS register can be the operand for any instruction as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC, C, OV or N bits, then the write to these five bits is disabled. These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF`, `MOVFF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, DC, OV or N bits in the STATUS register. For other instructions not affecting any Status bits (see Table 24-2).

Note: The C and DC bits operate as a $\overline{\text{borrow}}$ and digit $\overline{\text{borrow}}$ bit respectively, in subtraction.

REGISTER 5-2: STATUS REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	N	OV	Z	DC(1)	C(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **N:** Negative bit
This bit is used for signed arithmetic (2's complement). It indicates whether the result was negative (ALU MSB = 1).
1 = Result was negative
0 = Result was positive

bit 3 **OV:** Overflow bit
This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude which causes the sign bit (bit 7 of the result) to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

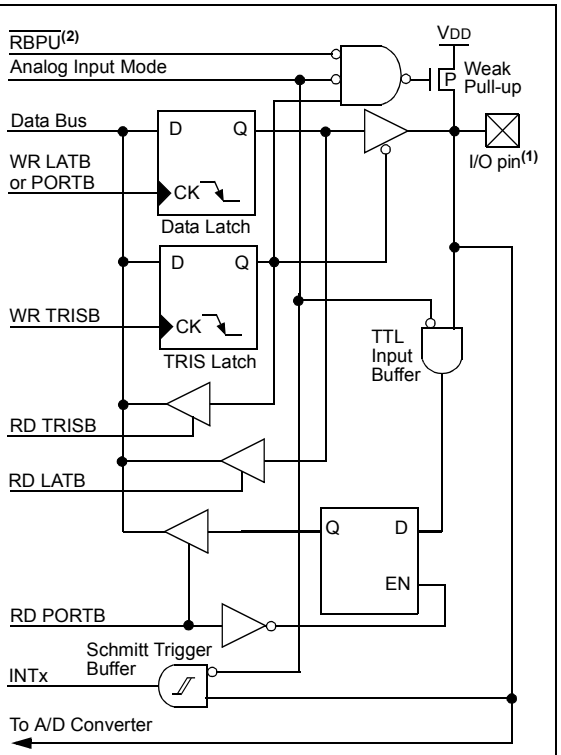
bit 1 **DC:** Digit Carry/$\overline{\text{Borrow}}$ bit(1)
For `ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions:
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit(2)
For `ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions:
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either bit 4 or bit 3 of the source register.

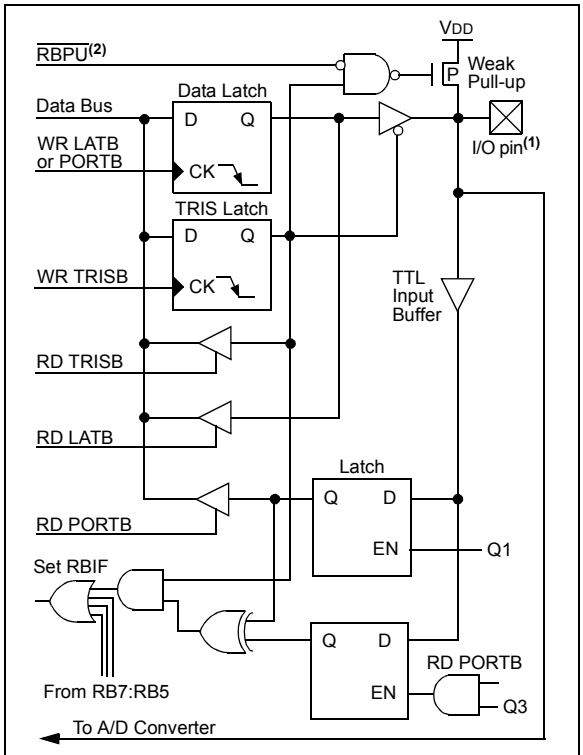
2: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low-order bit of the source register.

FIGURE 10-7: BLOCK DIAGRAM OF RB2:RB0 PINS



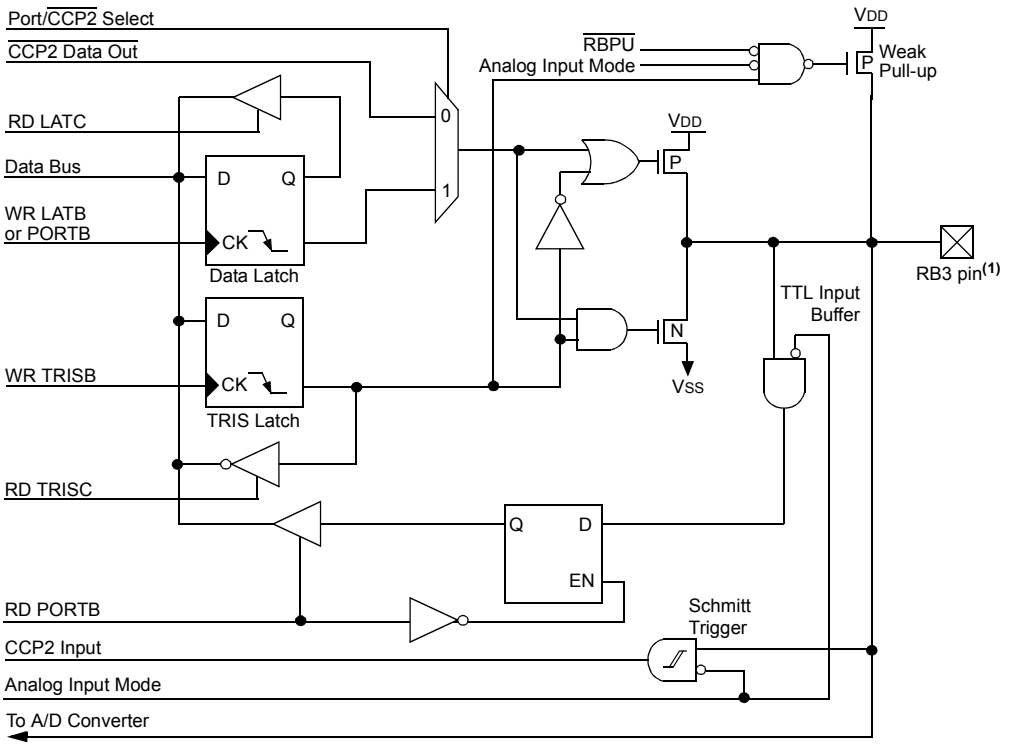
Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (INTCON2<7>).

FIGURE 10-8: BLOCK DIAGRAM OF RB4 PIN



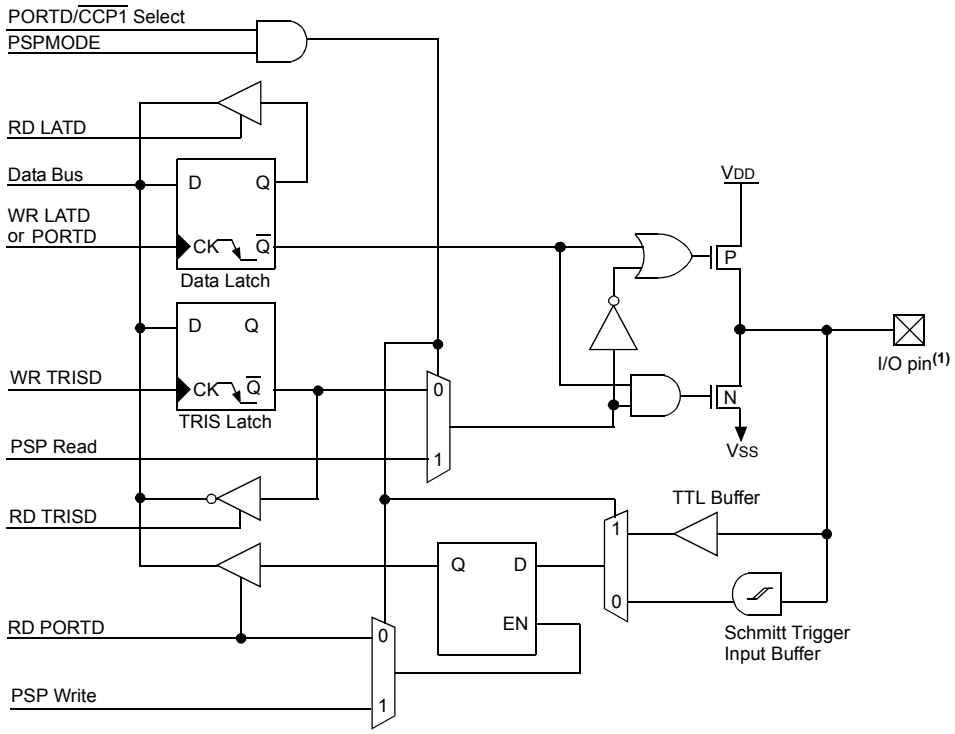
Note 1: I/O pins have diode protection to VDD and VSS.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (INTCON2<7>).

FIGURE 10-9: BLOCK DIAGRAM OF RB3/CCP2 PIN



Note 1: I/O pins have diode protection to VDD and VSS.

FIGURE 10-12: BLOCK DIAGRAM OF RD4:RD0 PINS



Note 1: I/O pins have diode protection to VDD and VSS.

TABLE 10-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit 0	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 0.
RD1/PSP1	bit 1	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 1.
RD2/PSP2	bit 2	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 2.
RD3/PSP3	bit 3	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 3.
RD4/PSP4	bit 4	ST/TTL(1)	Input/output port pin or Parallel Slave Port bit 4.
RD5/PSP5/P1B	bit 5	ST/TTL(1)	Input/output port pin, Parallel Slave Port bit 5 or Enhanced PWM output P1B.
RD6/PSP6/P1C	bit 6	ST/TTL(1)	Input/output port pin, Parallel Slave Port bit 6 or Enhanced PWM output P1C.
RD7/PSP7/P1D	bit 7	ST/TTL(1)	Input/output port pin, Parallel Slave Port bit 7 or Enhanced PWM output P1D.

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 10-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
LATD	LATD Data Latch Register								xxxx xxxx	uuuu uuuu
TRISD	PORTD Data Direction Register								1111 1111	1111 1111
TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits			0000 -111	0000 -111
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

15.5 PWM Mode

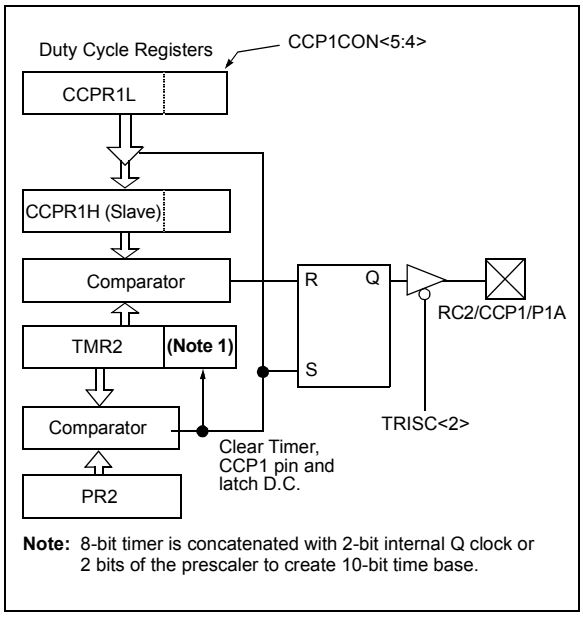
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 15-3 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 15.5.3 "Setup for PWM Operation"**.

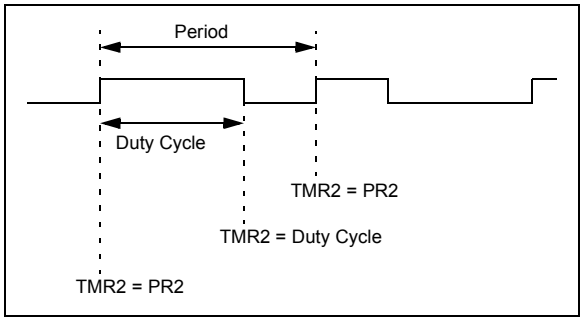
FIGURE 15-3: SIMPLIFIED PWM BLOCK DIAGRAM



Note: 8-bit timer is concatenated with 2-bit internal Q clock or 2 bits of the prescaler to create 10-bit time base.

A PWM output (Figure 15-4) has a time base (*period*) and a time that the output is high (*duty cycle*). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 15-4: PWM OUTPUT



15.5.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following equation.

EQUATION 15-1:

$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 Prescale Value})$$

PWM frequency is defined as 1/[PWM period]. When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is copied from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see **Section 13.0 "Timer2 Module"**) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

15.5.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The PWM duty cycle is calculated by the following equation.

EQUATION 15-2:

$$\text{PWM Duty Cycle} = (\text{CCPR1L:CCP1CON<5:4>}) \cdot T_{OSC} \cdot (\text{TMR2 Prescale Value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time but the duty cycle value is not copied into CCPR1H until a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

REGISTER 18-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN(1)	SYNC	—	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care.
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-Bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **Unimplemented:** Read as '0'

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode.

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** 9th bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

TABLE 18-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1, HIGH SPEED)

BAUD RATE (K)	Fosc = 40.000 MHz			Fosc = 20.000 MHz			Fosc = 16.000 MHz			Fosc = 10.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
2.4	—	—	—	4.88	103.45	255	3.91	62.76	255	2.44	1.73	255
9.6	9.77	1.73	255	9.62	0.16	129	9.62	0.16	103	9.63	0.16	64
19.2	19.23	0.16	129	19.23	0.16	64	19.23	0.16	51	18.94	-1.36	32
38.4	38.46	0.16	64	37.88	-1.36	32	38.46	0.16	25	39.06	1.73	15
57.6	58.14	0.94	42	56.82	-1.36	21	58.82	2.12	16	56.82	-1.36	10
76.8	75.76	-1.36	32	78.13	1.73	15	76.92	0.16	12	78.13	1.73	7
96.0	96.15	0.16	25	96.15	0.16	12	100.00	4.17	9	89.29	-6.99	6
115.2	113.64	-1.36	21	113.64	-1.36	10	111.11	-3.55	8	125.00	8.51	4
250.0	250.00	0.00	9	250.00	0.00	4	250.00	0.00	3	208.33	-16.67	2
300.0	312.50	4.17	7	312.50	4.17	3	333.33	11.11	2	312.50	4.17	1
500.0	500.00	0.00	4	416.67	-16.67	2	500.00	0.00	1	—	—	—
625.0	625.00	0.00	3	625.00	0.00	1	—	—	—	625.00	0.00	0
1000.0	833.33	-16.67	2	—	—	—	1000.00	0.00	0	—	—	—
1250.0	1250.00	0.00	1	1250.00	0.00	0	—	—	—	—	—	—

BAUD RATE (K)	Fosc = 8.000000 MHz			Fosc = 7.159090 MHz			Fosc = 5.068800 MHz			Fosc = 4.000 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—	0.98	225.52	255
1.2	1.95	62.76	255	1.75	45.65	255	1.24	3.13	255	1.20	0.16	207
2.4	2.40	0.16	207	2.41	0.23	185	2.40	0.00	131	2.40	0.16	103
9.6	9.62	0.16	51	9.52	-0.83	46	9.60	0.00	32	9.62	0.16	25
19.2	19.23	0.16	25	19.45	1.32	22	18.64	-2.94	16	19.23	0.16	12
38.4	38.46	0.16	12	37.29	-2.90	11	39.60	3.13	7	35.71	-6.99	6
57.6	55.56	-3.55	8	55.93	-2.90	7	52.80	-8.33	5	62.50	8.51	3
76.8	71.43	-6.99	6	74.57	-2.90	5	79.20	3.13	3	83.33	8.51	2
96.0	100.00	4.17	4	89.49	-6.78	4	—	—	—	—	—	—
115.2	125.00	8.51	3	111.86	-2.90	3	105.60	-8.33	2	125.00	8.51	1
250.0	250.00	0.00	1	223.72	-10.51	1	—	—	—	250.00	0.00	0
300.0	—	—	—	—	—	—	316.80	5.60	0	—	—	—
500.0	500.00	0.00	0	447.44	-10.51	0	—	—	—	—	—	—

BAUD RATE (K)	Fosc = 3.579545 MHz			Fosc = 2.000000 MHz			Fosc = 1.000000 MHz			Fosc = 0.032768 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.87	191.30	255	0.49	62.76	255	0.30	0.16	207	0.29	-2.48	6
1.2	1.20	0.23	185	1.20	0.16	103	1.20	0.16	51	1.02	-14.67	1
2.4	2.41	0.23	92	2.40	0.16	51	2.40	0.16	25	2.05	-14.67	0
9.6	9.73	1.32	22	9.62	0.16	12	8.93	-6.99	6	—	—	—
19.2	18.64	-2.90	11	17.86	-6.99	6	20.83	8.51	2	—	—	—
38.4	37.29	-2.90	5	41.67	8.51	2	31.25	-18.62	1	—	—	—
57.6	55.93	-2.90	3	62.50	8.51	1	62.50	8.51	0	—	—	—
76.8	74.57	-2.90	2	—	—	—	—	—	—	—	—	—
115.2	111.86	-2.90	1	125.00	8.51	0	—	—	—	—	—	—
250.0	223.72	-10.51	0	—	—	—	—	—	—	—	—	—

21.0 COMPARATOR VOLTAGE REFERENCE MODULE

The comparator voltage reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of CVREF values and has a power-down function to conserve power when the reference is not being used. The CVRCON register controls the operation of the reference as shown in Register 21-1. The block diagram is given in Figure 21-1.

The comparator reference supply voltage comes from VDD and VSS.

21.1 Configuring the Comparator Voltage Reference

The comparator voltage reference can output 16 distinct voltage levels for each range. The equations used to calculate the output of the comparator voltage reference are as follows:

EQUATION 21-1:

$$\text{If CVRR} = 1: \quad CV_{REF} = (CVR\langle 3:0\rangle) \bullet \frac{V_{DD}}{24}$$

$$\text{If CVRR} = 0: \quad CV_{REF} = (CVR\langle 3:0\rangle + 8) \bullet \frac{V_{DD}}{32}$$

The settling time of the comparator voltage reference must be considered when changing the CVREF output (see Table 26-2 in **Section 26.0 "Electrical Characteristics"**).

REGISTER 21-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE(1)	CVRR	—	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CVREN**: Comparator Voltage Reference Enable bit
1 = CVREF circuit powered on
0 = CVREF circuit powered down

bit 6 **CVROE**: Comparator VREF Output Enable bit(1)
1 = CVREF voltage level is also output on the RA2/AN2/VREF-/CVREF pin
0 = CVREF voltage is disconnected from the RA2/AN2/VREF-/CVREF pin

bit 5 **CVRR**: Comparator VREF Range Selection bit
1 = 0.00 VDD to 0.667 VDD, with VDD/24 step size
0 = 0.25 VDD to 0.75 VDD, with VDD/32 step size

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **CVR3:CVR0:** Comparator VREF Value Selection 0 ≤ VR3:VR0 ≤ 15 bits

When CVRR = 1:
$CV_{REF} = (CVR\langle 3:0\rangle) \bullet \frac{V_{DD}}{24}$

When CVRR = 0:
$CV_{REF} = 1/4 \bullet (CV_{RSRC}) + (CVR\langle 3:0\rangle + 8) \bullet \frac{V_{DD}}{32}$

Note 1: CVROE overrides the TRISA<2> bit setting.

TABLE 24-1: OPCODE FIELD DESCRIPTIONS

Field	Description
a	RAM access bit: a = 0: RAM location in Access RAM (BSR register is ignored) a = 1: RAM bank is specified by BSR register
bbb	Bit address within an 8-bit file register (0 to 7).
BSR	Bank Select Register. Used to select the current RAM bank.
d	Destination select bit: d = 0: store result in WREG d = 1: store result in file register f
dest	Destination either the WREG register or the specified register file location.
f	8-bit register file address (0x00 to 0xFF).
fs	12-bit register file address (0x000 to 0xFFF). This is the source address.
fd	12-bit register file address (0x000 to 0xFFF). This is the destination address.
k	Literal field, constant data or label (may be either an 8-bit, 12-bit or a 20-bit value).
label	Label name.
mm * *+ *- +*	The mode of the TBLPTR register for the table read and table write instructions. Only used with table read and table write instructions: No Change to register (such as TBLPTR with table reads and writes). Post-Increment register (such as TBLPTR with table reads and writes). Post-Decrement register (such as TBLPTR with table reads and writes). Pre-Increment register (such as TBLPTR with table reads and writes).
n	The relative address (2's complement number) for relative branch instructions, or the direct address for Call/Branch and Return instructions.
PRODH	Product of Multiply High Byte.
PRODL	Product of Multiply Low Byte.
s	Fast Call/Return mode select bit: s = 0: do not update into/from shadow registers s = 1: certain registers loaded into/from shadow registers (Fast mode)
u	Unused or Unchanged.
WREG	Working register (accumulator).
x	Don't care ('0' or '1'). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
TBLPTR	21-bit Table Pointer (points to a Program Memory location).
TABLAT	8-bit Table Latch.
TOS	Top-of-Stack.
PC	Program Counter.
PCL	Program Counter Low Byte.
PCH	Program Counter High Byte.
PCLATH	Program Counter High Byte Latch.
PCLATU	Program Counter Upper Byte Latch.
GIE	Global Interrupt Enable bit.
WDT	Watchdog Timer.
$\overline{TO}$	Time-out bit.
$\overline{PD}$	Power-down bit.
C, DC, Z, OV, N	ALU Status bits: Carry, Digit Carry, Zero, Overflow, Negative.
[ ]	Optional.
( )	Contents.
→	Assigned to.
< >	Register bit field.
∈	In the set of.
italics	User-defined term (font is Courier New).

MOVFF **Move f to f**

Syntax: [*label*] MOVFF f_s,f_d

Operands: $0 \le f_s \le 4095$
$0 \le f_d \le 4095$

Operation: $(f_s) \rightarrow f_d$

Status Affected: None

Encoding:

1st word (source)	1100	ffff	ffff	$ffff_s$
2nd word (destin.)	1111	ffff	ffff	$ffff_d$

Description: The contents of source register 'f_s' are moved to destination register 'f_d'. Location of source 'f_s' can be anywhere in the 4096-byte data space (000h to FFFh) and location of destination 'f_d' can also be anywhere from 000h to FFFh. Either source or destination can be W (a useful special situation). MOVFF is particularly useful for transferring a data memory location to a peripheral register (such as the transmit buffer or an I/O port).

The MOVFF instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register.

The MOVFF instruction should not be used to modify interrupt settings while any interrupt is enabled (see Page 87).

Words: 2

Cycles: 2 (3)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f' (src)	Process Data	No operation
Decode	No operation No dummy read	No operation	Write register 'f' (dest)

Example: MOVFF REG1, REG2

Before Instruction
REG1 = 0x33
REG2 = 0x11

After Instruction
REG1 = 0x33,
REG2 = 0x33

MOVLB **Move Literal to Low Nibble in BSR**

Syntax: [*label*] MOVLB k

Operands: $0 \le k \le 255$

Operation: $k \rightarrow BSR$

Status Affected: None

Encoding:

0000	0001	kkkk	kkkk

Description: The 8-bit literal 'k' is loaded into the Bank Select Register (BSR).

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write literal 'k' to BSR

Example: MOVLB 5

Before Instruction
BSR register = 0x02

After Instruction
BSR register = 0x05

TBLWT **Table Write**

Syntax: [*label*] TBLWT (*; *+; *-; +*)

Operands: None

Operation: if TBLWT*,
(TABLAT) → Holding Register,
TBLPTR - No Change;
if TBLWT*+,
(TABLAT) → Holding Register,
(TBLPTR) +1 → TBLPTR;
if TBLWT*-,
(TABLAT) → Holding Register,
(TBLPTR) -1 → TBLPTR;
if TBLWT+*,
(TBLPTR) +1 → TBLPTR,
(TABLAT) → Holding Register

Status Affected: None

Encoding:

0000	0000	0000	11nn nn=0 * =1 *+ =2 *- =3 +*

Description: This instruction uses the 3 LSBs of TBLPTR to determine which of the 8 holding registers the TABLAT is written to. The holding registers are used to program the contents of Program Memory (P.M.). (Refer to **Section 6.0 "Flash Program Memory"** for additional details on programming Flash memory.)
The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2 MByte address range. The LSb of the TBLPTR selects which byte of the program memory location to access.

TBLPTR[0] = 0: Least Significant Byte of Program Memory Word

TBLPTR[0] = 1: Most Significant Byte of Program Memory Word

The TBLWT instruction can modify the value of TBLPTR as follows:

- no change
- post-increment
- post-decrement
- pre-increment

TBLWT Table Write (Continued)

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	No operation	No operation
No operation	No operation (Read TABLAT)	No operation	No operation (Write to Holding Register)

Example1: `TBLWT *+;`

Before Instruction
TABLAT = 0x55
TBLPTR = 0x00A356
HOLDING REGISTER (0x00A356) = 0xFF

After Instructions (table write completion)
TABLAT = 0x55
TBLPTR = 0x00A357
HOLDING REGISTER (0x00A356) = 0x55

Example 2: `TBLWT +*;`

Before Instruction
TABLAT = 0x34
TBLPTR = 0x01389A
HOLDING REGISTER (0x01389A) = 0xFF
HOLDING REGISTER (0x01389B) = 0xFF

After Instruction (table write completion)
TABLAT = 0x34
TBLPTR = 0x01389B
HOLDING REGISTER (0x01389A) = 0xFF
HOLDING REGISTER (0x01389B) = 0x34

FIGURE 26-1: PIC18F2220/2320/4220/4320 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

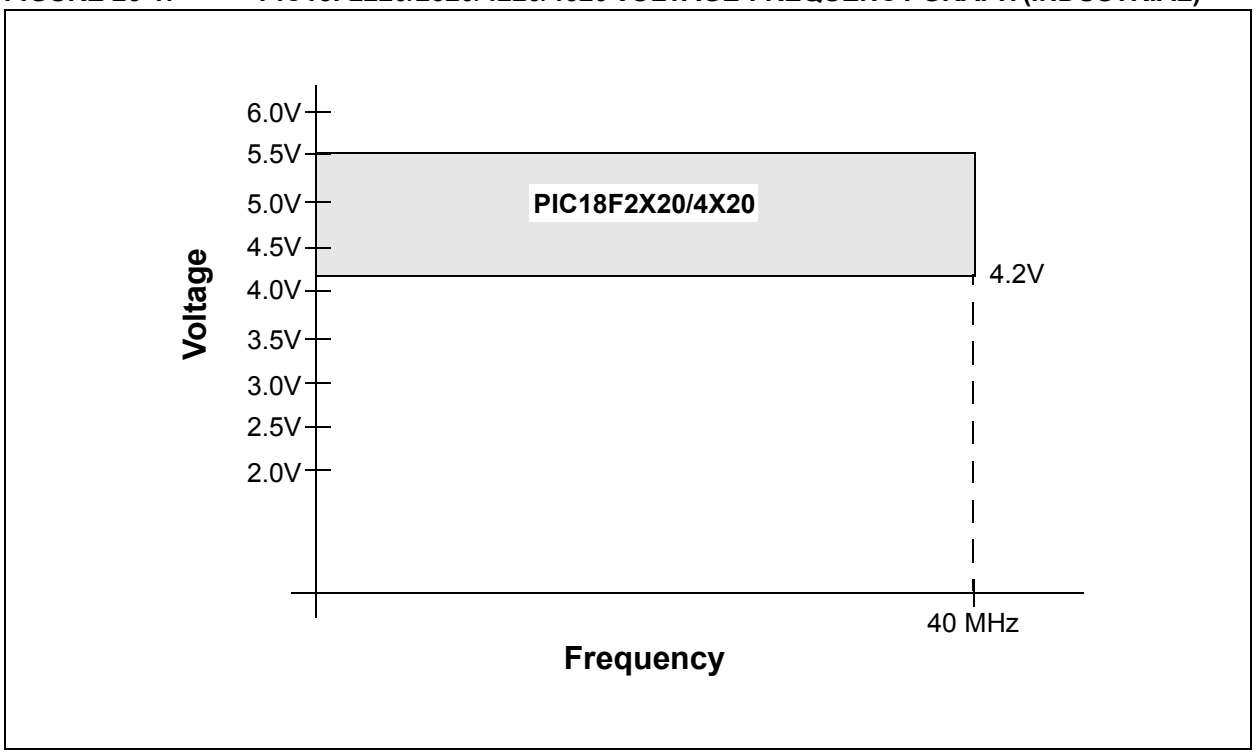
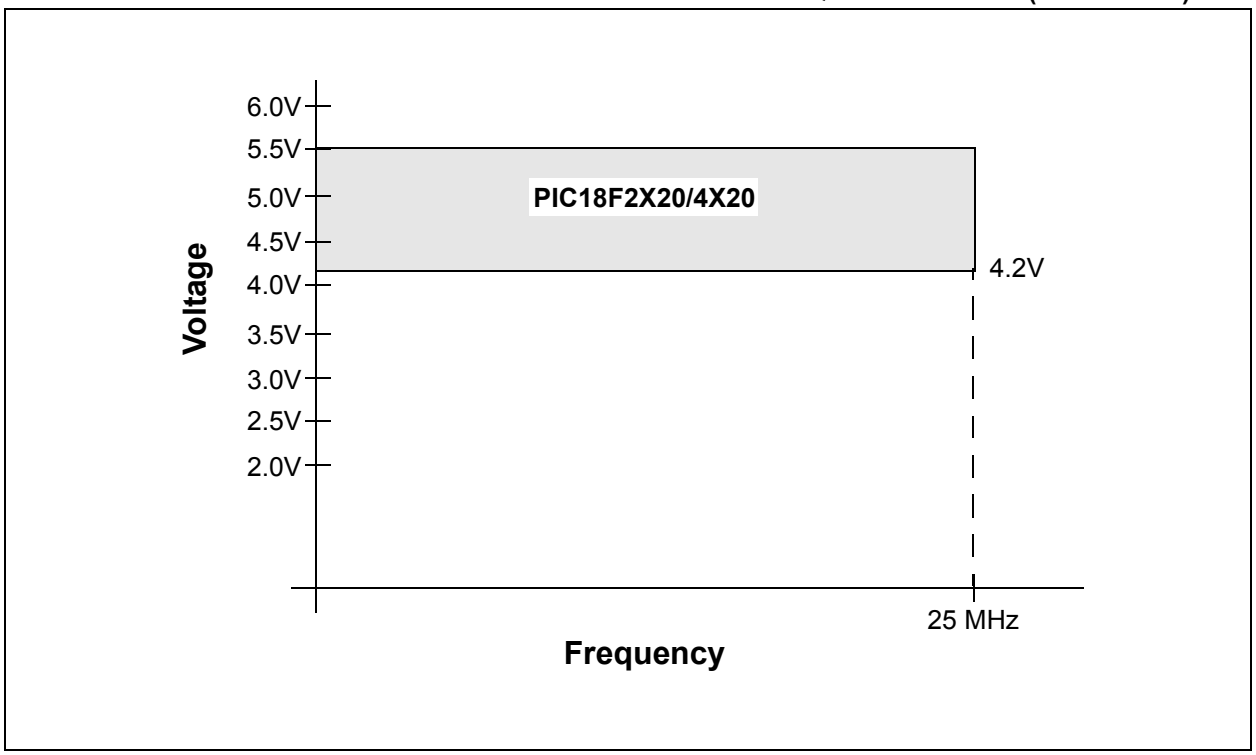


FIGURE 26-2: PIC18F2220/2320/4220/4320 VOLTAGE-FREQUENCY GRAPH (EXTENDED)



26.2 DC Characteristics: Power-Down and Supply Current PIC18F2220/2320/4220/4320 (Industrial) PIC18LF2220/2320/4220/4320 (Industrial) (Continued)

PIC18LF2220/2320/4220/4320 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2220/2320/4220/4320 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD)(2,3)						
	PIC18LF2X20/4X20	140	275	µA	-40°C	VDD = 2.0V	FOSC = 4 MHz (**RC_IDLE** mode, internal oscillator source)
		140	275	µA	+25°C		
		150	275	µA	+85°C		
	PIC18LF2X20/4X20	220	375	µA	-40°C	VDD = 3.0V	
		220	375	µA	+25°C		
		210	375	µA	+85°C		
	All devices	390	800	µA	-40°C	VDD = 5.0V	
		400	800	µA	+25°C		
		380	800	µA	+85°C		
	Extended devices	410	800	µA	+125°C		
	PIC18LF2X20/4X20	150	250	µA	-40°C	VDD = 2.0V	FOSC = 1 MHz (**PRI_RUN**, EC oscillator)
		150	250	µA	+25°C		
		160	250	µA	+85°C		
	PIC18LF2X20/4X20	340	350	µA	-40°C	VDD = 3.0V	
		300	350	µA	+25°C		
		280	350	µA	+85°C		
	All devices	0.72	1.0	mA	-40°C	VDD = 5.0V	
		0.63	1.0	mA	+25°C		
		0.57	1.0	mA	+85°C		
	Extended devices	0.53	1.0	mA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

4: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

26.2 DC Characteristics: Power-Down and Supply Current PIC18F2220/2320/4220/4320 (Industrial) PIC18LF2220/2320/4220/4320 (Industrial) (Continued)

PIC18LF2220/2320/4220/4320 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2220/2320/4220/4320 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
D025 (ΔIOSCB)	**Timer1 Oscillator**	2.1	2.2	μA	-40°C	VDD = 2.0V	32 kHz on Timer1(4)
		1.8	2.2	μA	+25°C		
		2.1	2.2	μA	+85°C		
		2.2	3.8	μA	-40°C	VDD = 3.0V	32 kHz on Timer1(4)
		2.6	3.8	μA	+25°C		
		2.9	3.8	μA	+85°C		
		3.0	6.0	μA	-40°C	VDD = 5.0V	32 kHz on Timer1(4)
		3.2	6.0	μA	+25°C		
		3.4	7.0	μA	+85°C		
D026 (ΔIAD)	**A/D Converter**	1.0	2.0	μA	-40°C to +85°C	VDD = 2.0V	A/D on, not converting
		1.0	2.0	μA	-40°C to +85°C	VDD = 3.0V	
		1.0	2.0	μA	-40°C to +85°C	VDD = 5.0V	
	Extended devices only	1.0	8.0	μA	-40°C to +125°C	VDD = 5.0V	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

4: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

C

D

Q

R