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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560d30l3b4e0x

List of tables

1 Introduction

1.1 Document overview

This document describes the device features and highlights the important electrical and physical characteristics.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices designed to be central to the development of the next wave of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology and designed specifically for embedded applications.

The advanced and cost-efficient e200z0h host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (auxiliary processing unit), providing improved code density. It operates at speeds of up to 48 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with the user's implementations.

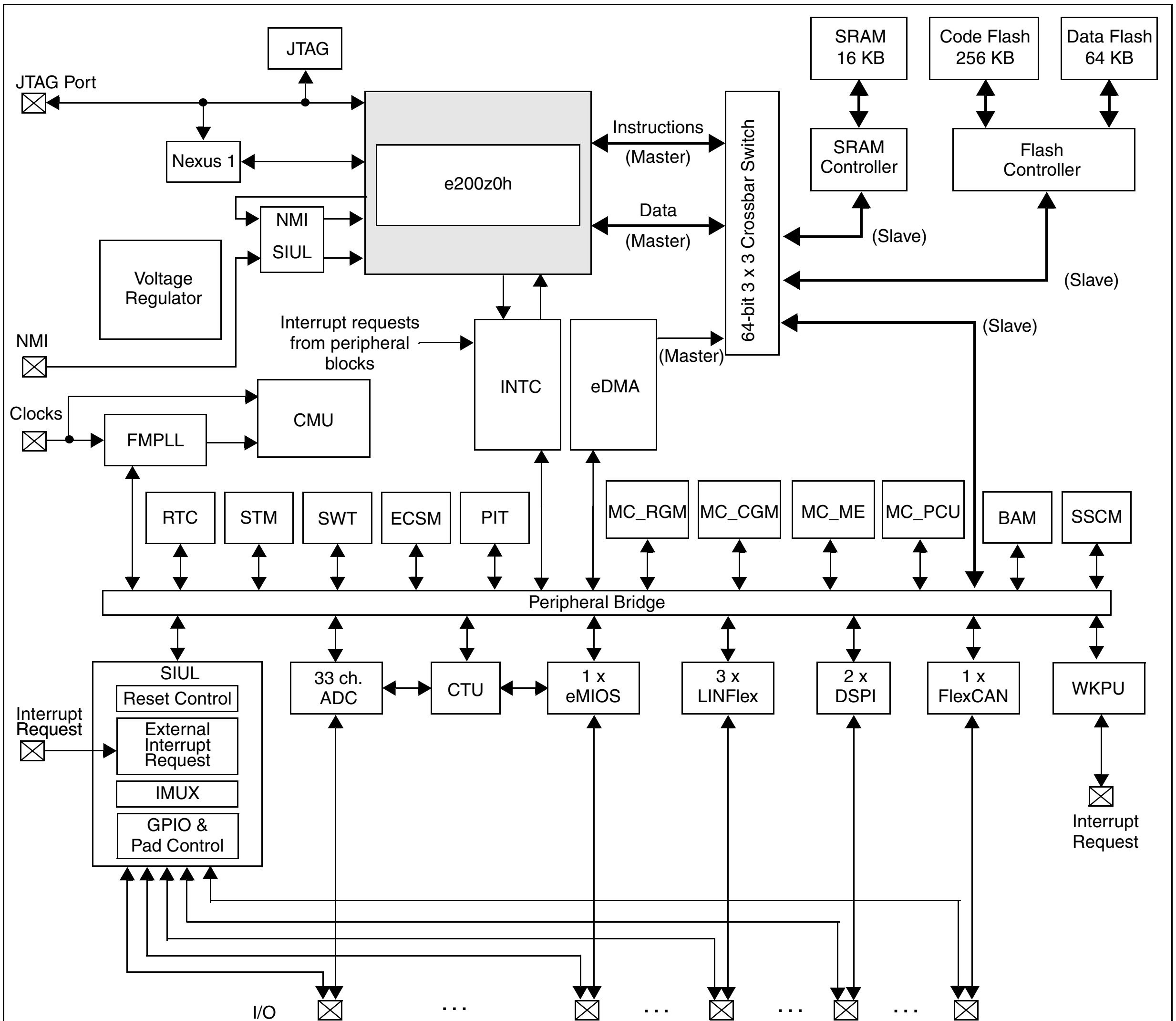
The device platform has a single level of memory hierarchy and can support a wide range of on-chip static random access memory (SRAM) and internal flash memory.

Table 2. Pictus 512K device comparison

Feature	Device			
	SPC560D30L1	SPC560D30L3	SPC560D40L1	SPC560D40L3
CPU	e200z0h			
Execution speed	Static – up to 48 MHz			
Code flash memory	128 KB		256 KB	
Data flash memory	64 KB (4 × 16 KB)			
SRAM	12 KB		16 KB	
eDMA	16 ch			
ADC (12-bit)	16 ch	33 ch	16 ch	33 ch
CTU	16 ch			
Total timer I/O(1) eMIOS	14 ch, 16-bit	28 ch, 16-bit	14 ch, 16-bit	28 ch, 16-bit
– Type X(2)	2 ch	5 ch	2 ch	5 ch
– Type Y(3)	—	9 ch	—	9 ch
– Type G(4)	7 ch	7 ch	7 ch	7 ch

2 Block diagram

Figure 1 shows a top-level block diagram of the Pictus 512K device series.



Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DSPI	Deserial Serial Peripheral Interface
ECSM	Error Correction Status Module
eDMA	Enhanced Direct Memory Access
eMIOS	Enhanced Modular Input Output System
Flash	Flash memory
FlexCAN	Controller Area Network (FlexCAN)
FMPLL	Frequency-Modulated Phase-Locked Loop
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)

MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
NMI	Non-Maskable Interrupt
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
WKPU	Wakeup Unit
XBAR	Crossbar switch

Figure 1. Pictus 512K series block diagram

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] — CS4_0 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 — DSPI_0 SIUL ADC	I/O I/O — I/O I I	S	Tristate	43	68
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — CS0_1 WKPU[9][3]	SIUL eMIOS_0 — DSPI_1 WKPU	I/O I/O — I/O I	S	Tristate	20	29
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	79
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1]	SIUL eMIOS_0 — DSPI_1 SIUL	I/O I/O — I/O I	S	Tristate	52	80
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] — — EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 — — SIUL ADC	I/O I/O — — I I	S	Tristate	44	71
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[5]	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0]	SIUL eMIOS_0 eMIOS_0 — SIUL BAM	I/O I/O — — I I	S	Input, weak pull-up	45	72
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[5]	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — I/O I	S	Pull-down	46	73

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number LQFP64	Pin number LQFP100
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — LIN0RX WKPU[4][3] CAN0RX	SIUL — — LINFlex_0 WKPU FlexCAN_0	I/O — — I I I	S	Tristate	15	24
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX — —	SIUL LINFlex_0 — —	I/O O — —	M	Tristate	64	100
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — — — WKPU[11][3] LIN0RX	SIUL — — — WKPU LINFlex_0	I/O — — — I I	S	Tristate	1	1
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — ADC1_P[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	50
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — ADC1_P[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	53
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — ADC1_P[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	54
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — ADC1_P[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	55

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 7* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 7. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.6 Thermal characteristics

4.6.1 Package thermal characteristics

Table 14. LQFP thermal characteristics(1)

Symbol	C		Parameter	Conditions(2)		Value	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection(3)	Single-layer board —1s	LQFP64	72.1	°C/W
					LQFP100	65.2	
				Four-layer board — 2s2p	LQFP64	57.3	
					LQFP100	51.8	
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board(4)	Four-layer board — 2s2p	LQFP64	44.1	°C/W
					LQFP100	41.3	
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case(5)	Single-layer board — 1s	LQFP64	26.5	°C/W
					LQFP100	23.9	
				Four-layer board — 2s2p	LQFP64	26.2	
					LQFP100	23.7	
Ψ_{JB}	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board — 1s	LQFP64	41	°C/W
					LQFP100	41.6	
				Four-layer board — 2s2p	LQFP64	43	
					LQFP100	43.4	
Ψ_{JC}	CC	D	Junction-to-case thermal characterization parameter, natural convection	Single-layer board — 1s	LQFP64	11.5	°C/W
					LQFP100	10.4	
				Four-layer board — 2s2p	LQFP64	11.1	
					LQFP100	10.2	

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C
3. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-7. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA}.
4. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB}.
5. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC}.

4.6.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using *Equation 1*:

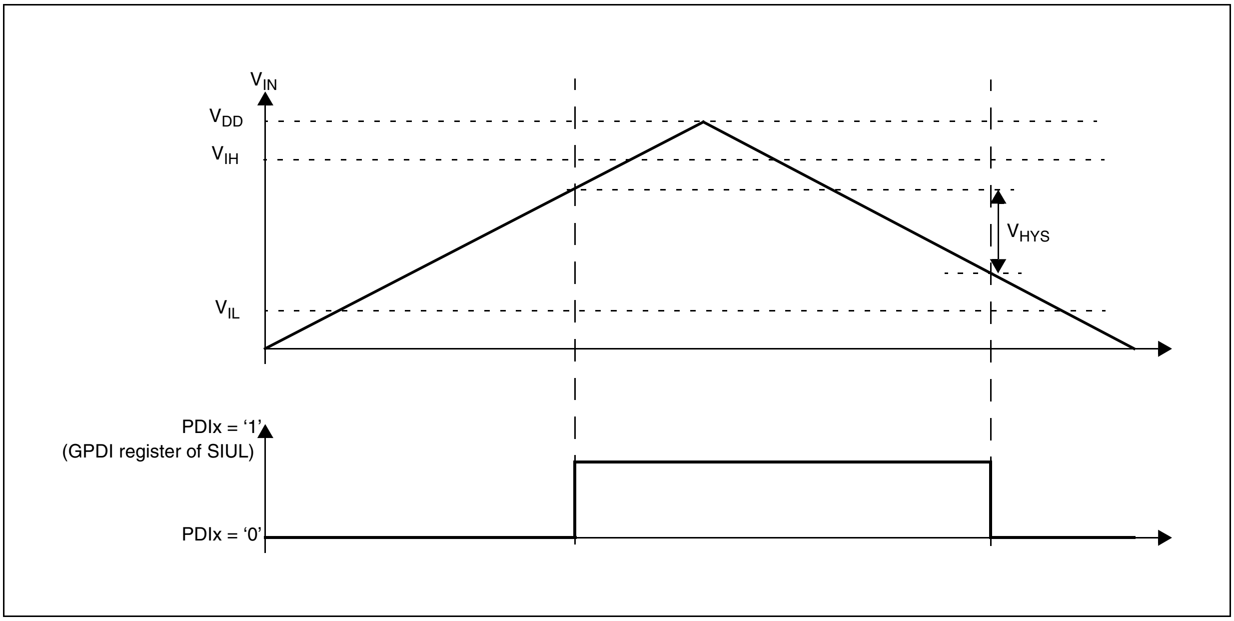


Figure 4. Input DC electrical characteristics definition

Table 15. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions(1)		Value Min	Value Typ	Value Max	Unit
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	V
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}(2)	SR	P	Digital input filtered pulse	—		—	—	40	ns
W_{NFI}(2)	SR	P	Digital input not filtered pulse	—		1000	—	—	ns

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

4.7.4 Output pin transition times

Table 19. Output pin transition times

Symbol		C	Parameter	Conditions(1)		Value Min	Value Typ	Value Max	Unit
t_{tr}	CC	D	Output transition time output pin(2) SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
t_{tr}	CC	D	Output transition time output pin(2) MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 20*.

Table 21 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 20. I/O supply segment

Package	Supply segment 1	Supply segment 2	Supply segment 3	Supply segment 4
LQFP100	pin 16 – pin 35	pin 37 – pin 69	pin 70 – pin 83	pin 84 – pin 15
LQFP64	pin 8 – pin 26	pin 28 – pin 55	pin 56 – pin 7	—

Table 26. Power consumption on VDD_BV and VDD_HV (continued)

Symbol		C	Parameter	Conditions(1)		Value			Unit
						Min	Typ	Max	
$I_{DDSTDBY}$	CC	P	STANDBY mode current(9)	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	30	100	µA
		D			T_A = 55 °C	—	75	—	
		D			T_A = 85 °C	—	180	700	
		D			T_A = 105 °C	—	315	1000	
		P			T_A = 125 °C	—	560	1700	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
3. Higher current may be sinked by device during power-up and standby exit. Please refer to in-rush average current on *Table 24*.
4. RUN current measured with typical application with accesses on both flash memory and SRAM.
5. Only for the “P” classification: Code fetched from SRAM: serial IPs CAN and LIN in loop-back mode, DSPI as Master, PLL as system clock (3 × Multiplier) peripherals on (eMIOS/CTU/ADC) and running at maximum frequency, periodic SW/WDG timer reset enabled.
6. Data flash power down. Code flash in low power. SIRC (128 kHz) and FIRC (16 MHz) on. 10 MHz XTAL clock. FlexCAN: 0 ON (clocked but no reception or transmission). LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON.PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.
7. Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, HPVreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.
8. When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.
9. Only for the “P” classification: ULPVreg on, HP/LPVreg off, 16 KB SRAM on, device configured for minimum consumption, all possible modules switched off.

4.11 Flash memory electrical characteristics

The data flash operation depends strongly on the code flash operation. If code flash is switched-off, the data flash is disabled.

4.11.1 Program/Erase characteristics

Table 27 shows the program and erase characteristics.

Table 27. Program and erase specifications (code flash)

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$t_{dwprogram}$	CC	C	Double word (64 bits) program time(4)	—	22	50	500	µs
$t_{16Kpperase}$	CC	C	16 KB block preprogram and erase time	—	300	500	5000	ms

Table 36. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance (ESR) Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout $C_1 = C_2$ (pF)(1)	Shunt capacitance between xtalout and xtalin C0(2) (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1. The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2. The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

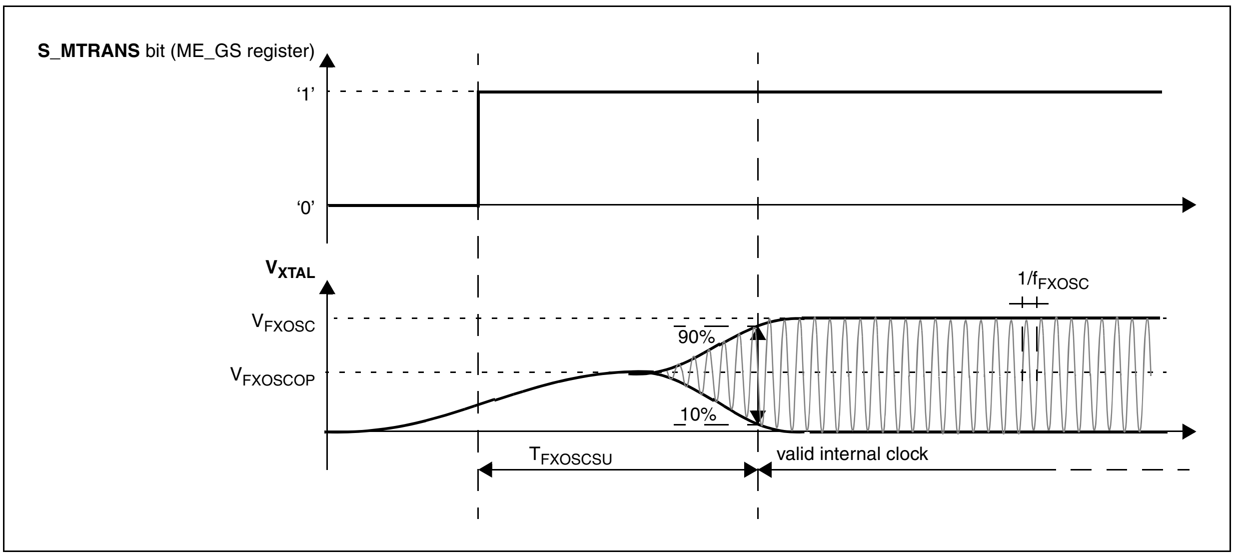


Figure 10. Fast external crystal oscillator (4 to 16 MHz) timing diagram

Table 37. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz

Equation 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as anti-aliasing.

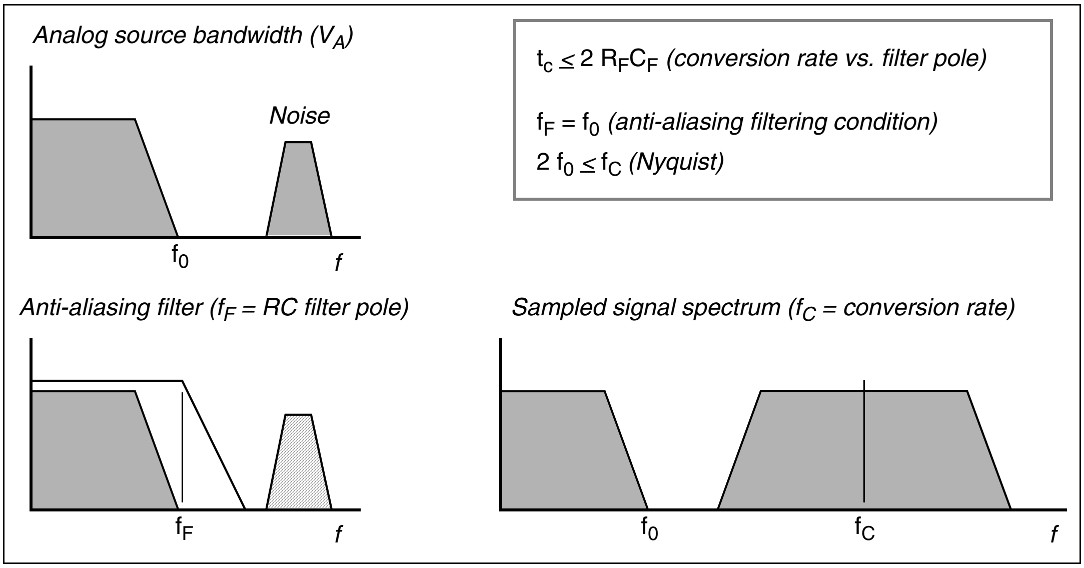


Figure 15. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (t_c). Again the conversion period t_c is longer than the sampling time t_s, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time t_s, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 2048 \bullet C_S$$

4.17.3 ADC electrical characteristics

Table 41. ADC input leakage current

Symbol		C	Parameter	Conditions		Value Min	Value Typ	Value Max	Unit
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 42. ADC conversion characteristics

Symbol		C	Parameter	Conditions(1)	Value Min	Value Typ	Value Max	Unit
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})(2)	—	–0.1	—	0.1	V
V_{DD_ADC}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	—	Analog input voltage(3)	—	V_{SS_ADC} – 0.1	—	V_{DD_ADC} + 0.1	V
f_{ADC}	SR	—	ADC analog frequency	V_{DD} = 5.0 V	3.33	—	32 + 4%	MHz
				V_{DD} = 3.3 V	3.33	—	20 + 4%	
Δ_{ADC_SYS}	SR	—	ADC clock duty cycle (ipg_clk)	ADCLKSEL = 1(4)	45	—	55	%
t_{ADC_PU}	SR	—	ADC power up delay	—	—	—	1.5	µs
t_s	CC	T	Sampling time(5) V_{DD} = 3.3 V	f_{ADC} = 20 MHz, INPSAMP = 12	600	—	—	ns
				f_{ADC} = 3.33 MHz, INPSAMP = 255	—	—	76.2	µs
		T	Sampling time(5) V_{DD} = 5.0 V	f_{ADC} = 24 MHz, INPSAMP = 13	500	—	—	ns
				f_{ADC} = 3.33 MHz, INPSAMP = 255	—	—	76.2	µs

Table 42. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions(1)		Min	Typ	Max	Unit
t_c	CC	P	Conversion time(6) V_{DD} = 3.3 V	f_{ADC} = 20 MHz, INPCMP = 0		2.4	—	—	µs
				f_{ADC} = 13.33 MHz, INPCMP = 0		—	—	3.6	
		P	Conversion time(6) V_{DD} = 5.0 V	f_{ADC} = 32 MHz, INPCMP = 0		1.5	—	—	µs
				f_{ADC} = 13.33 MHz, INPCMP = 0		—	—	3.6	
C_S	CC	D	ADC input sampling capacitance	—			5		pF
C_{P1}	CC	D	ADC input pin capacitance 1	—			3		pF
C_{P2}	CC	D	ADC input pin capacitance 2	—			1		pF
C_{P3}	CC	D	ADC input pin capacitance 3	—			1.5		pF
R_{SW1}	CC	D	Internal resistance of analog source	—		—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-precise channels	No overload		—	1	3	LSB
INLX	CC	T	Absolute Integral non-linearity-extended channels	No overload		—	1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload		—	0.5	1	LSB
E_O	CC	T	Absolute Offset error	—		—	2	—	LSB
E_G	CC	T	Absolute Gain error	—		—	2	—	LSB
TUEP(7)	CC	P	Total unadjusted error for precise channels, input only pins	Without current injection		–6		6	LSB
		T		With current injection		–8		8	

Table 43. On-chip peripherals current consumption(1) (continued)

Symbol		C	Parameter	Conditions		Typical value(2)	Unit
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on V_{DD_BV}	Ballast static consumption (only clocked)		1	µA
				Ballast dynamic consumption (continuous communication): – Baudrate: 2 Mbit/s – Transmission every 8 µs – Frame: 16 bits		$16 \times f_{periph}$	µA
$I_{DD\_BV(ADC)}$	CC	T	ADC supply current on V_{DD_BV}	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	$41 \times f_{periph}$	µA
					Ballast dynamic consumption (continuous conversion)(3)	$5 \times f_{periph}$	µA
$I_{DD\_HV\_ADC(ADC)}$	CC	T	ADC supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	$2 \times f_{periph}$	µA
					Analog dynamic consumption (continuous conversion)	$75 \times f_{periph} + 32$	µA
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	8.21	mA
$I_{DD\_HV(PLL)}$	CC	T	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	$30 \times f_{periph}$	µA

1. Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 48 MHz
2. f_{periph} is an absolute value.
3. During the conversion, the total current consumption is given from the sum of the static and dynamic consumption, i.e., $(41 + 5) \times f_{periph}$.

4.18.2 DSPI characteristics

Table 44. DSPI characteristics(1)

No.	Symbol		C	Parameter		DSPI0/DSPI1 Min	Typ	Max	Unit
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	
			D		Master mode (MTFE = 1)	83	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	MHz

5.2.2 LQFP64

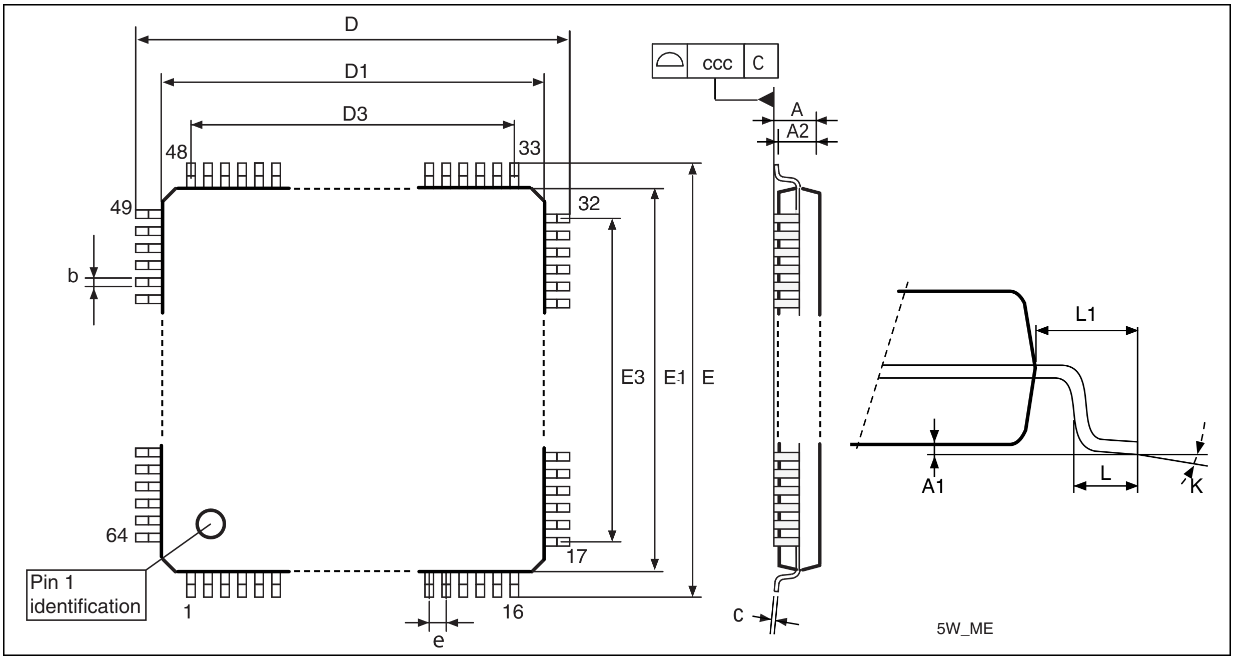


Figure 27. LQFP64 mechanical drawing

Table 47. LQFP64 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.6	—	—	0.0630
A1	0.05	—	0.15	0.0020	—	0.0059
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	—	0.2	0.0035	—	0.0079
D	11.8	12	12.2	0.4646	0.4724	0.4803
D1	9.8	10	10.2	0.3858	0.3937	0.4016
D3	—	7.5	—	—	0.2953	—
E	11.8	12	12.2	0.4646	0.4724	0.4803
E1	9.8	10	10.2	0.3858	0.3937	0.4016
E3	—	7.5	—	—	0.2953	—
e	—	0.5	—	—	0.0197	—
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1	—	1	—	—	0.0394	—

Table 50. Abbreviations (continued)

Abbreviation	Meaning
TDO	Test data output
TMS	Test mode select

Revision history

Table 51 summarizes revisions to this document.

Table 51. Document revision history

Date	Revision	Changes
09-Jul-2009	1	Initial release.
18-Feb-2010	2	Updated the following tables: - Absolute maximum ratings - Low voltage power domain electrical characteristics; - On-chip peripherals current consumption - DSPI characteristics; - JTAG characteristics; - ADC conversion characteristics; Inserted a note on “Flash power supply DC characteristics” section.
10-Aug-2010	3	“Features” section: Updated information concerning eMIOS, ADC, LINFlex, Nexus and low power capabilities “Pictus 512K device comparison” table: updated the “Execution speed” row “Pictus 512K series block diagram” figure: – updated max number of Crossbar Switches – updated Legend “Pictus 512K series block summary” table: added contents concernig the eDMA block “LQFP100 pin configuration (top view)” figure: – removed alternate functions – updated supply pins “LQFP64 pin configuration (top view)” figure: removed alternate functions Added “Pin muxing” section “NVUSRO register” section: Deleted “NVUSRO[WATCHDOG_EN] field description“ section “Recommended operating conditions (3.3 V)” table: – TV_{DD}: deleted min value – In footnote No. 3, changed capacitance value between V_{DD_BV} and V_{SS_LV} “Recommended operating conditions (5.0 V)” table: deleted TV_{DD} min value “LQFP thermal characteristics” table: changed $R_{\theta JC}$ values “I/O input DC electrical characteristics” table: – W_{FI}: updated max value – W_{NFI}: updated min value “I/O consumption” table: removed I_{DYNSEG} row Added “I/O weight” table “Program and erase specifications (Code Flash)” table: deleted T_{Bank_C} row

Table 51. Document revision history (continued)

Date	Revision	Changes
16-Sep-2011	4 (cont.)	MEDIUM configuration output buffer electrical characteristics: changed “I_{OH} = 100 µA” to “I_{OL} = 100 µA” in V_{OL} conditions I/O consumption: replaced instances of “Root medium square” with “Root mean square” Updated section “Voltage regulator electrical characteristics” Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added a fifth LVD (LVDHV3B); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; deleted note referencing power domain No. 2 (this domain is not present on the device); updated electrical characteristics table Updated and renamed section “Power consumption” (was previously section “Low voltage domain power consumption”) Program and erase specifications (code flash): updated symbols; updated t_{esus} values Updated Flash memory read access timing EMI radiated emission measurement: updated S_{EMI} values Updated FMPLL electrical characteristics Crystal oscillator and resonator connection scheme: inserted footnote about possibly requiring a series resistor Fast internal RC oscillator (16 MHz) electrical characteristics: updated t_{FIRCSU} values Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 13 ADC conversion characteristics: – updated conditions for sampling time V_{DD} = 5.0 V – updated conditions for conversion time V_{DD} = 5.0 V Updated Abbreviations Removed Order codes tables.
01-Dec-2011	5	Replaced “TBD” with “8.21 mA” in $I_{DD\_HV(FLASH)}$ cell of On-chip peripherals current consumption table