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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560d40l1b4e0x

Figure 3 shows the Pictus 512K in the LQFP64 package.

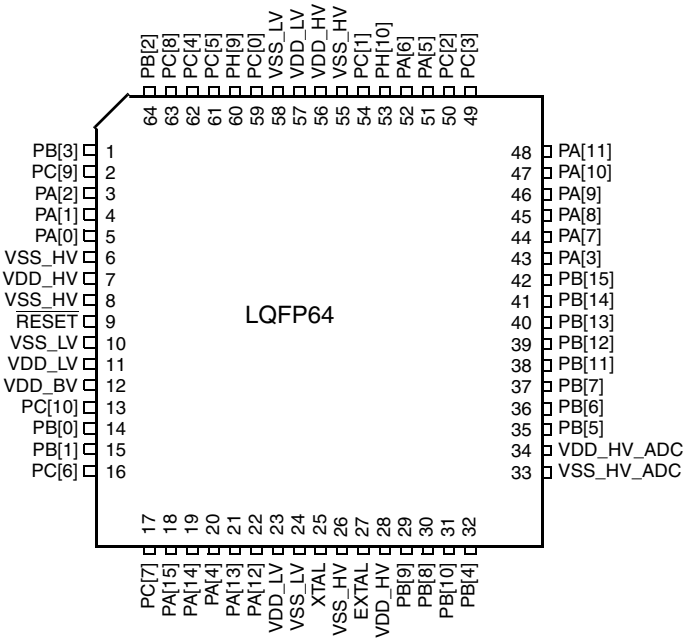


Figure 3. LQFP64 pin configuration (top view)

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up while TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.

3.3 Voltage supply pins

Voltage supply pins are used to provide power to the device. Two dedicated pins are used for 1.2 V regulator stabilization.

Table 4. Voltage supply pin descriptions

Port pin	Function	Pin number	
		LQFP64	LQFP100
VDD_HV	Digital supply voltage	7, 28, 34, 56	15, 37, 52, 70, 84
VSS_HV	Digital ground	6, 8, 26, 33, 55	14, 16, 35, 51, 69, 83
VDD_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{SS_LV} pin.(1)	11, 23, 57	19, 32, 85
VSS_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{DD_LV} pin.(1)	10, 24, 58	18, 33, 86
VDD_BV	Internal regulator supply voltage	12	20

1. A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet for details).

3.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[a]

M = Medium[a] [b]

F = Fast[a] [b]

I = Input only with analog feature[a]

J = Input/Output ('S' pad) with analog feature

X = Oscillator

3.5 System pins

The system pins are listed in *Table 5*.

Table 5. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET configuration	Pin number	
					LQFP64	LQFP100
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	9	17

a. See the I/O pad electrical characteristics in the device datasheet for details.

b. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see the PCR[SRC] description in the device reference manual).

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] — CS4_0 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 — DSPI_0 SIUL ADC	I/O I/O — I/O I I	S	Tristate	43	68
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — CS0_1 WKPU[9][3]	SIUL eMIOS_0 — DSPI_1 WKPU	I/O I/O — I/O I	S	Tristate	20	29
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	51	79
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1]	SIUL eMIOS_0 — DSPI_1 SIUL	I/O I/O — I/O I	S	Tristate	52	80
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] — — EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 — — SIUL ADC	I/O I/O — — I I	S	Tristate	44	71
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[5]	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0]	SIUL eMIOS_0 eMIOS_0 — SIUL BAM	I/O I/O — — I I	S	Input, weak pull-up	45	72
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[5]	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — I/O I	S	Pull-down	46	73

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — LIN0RX WKPU[4][3] CAN0RX	SIUL — — LINFlex_0 WKPU FlexCAN_0	I/O — — I I I	S	Tristate	15	24
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX — —	SIUL LINFlex_0 — —	I/O O — —	M	Tristate	64	100
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — — — WKPU[11][3] LIN0RX	SIUL — — — WKPU LINFlex_0	I/O — — — I I	S	Tristate	1	1
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — ADC1_P[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	50
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — ADC1_P[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	53
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — ADC1_P[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	54
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — ADC1_P[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	55

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ADC1_S[4] WKPU[25][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	30	39
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ADC1_S[5] WKPU[26][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	29	38
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ADC1_S[6] WKPU[8][3]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	40
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC1_S[12]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	59
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC1_X[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	61
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC1_X[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	63
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC1_X[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	65

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction (2)	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 —	GPIO[54] — — — ADC1_P[10]	SIUL — — — ADC	I — — — I	I	Tristate	—	47
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 —	GPIO[55] — — — ADC1_P[11]	SIUL — — — ADC	I — — — I	I	Tristate	—	48
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 —	GPIO[56] — — — ADC1_P[12]	SIUL — — — ADC	I — — — I	I	Tristate	—	49
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — ADC1_P[13]	SIUL — — — ADC	I — — — I	I	Tristate	—	56
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — ADC1_P[14]	SIUL — — — ADC	I — — — I	I	Tristate	—	57
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — ADC1_P[15]	SIUL — — — ADC	I — — — I	I	Tristate	—	58
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC1_S[8]	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	60
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC1_S[9]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	—	62

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ADC1_S[10]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	64
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ADC1_S[11]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	66
Port E									
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 —	GPIO[64] E0UC[16] — — WKPU[6][3]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	—	6
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	8
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 — —	GPIO[66] E0UC[18] — — EIRQ[21] SIN_1	SIUL eMIOS_0 — — SIUL DSPI_1	I/O I/O — — I I	M	Tristate	—	89
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	—	90
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	—	93
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	—	94

4.5 Recommended operating conditions

Table 12. Recommended operating conditions (3.3 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS}	SR	—	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}(1)	SR	—	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}(2)	SR	—	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}(3)	SR	—	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}(4)	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	3.0(5)	3.6	V
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	—	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
				Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	—	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	—	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
TV_{DD}	SR	—	V_{DD} slope to ensure correct power up(6)	—	3.0(7)	250×10^3 (0.25 [V/µs])	V/s

1. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
2. 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
3. 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
6. Guaranteed by device validation
7. Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH})

Table 13. Recommended operating conditions (5.0 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS}	SR	—	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}(1)	SR	—	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
				Voltage drop(2)	3.0	5.5	

4.6 Thermal characteristics

4.6.1 Package thermal characteristics

Table 14. LQFP thermal characteristics(1)

Symbol		C	Parameter	Conditions(2)		Value	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection(3)	Single-layer board —1s	LQFP64	72.1	°C/W
					LQFP100	65.2	
				Four-layer board — 2s2p	LQFP64	57.3	
					LQFP100	51.8	
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board(4)	Four-layer board — 2s2p	LQFP64	44.1	°C/W
					LQFP100	41.3	
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case(5)	Single-layer board — 1s	LQFP64	26.5	°C/W
					LQFP100	23.9	
				Four-layer board — 2s2p	LQFP64	26.2	
					LQFP100	23.7	
Ψ_{JB}	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board — 1s	LQFP64	41	°C/W
					LQFP100	41.6	
				Four-layer board — 2s2p	LQFP64	43	
					LQFP100	43.4	
Ψ_{JC}	CC	D	Junction-to-case thermal characterization parameter, natural convection	Single-layer board — 1s	LQFP64	11.5	°C/W
					LQFP100	10.4	
				Four-layer board — 2s2p	LQFP64	11.1	
					LQFP100	10.2	

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C
3. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-7. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA}.
4. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB}.
5. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC}.

4.6.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using *Equation 1*:

4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- *Table 16* provides weak pull figures. Both pull-up and pull-down resistances are supported.
- *Table 17* provides output driver characteristics for I/O pads when in SLOW configuration.
- *Table 18* provides output driver characteristics for I/O pads when in MEDIUM configuration.

Table 16. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 17. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V_{DD}	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	0.8V_{DD}	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V_{DD}	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	0.1V_{DD}	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

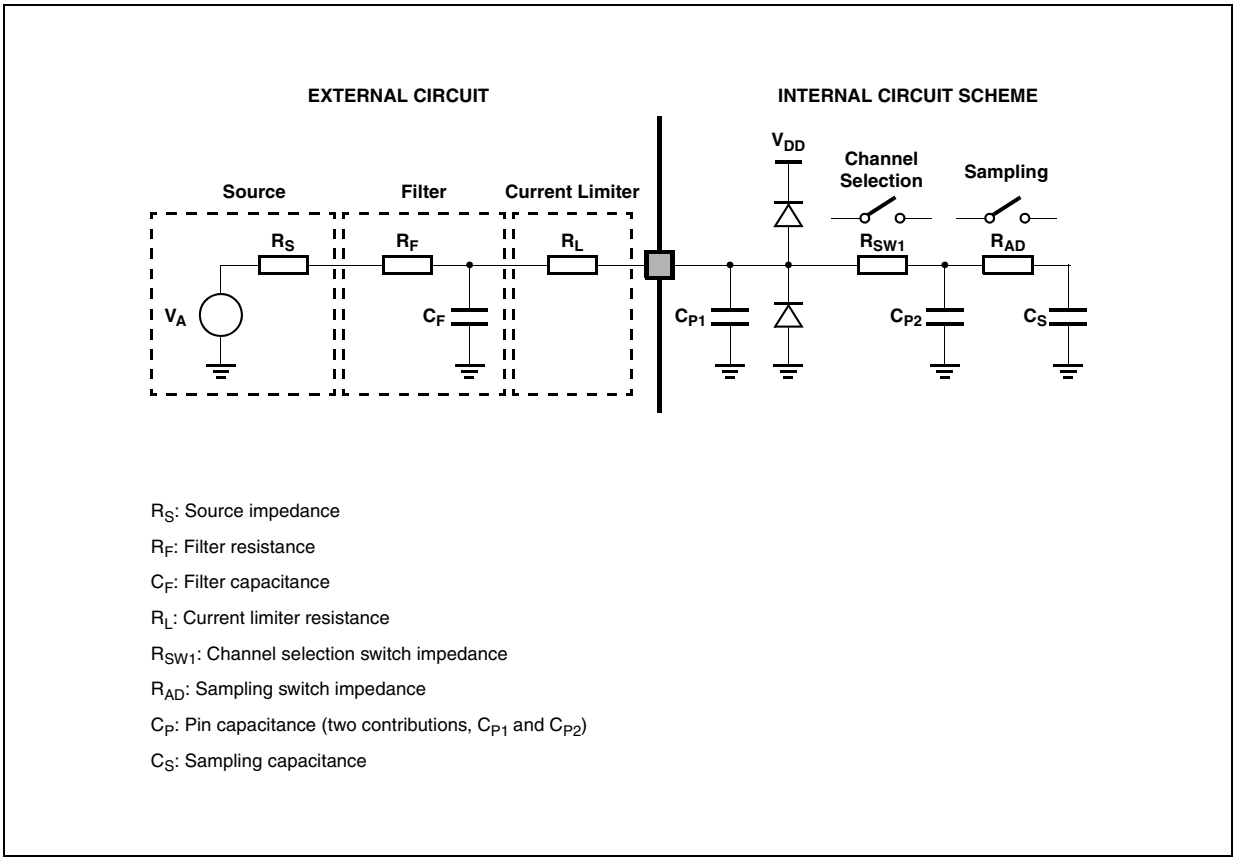
Table 22. I/O weight[1] (continued)

Pad	LQFP100/LQFP64			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PD[7]	1%	1%	1%	1%
PD[8]	1%	1%	1%	1%
PB[4]	1%	1%	1%	1%
PB[5]	1%	1%	1%	1%
PB[6]	1%	1%	1%	1%
PB[7]	1%	1%	1%	1%
PD[9]	1%	1%	1%	1%
PD[10]	1%	1%	1%	1%
PD[11]	1%	1%	1%	1%
PB[11]	9%	9%	11%	11%
PD[12]	8%	8%	10%	10%
PB[12]	8%	8%	10%	10%
PD[13]	8%	8%	9%	9%
PB[13]	8%	8%	9%	9%
PD[14]	7%	7%	9%	9%
PB[14]	7%	7%	8%	8%
PD[15]	7%	7%	8%	8%
PB[15]	6%	6%	7%	7%
PA[3]	6%	6%	7%	7%
PA[7]	4%	4%	5%	5%
PA[8]	4%	4%	5%	5%
PA[9]	4%	4%	5%	5%
PA[10]	5%	5%	6%	6%
PA[11]	5%	5%	6%	6%
PE[12]	5%	5%	6%	6%
PC[3]	5%	5%	6%	6%
PC[2]	5%	7%	6%	6%
PA[5]	5%	6%	5%	6%
PA[6]	4%	4%	5%	5%
PC[1]	5%	17%	4%	12%
PC[0]	6%	9%	7%	8%
PE[2]	7%	10%	8%	9%

Table 24. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low-power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low-power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up[5]	—	—	—	300[6]	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.
3. This value is acceptable to guarantee operation from 4.5 V to 5.5 V.
4. External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.
5. In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 µs, depending on external capacitances to be loaded).



R_S: Source impedance

R_F: Filter resistance

C_F: Filter capacitance

R_L: Current limiter resistance

R_{SW1}: Channel selection switch impedance

R_{AD}: Sampling switch impedance

C_P: Pin capacitance (two contributions, C_{P1} and C_{P2})

C_S: Sampling capacitance

Figure 12. Input equivalent circuit (precise channels)

Table 42. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
TUEX[7]	CC	T	Total unadjusted error for extended channel	Without current injection	–10		10	LSB
		T		With current injection	–12		12	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS} **must** be common (to be tied together externally).
3. V_{AINx} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.
4. Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.
5. During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sampling time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.
6. This parameter does not include the sampling time t_S, but only the time for determining the digital result and the time to load the result's register with the conversion result.
7. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.18 On-chip peripherals

4.18.1 Current consumption

Table 43. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Typical value[2]	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	500 Kbyte/s	Total (static + dynamic) consumption: – FlexCAN in loop-back mode – XTAL at 8 MHz used as CAN engine clock source – Message sending period is 580 µs	8 × f_{periph} + 85	µA
				125 Kbyte/s		8 × f_{periph} + 27	µA
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: – eMIOS channel OFF – Global prescaler enabled		29 × f_{periph}	µA
				Dynamic consumption: – It does not change varying the frequency (0.003 mA)		3	µA
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: – LIN mode – Baudrate: 20 Kbyte/s		5 × f_{periph} + 31	µA

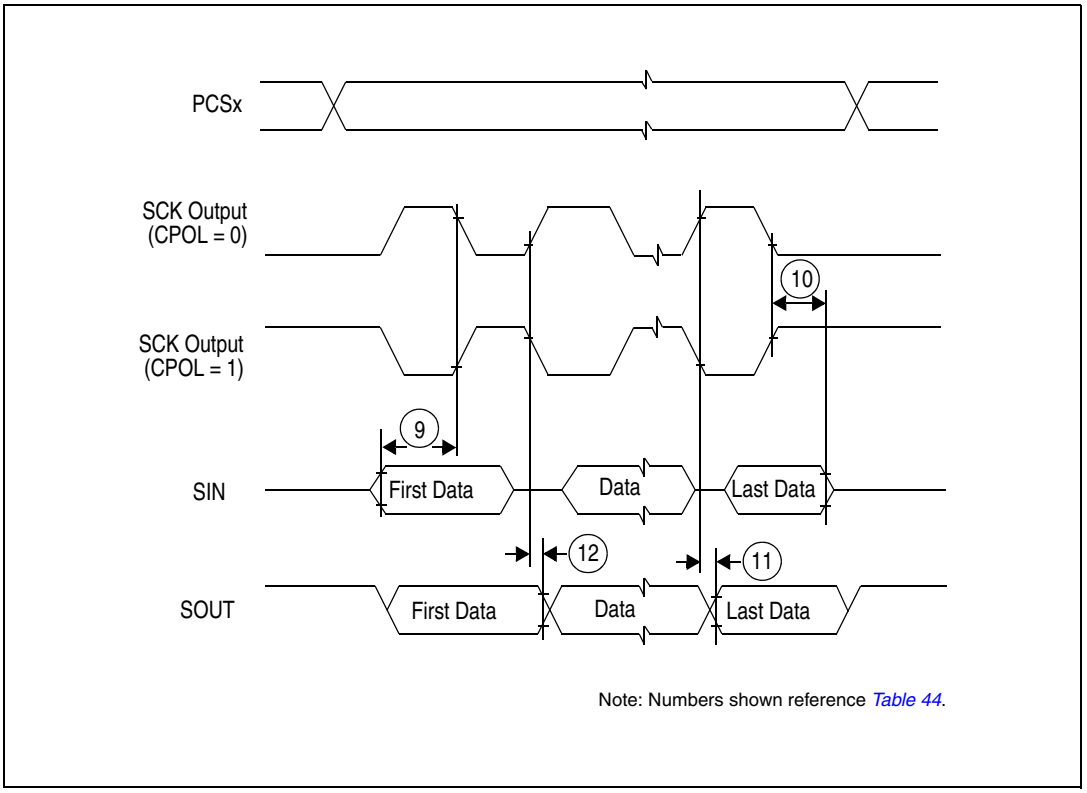


Figure 17. DSPI classic SPI timing – master, CPHA = 1

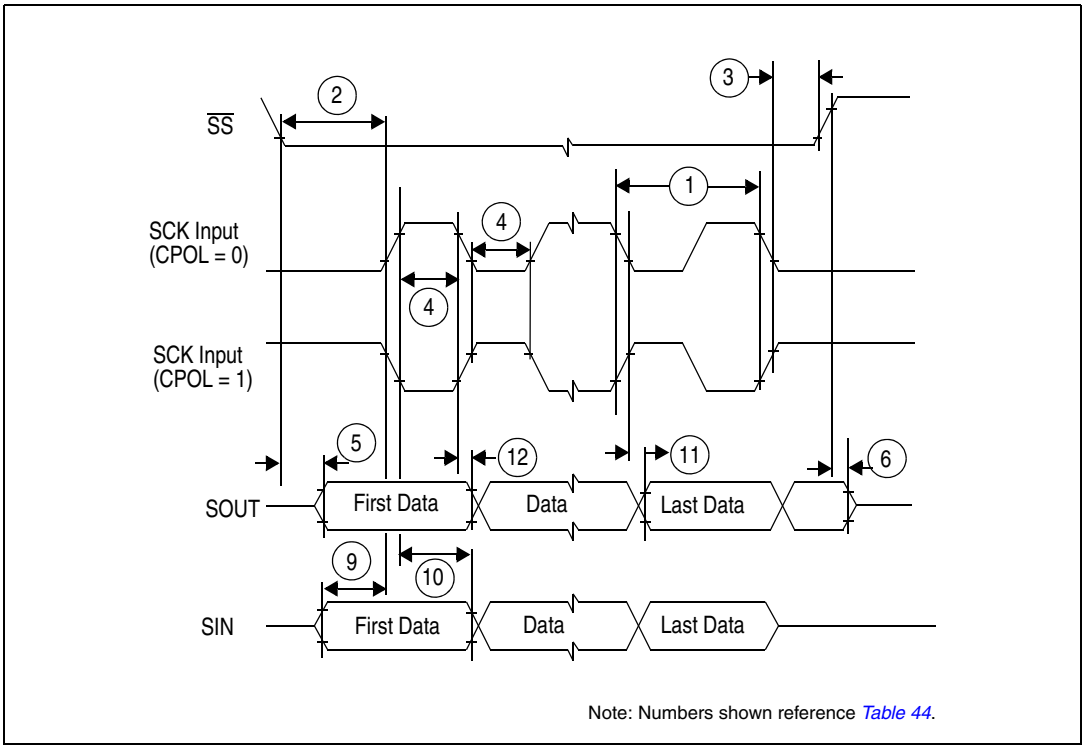


Figure 18. DSPI classic SPI timing – slave, CPHA = 0

Table 46. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	**mm**			**inches**		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 47. LQFP64 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	—	—	0.08	—	—	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6 Ordering information

Table 48. Order codes

Order code	CPU	Memory		Package	Op. temp. (°C)	Speed (MHz)	Voltage	Packing
		Code flash / SRAM (KB)	Data flash					
SPC560D30L1B3E0X	e200z0h	128 / 12	4 x 16 KB	LQFP64	–40 to 105	32	3.3 / 5 V	Tape & Reel
SPC560D30L1C3E0X					–40 to 125			
SPC560D30L1B4E0X	e200z0h	128 / 12	4 x 16 KB	LQFP64	–40 to 105	48	3.3 / 5 V	Tape & Reel
SPC560D30L1C4E0X					–40 to 125			
SPC560D30L1B3E0X	e200z0h	128 / 12	4 x 16 KB	LQFP64	–40 to 105	32	3.3 / 5 V	Tape & Reel
SPC560D30L1C3E0X					–40 to 125			
SPC560D30L1B4E0X	e200z0h	128 / 12	4 x 16 KB	LQFP64	–40 to 105	48	3.3 / 5 V	Tape & Reel
SPC560D30L1C4E0X					–40 to 125			
SPC560D40L3B3E0X	e200z0h	256 / 16	4 x 16 KB	LQFP100	–40 to 105	32	3.3 / 5 V	Tape & Reel
SPC560D40L3C3E0X					–40 to 125			
SPC560D40L3B4E0X	e200z0h	256 / 16	4 x 16 KB	LQFP100	–40 to 105	48	3.3 / 5 V	Tape & Reel
SPC560D40L3C4E0X					–40 to 125			
SPC560D40L3B3E0X	e200z0h	256 / 16	4 x 16 KB	LQFP100	–40 to 105	32	3.3 / 5 V	Tape & Reel
SPC560D40L3C3E0X					–40 to 125			
SPC560D40L3B4E0X	e200z0h	256 / 16	4 x 16 KB	LQFP100	–40 to 105	48	3.3 / 5 V	Tape & Reel
SPC560D40L3C4E0X					–40 to 125			

Table 49. Order codes for engineering samples(1)

Order code	CPU	Memory		Package	Op. temp. (°C)	Speed (MHz)	Voltage	Packing
		Code flash / SRAM (KB)	Data flash					
SPC560D40L1-ENG	e200z0h	256 / 16	4 x 16 KB	LQFP64	–40 to 125	48	3.3 / 5 V	Tape & Reel
SPC560D40L3-ENG				LQFP100				

1. Engineering samples are suitable only for evaluation and development purpose but NOT for qualification and production. Their silicon version and maturity may vary until the product has reached qualification.

Table 51. Document revision history (continued)

Date	Revision	Changes
16-Sep-2011	4 (cont.)	MEDIUM configuration output buffer electrical characteristics: changed "I_{OH} = 100 µA" to "I_{OL} = 100 µA" in V_{OL} conditions I/O consumption: replaced instances of "Root medium square" with "Root mean square" Updated section "Voltage regulator electrical characteristics" Section "Low voltage detector electrical characteristics": changed title (was "Voltage monitor electrical characteristics"); added a fifth LVD (LVDHV3B); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of "Low voltage monitor" with "Low voltage detector"; deleted note referencing power domain No. 2 (this domain is not present on the device); updated electrical characteristics table Updated and renamed section "Power consumption" (was previously section "Low voltage domain power consumption") Program and erase specifications (code flash): updated symbols; updated t_{esus} values Updated Flash memory read access timing EMI radiated emission measurement: updated S_{EMI} values Updated FMPLL electrical characteristics Crystal oscillator and resonator connection scheme: inserted footnote about possibly requiring a series resistor Fast internal RC oscillator (16 MHz) electrical characteristics: updated t_{FIRCSU} values Section "Input impedance and ADC accuracy": changed "V_A/V_{A2}" to "V_{A2}/V_A" in Equation 13 ADC conversion characteristics: – updated conditions for sampling time V_{DD} = 5.0 V – updated conditions for conversion time V_{DD} = 5.0 V Updated Abbreviations Removed Order codes tables.
01-Dec-2011	5	Replaced "TBD" with "8.21 mA" in $I_{DD\_HV(FLASH)}$ cell of On-chip peripherals current consumption table

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