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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560d40l1c4e0x

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Figure 2 shows the Pictus 512K in the LQFP100 package.

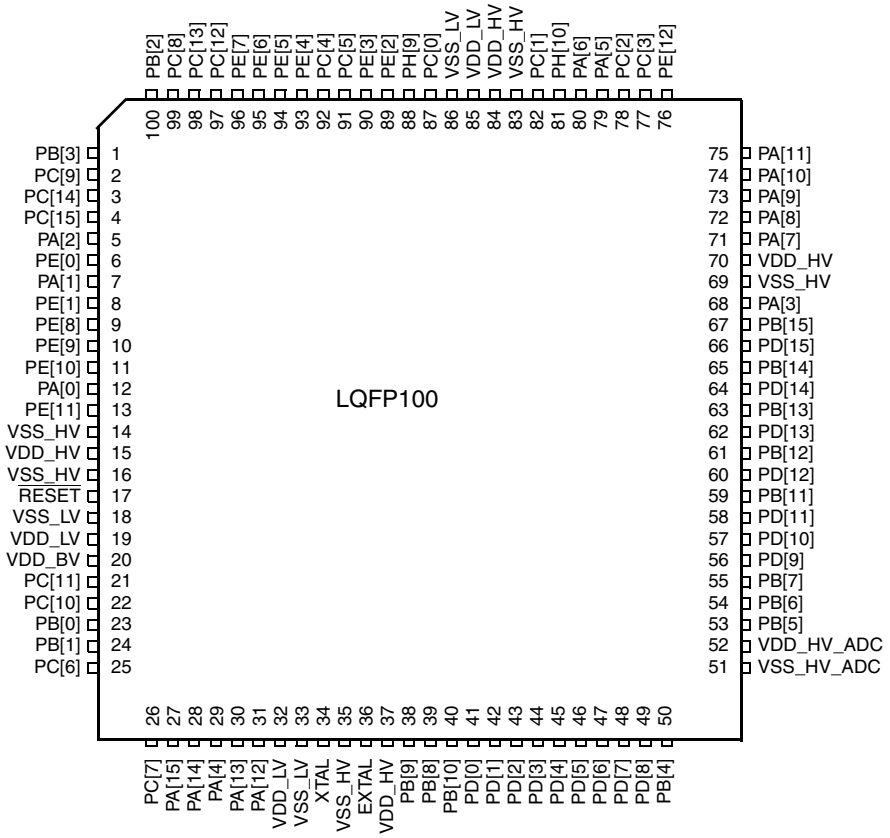

Figure 2. LQFP100 pin configuration (top view)

Table 4. Voltage supply pin descriptions

Port pin	Function	Pin number	
		LQFP64	LQFP100
VDD_HV	Digital supply voltage	7, 28, 34, 56	15, 37, 52, 70, 84
VSS_HV	Digital ground	6, 8, 26, 33, 55	14, 16, 35, 51, 69, 83
VDD_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{SS_LV} pin.(1)	11, 23, 57	19, 32, 85
VSS_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{DD_LV} pin.(1)	10, 24, 58	18, 33, 86
VDD_BV	Internal regulator supply voltage	12	20

1. A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet for details).

3.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[a]

M = Medium[a] [b]

F = Fast[a] [b]

I = Input only with analog feature[a]

J = Input/Output ('S' pad) with analog feature

X = Oscillator

3.5 System pins

The system pins are listed in *Table 5*.

Table 5. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET configuration	Pin number	
					LQFP64	LQFP100
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	9	17

a. See the I/O pad electrical characteristics in the device datasheet for details.

b. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see the PCR[SRC] description in the device reference manual).

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] — LIN2TX ADC1_S[2]	SIUL eMIOS_0 — LINFlex_2 ADC	I/O I/O — O I	S	Tristate	47	74
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] — — EIRQ[16] ADC1_S[3] LIN2RX	SIUL eMIOS_0 — — SIUL ADC LINFlex_2	I/O I/O — — I I I	S	Tristate	48	75
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — — — EIRQ[17] SIN_0	SIUL — — — SIUL DSPI_0	I/O — — — I I	S	Tristate	22	31
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — CS3_1	SIUL DSPI_0 — DSPI_1	I/O O — I/O	M	Tristate	21	30
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	19	28
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10][3]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M	Tristate	18	27
Port B									
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — LIN2TX	SIUL FlexCAN_0 — LINFlex_2	I/O O — O	M	Tristate	14	23

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] — — EIRQ[20]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	4
Port D									
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — —	GPIO[48] — — — WKPU[27][3] ADC1_P[4]	SIUL — — — WKPU ADC	I — — — I I	I	Tristate	—	41
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — —	GPIO[49] — — — WKPU[28][3] ADC1_P[5]	SIUL — — — WKPU ADC	I — — — I I	I	Tristate	—	42
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — ADC1_P[6]	SIUL — — — ADC	I — — — I	I	Tristate	—	43
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — ADC1_P[7]	SIUL — — — ADC	I — — — I	I	Tristate	—	44
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — ADC1_P[8]	SIUL — — — ADC	I — — — I	I	Tristate	—	45
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — ADC1_P[9]	SIUL — — — ADC	I — — — I	I	Tristate	—	46

Table 13. Recommended operating conditions (5.0 V) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS_LV}(3)	SR	—	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}(4)	SR	—	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
				Voltage drop(2)	3.0	5.5	
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS}	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC} (5)	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
				Voltage drop(2)	3.0	5.5	
				Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	—	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
				Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	—	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	—	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
TV_{DD}	SR	—	V_{DD} slope to ensure correct power up(6)	—	3.0(7)	250 x 10^3 (0.25 [V/µs])	V/s

1. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
2. Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.6 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.
3. 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
4. 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).
5. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
6. Guaranteed by device validation
7. Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH})

Note: SRAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

Table 22. I/O weight[1] (continued)

Pad	LQFP100/LQFP64			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PC[14]	8%	8%	10%	10%
PC[15]	8%	11%	9%	10%
PA[2]	8%	8%	9%	9%
PE[0]	7%	7%	9%	9%
PA[1]	7%	7%	8%	8%
PE[1]	7%	10%	8%	8%
PE[8]	6%	9%	8%	8%
PE[9]	6%	6%	7%	7%
PE[10]	6%	6%	7%	7%
PA[0]	5%	7%	6%	7%
PE[11]	5%	5%	6%	6%
PC[11]	7%	7%	9%	9%
PC[10]	8%	11%	9%	10%
PB[0]	8%	11%	9%	10%
PB[1]	8%	8%	10%	10%
PC[6]	8%	8%	10%	10%
PC[7]	8%	8%	10%	10%
PA[15]	8%	11%	9%	10%
PA[14]	7%	11%	9%	9%
PA[4]	7%	7%	8%	8%
PA[13]	7%	10%	8%	9%
PA[12]	7%	7%	8%	8%
PB[9]	1%	1%	1%	1%
PB[8]	1%	1%	1%	1%
PB[10]	5%	5%	6%	6%
PD[0]	1%	1%	1%	1%
PD[1]	1%	1%	1%	1%
PD[2]	1%	1%	1%	1%
PD[3]	1%	1%	1%	1%
PD[4]	1%	1%	1%	1%
PD[5]	1%	1%	1%	1%
PD[6]	1%	1%	1%	1%

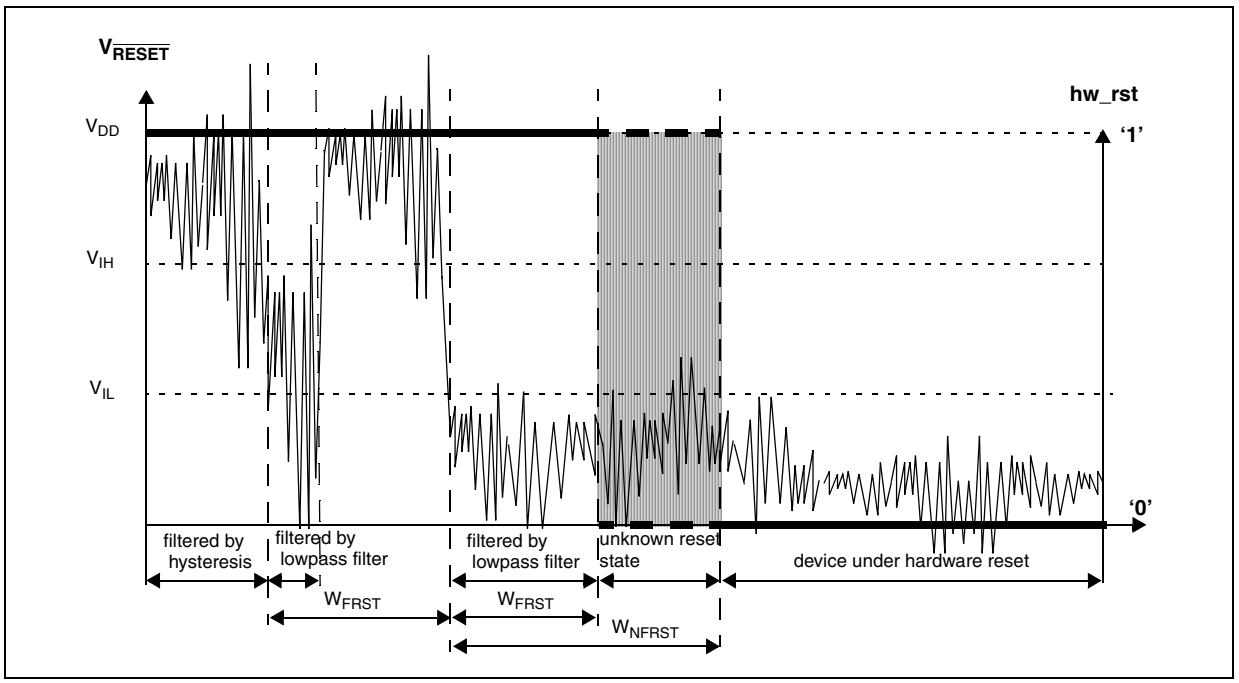

Figure 6. Noise filtering on reset signal

Table 23. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD} + 0.4$	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

Table 24. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low-power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low-power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up[5]	—	—	—	300[6]	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.
3. This value is acceptable to guarantee operation from 4.5 V to 5.5 V.
4. External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.
5. In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 µs, depending on external capacitances to be loaded).

Table 33. EMI radiated emission measurement(1)(2)

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150	—	1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	48	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP100 package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 48 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14	dBµV

1. EMI testing and I/O port waveforms per IEC 61967-1, -2, -4
2. For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard. For more details, refer to the application note *Electrostatic Discharge Sensitivity Measurement* (AN1181).

Table 34. ESD absolute maximum ratings(1) (2)

Symbol		C	Ratings	Conditions	Class	Max value	Unit
$V_{ESD(HBM)}$	C C	T	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	C C	T	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
$V_{ESD(CDM)}$	C C	T	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	V
						750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	P	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	10	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

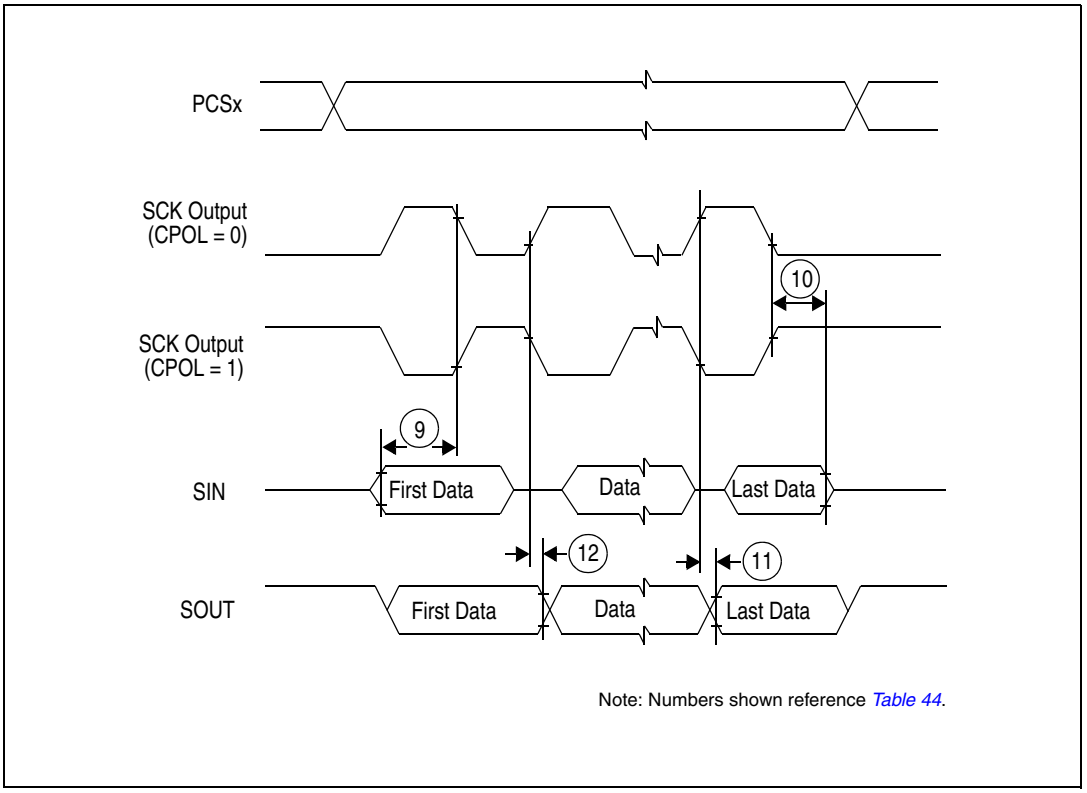

Figure 17. DSPI classic SPI timing – master, CPHA = 1

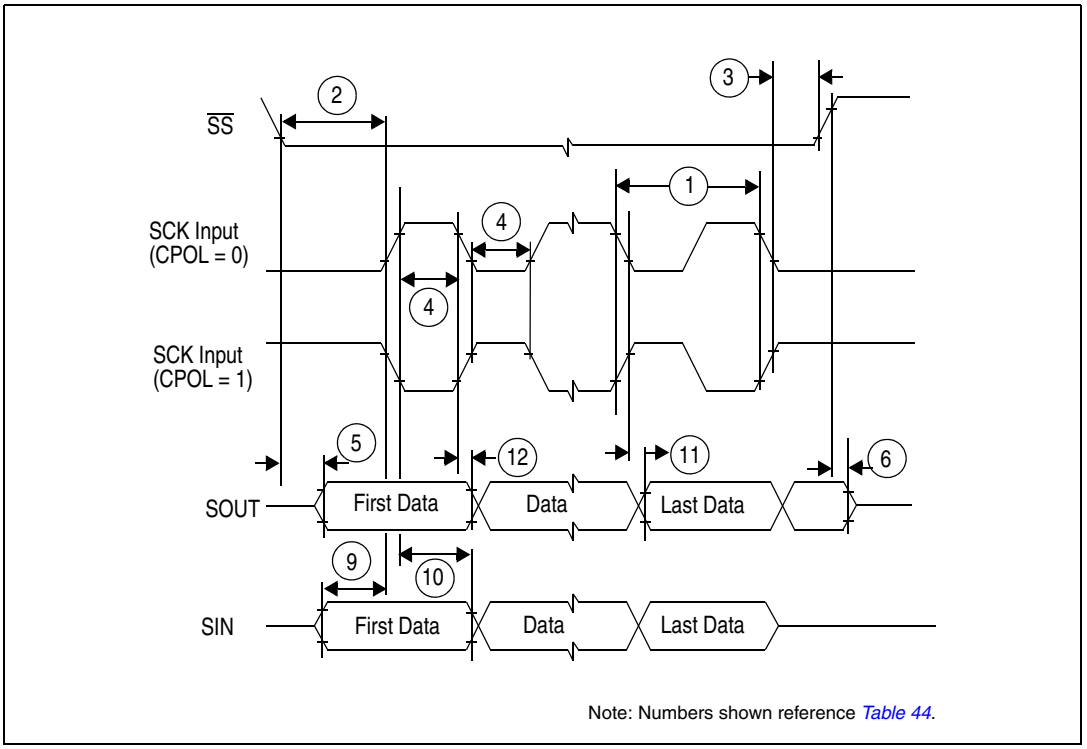

Figure 18. DSPI classic SPI timing – slave, CPHA = 0

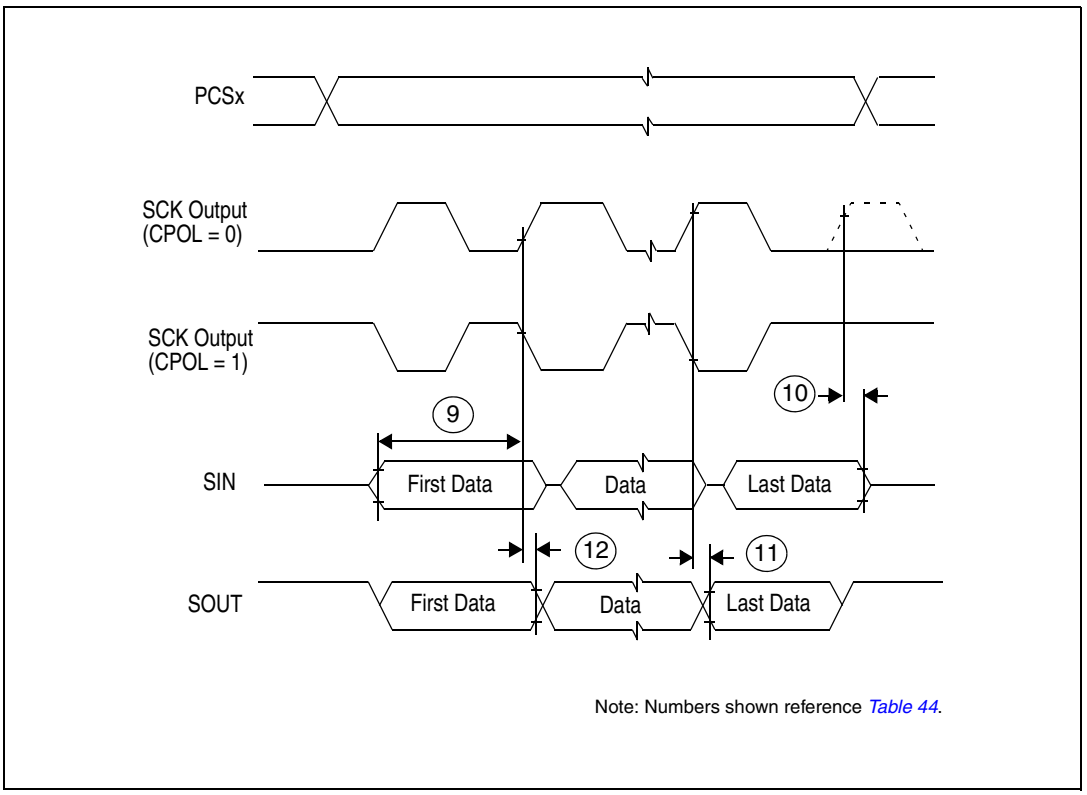

Figure 21. DSPI modified transfer format timing – master, CPHA = 1

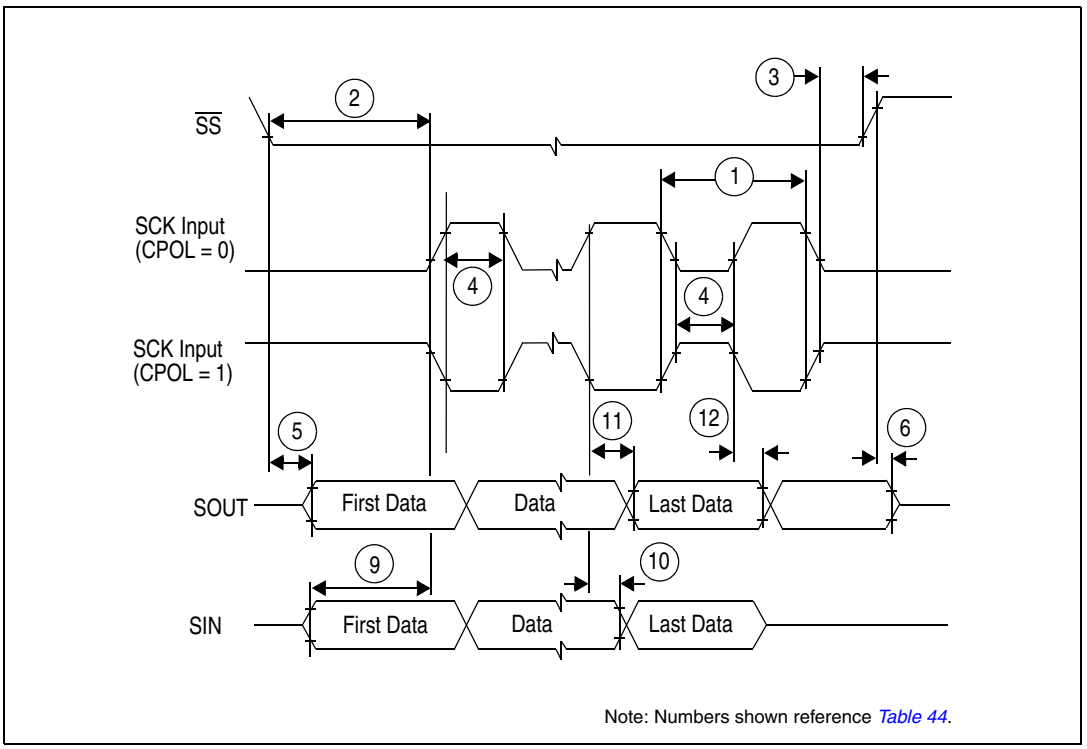

Figure 22. DSPI modified transfer format timing – slave, CPHA = 0

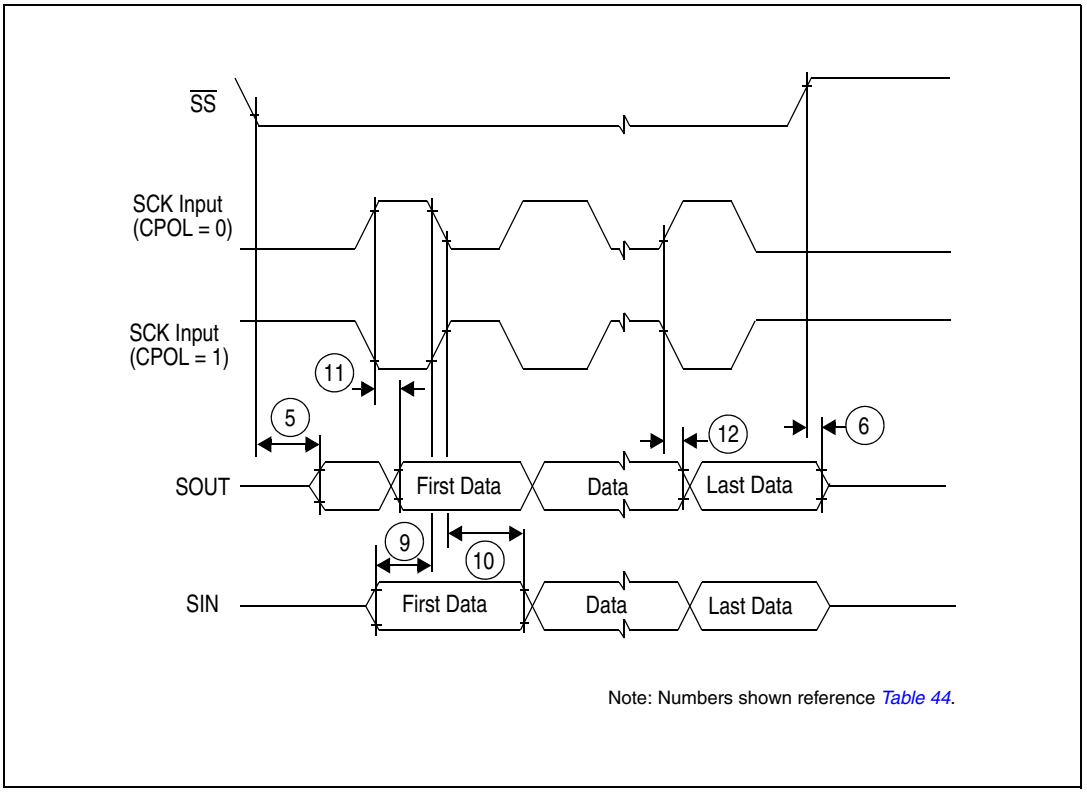

Figure 23. DSPI modified transfer format timing – slave, CPHA = 1

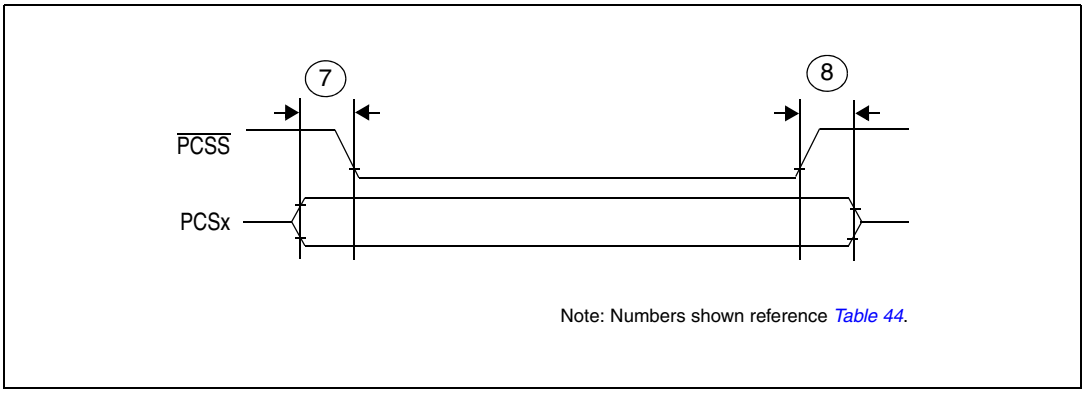

Figure 24. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

5 Package characteristics

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.2 Package mechanical data

5.2.1 LQFP100

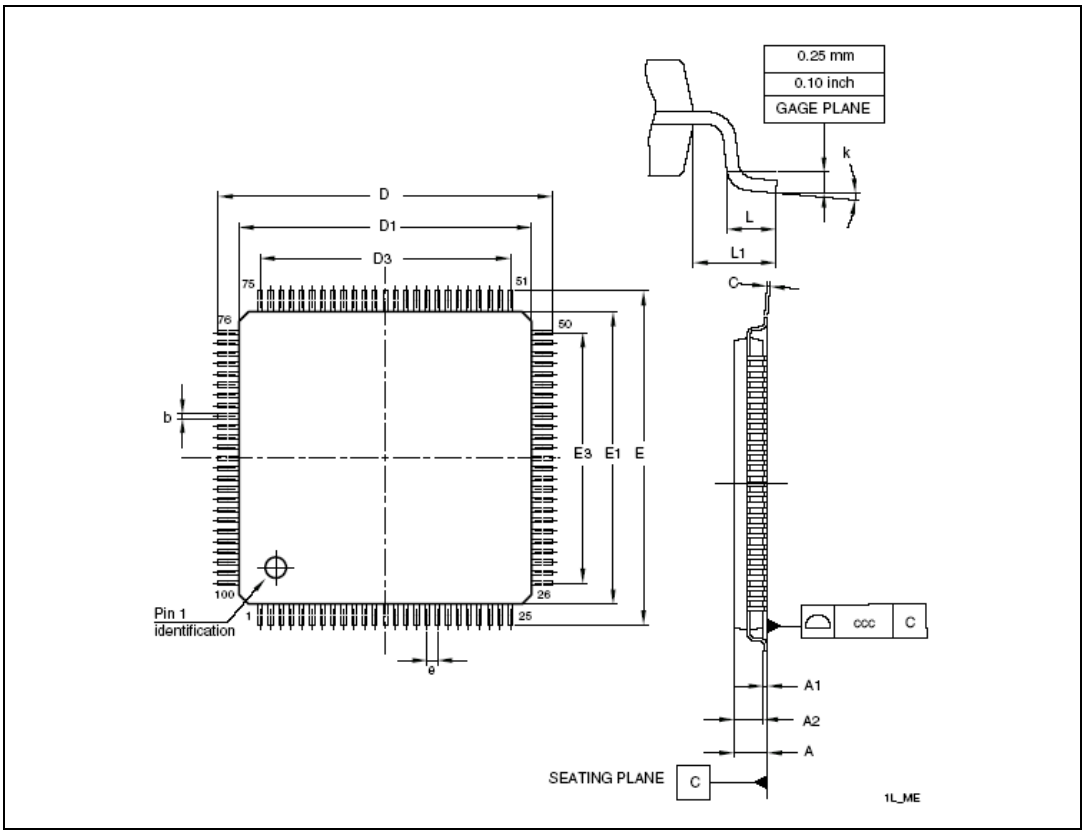

Figure 26. LQFP100 mechanical drawing

Table 50. Abbreviations (continued)

Abbreviation	Meaning
TDO	Test data output
TMS	Test mode select

Revision history

Table 51 summarizes revisions to this document.

Table 51. Document revision history

Date	Revision	Changes
09-Jul-2009	1	Initial release.
18-Feb-2010	2	Updated the following tables: - Absolute maximum ratings - Low voltage power domain electrical characteristics; - On-chip peripherals current consumption - DSPI characteristics; - JTAG characteristics; - ADC conversion characteristics; Inserted a note on “Flash power supply DC characteristics” section.
10-Aug-2010	3	“Features” section: Updated information concerning eMIOS, ADC, LINFlex, Nexus and low power capabilities “Pictus 512K device comparison” table: updated the “Execution speed” row “Pictus 512K series block diagram” figure: – updated max number of Crossbar Switches – updated Legend “Pictus 512K series block summary” table: added contents concernig the eDMA block “LQFP100 pin configuration (top view)” figure: – removed alternate functions – updated supply pins “LQFP64 pin configuration (top view)” figure: removed alternate functions Added “Pin muxing” section “NVUSRO register” section: Deleted “NVUSRO[WATCHDOG_EN] field description“ section “Recommended operating conditions (3.3 V)” table: – TV_{DD}: deleted min value – In footnote No. 3, changed capacitance value between V_{DD_BV} and V_{SS_LV} “Recommended operating conditions (5.0 V)” table: deleted TV_{DD} min value “LQFP thermal characteristics” table: changed $R_{\theta JC}$ values “I/O input DC electrical characteristics” table: – W_{FI}: updated max value – W_{NFI}: updated min value “I/O consumption” table: removed I_{DYNSEG} row Added “I/O weight” table “Program and erase specifications (Code Flash)” table: deleted T_{Bank_C} row

Table 51. Document revision history (continued)

Date	Revision	Changes
10-Aug-2010	3 (cont.)	Updated the following tables: – “Voltage regulator electrical characteristics” – “Low voltage monitor electrical characteristics” – “Low voltage power domain electrical characteristics” – “Start-up time/Switch-off time” – “Fast external crystal oscillator (4 to 16 MHz) electrical characteristics” – “FMPLL electrical characteristics” – “Fast internal RC oscillator (16 MHz) electrical characteristics” – “ADC conversion characteristics” – “On-chip peripherals current consumption” – “DSPI characteristics” “DSPI characteristics” section: removed “DSPI PCS strobe (PCSS) timing” figure Updated “Order codes” table Added “Order codes for engineering samples” table Updated “Commercial product code structure” table
16-Sep-2011	4	Formatting and editorial changes throughout Device comparison table: for the “Total timer I/O eMIOS”, changed “13 ch” to “14 ch” SPC560D30/SPC560D40 series block summary: – added definition for “AUTOSAR” acronym – changed “System watchdog timer” to “Software watchdog timer” LQFP64 pin configuration (top view): changed pin 6 from VPP_TEST to VSS_HV Added section “Pad configuration during reset phases” Added section “Voltage supply pins” Added section “Pad types” Added section “System pins” Renamed and updated section “Functional ports” (was previously section “Pin muxing”); update includes replacing all instances of WKUP with WKPU (WKPU is the correct abbreviation for Wakeup Unit) Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality Added section “NVUSRO[WATCHDOG_EN] field description” Absolute maximum ratings: Removed “C” column from table Replaced “TBD” with “—” in T_{VDD} min value cell of 3.3 V and 5 V recommended operating conditions tables LQFP thermal characteristics: removed $R_{\theta JB}$ single layer board conditions; updated footnote 4 I/O input DC electrical characteristics: removed footnote “All values need to be confirmed during device validation”; updated I_{LKG} characteristics