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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560d40l1c4e0y

List of figures

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] — LIN2TX ADC1_S[2]	SIUL eMIOS_0 — LINFlex_2 ADC	I/O I/O — O I	S	Tristate	47	74
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] — — EIRQ[16] ADC1_S[3] LIN2RX	SIUL eMIOS_0 — — SIUL ADC LINFlex_2	I/O I/O — — I I I	S	Tristate	48	75
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — — — EIRQ[17] SIN_0	SIUL — — — SIUL DSPI_0	I/O — — — I I	S	Tristate	22	31
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — CS3_1	SIUL DSPI_0 — DSPI_1	I/O O — I/O	M	Tristate	21	30
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	19	28
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10][3]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M	Tristate	18	27
Port B									
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — LIN2TX	SIUL FlexCAN_0 — LINFlex_2	I/O O — O	M	Tristate	14	23

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ADC1_S[4] WKPU[25][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	30	39
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ADC1_S[5] WKPU[26][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	29	38
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ADC1_S[6] WKPU[8][3]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	40
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC1_S[12]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	59
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC1_X[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	61
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC1_X[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	63
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC1_X[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	65

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] — — EIRQ[20]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	4
Port D									
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — —	GPIO[48] — — — WKPU[27][3] ADC1_P[4]	SIUL — — — WKPU ADC	I — — — I I	I	Tristate	—	41
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — —	GPIO[49] — — — WKPU[28][3] ADC1_P[5]	SIUL — — — WKPU ADC	I — — — I I	I	Tristate	—	42
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — ADC1_P[6]	SIUL — — — ADC	I — — — I	I	Tristate	—	43
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — ADC1_P[7]	SIUL — — — ADC	I — — — I	I	Tristate	—	44
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — ADC1_P[8]	SIUL — — — ADC	I — — — I	I	Tristate	—	45
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — ADC1_P[9]	SIUL — — — ADC	I — — — I	I	Tristate	—	46

capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:

– LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.

– LV_CFLA: Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.

– LV_DFLA: Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.

– LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

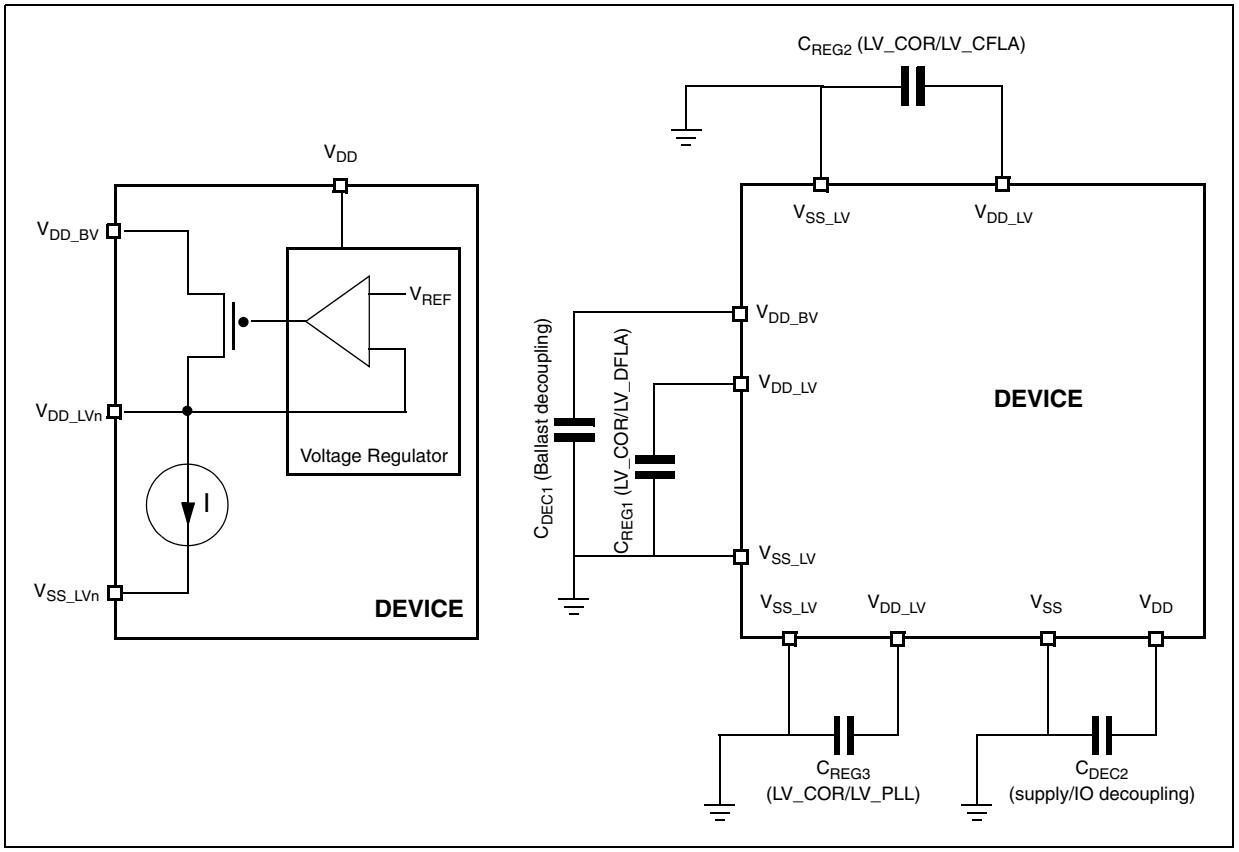

Figure 7. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see *Section 4.5, Recommended operating conditions*).

Table 24. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low-power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low-power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up[5]	—	—	—	300[6]	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.
3. This value is acceptable to guarantee operation from 4.5 V to 5.5 V.
4. External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.
5. In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 µs, depending on external capacitances to be loaded).

6. The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

4.9.2 Low voltage detector electrical characteristics

The device implements a power-on reset (POR) module to ensure correct power-up initialization, as well as five low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV3B monitors V_{DD_BV} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27_VREG in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual)
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

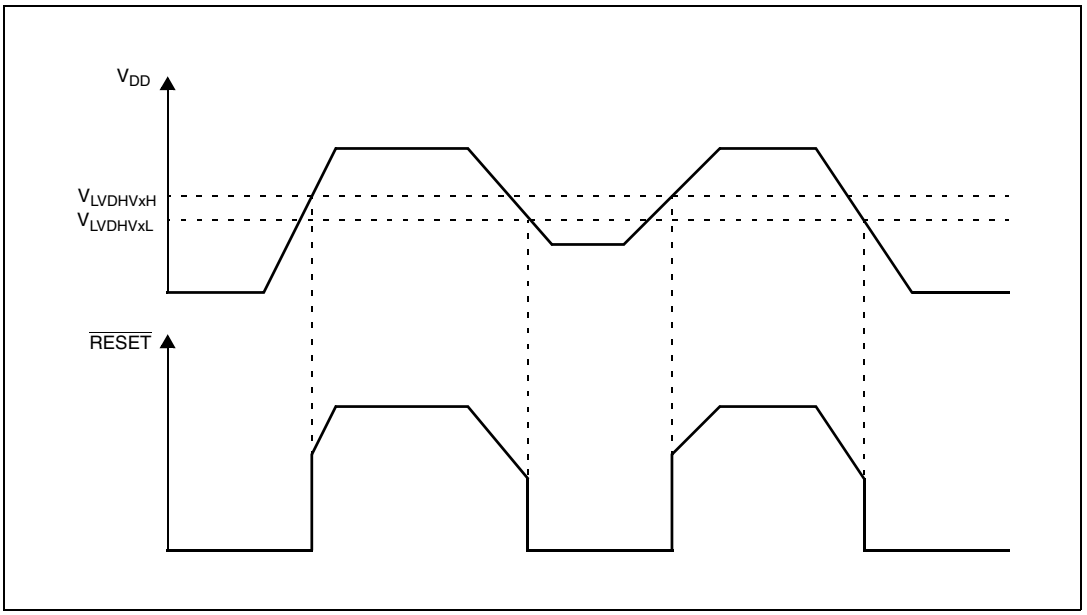

Figure 8. Low voltage detector vs reset

Table 25. Low voltage detector electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6	V
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95	V
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.6	—	2.9	V
$V_{LVDHV3BH}$	CC	P	LVDHV3B low voltage detector high threshold		—	—	2.95	V
$V_{LVDHV3BL}$	CC	P	LVDHV3B low voltage detector low threshold		2.6	—	2.9	V
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	V
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	V
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	1.16	V
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.16	V

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.10 Power consumption

Table 26 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 26. Power consumption on VDD_BV and VDD_HV

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—		—	90	130[3]	mA
I_{DDRUN}[4]	CC	T	RUN mode typical average current[5]	f_{CPU} = 8 MHz		—	7	—	mA
		T		f_{CPU} = 16 MHz		—	18	—	
		T		f_{CPU} = 32 MHz		—	29	—	
		P		f_{CPU} = 48 MHz		—	40	100	
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	8	15	mA
		P			T_A = 125 °C	—	14	25	
I_{DDSTOP}	CC	P	STOP mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	180	700[8]	µA
		D			T_A = 55 °C	—	500	—	
		D			T_A = 85 °C	—	1	6[8]	mA
		D			T_A = 105 °C	—	2	9[8]	
		P			T_A = 125 °C	—	4.5	12[8]	

Table 26. Power consumption on VDD_BV and VDD_HV (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{DDSTDBY}$	CC	P	STANDBY mode current[9]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	30	100	µA
		D			T_A = 55 °C	—	75	—	
		D			T_A = 85 °C	—	180	700	
		D			T_A = 105 °C	—	315	1000	
		P			T_A = 125 °C	—	560	1700	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
3. Higher current may be sinked by device during power-up and standby exit. Please refer to in-rush average current on *Table 24*.
4. RUN current measured with typical application with accesses on both flash memory and SRAM.
5. Only for the “P” classification: Code fetched from SRAM: serial IPs CAN and LIN in loop-back mode, DSPI as Master, PLL as system clock (3 × Multiplier) peripherals on (eMIOS/CTU/ADC) and running at maximum frequency, periodic SW/WDG timer reset enabled.
6. Data flash power down. Code flash in low power. SIRC (128 kHz) and FIRC (16 MHz) on. 10 MHz XTAL clock. FlexCAN: 0 ON (clocked but no reception or transmission). LINFlex: instances: 0, 1, 2 ON (clocked but no reception or transmission), instance: 3 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON.PIT ON. STM ON. ADC ON but no conversion except 2 analog watchdogs.
7. Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, HPVreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.
8. When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.
9. Only for the “P” classification: ULPVreg on, HP/LPVreg off, 16 KB SRAM on, device configured for minimum consumption, all possible modules switched off.

4.11 Flash memory electrical characteristics

The data flash operation depends strongly on the code flash operation. If code flash is switched-off, the data flash is disabled.

4.11.1 Program/Erase characteristics

Table 27 shows the program and erase characteristics.

Table 27. Program and erase specifications (code flash)

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$t_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	22	50	500	µs
$t_{16Kpperase}$	CC	C	16 KB block preprogram and erase time	—	300	500	5000	ms

Table 27. Program and erase specifications (code flash)

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$t_{32Kpperase}$	CC	C	32 KB block preprogram and erase time	—	400	600	5000	ms
$t_{128Kpperase}$	CC	C	128 KB block preprogram and erase time	—	800	1300	7500	ms
t_{esus}	CC	C	Erase suspend latency	—	—	30	30	µs

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.

Table 28. Program and erase specifications (data flash)

Symbol		C	Parameter	Value				Unit
				Min	Typ(1)	Initial max(2)	Max(3)	
$t_{swprogram}$	CC	C	Single word (32 bits) program time(4)	—	30	70	300	µs
$t_{16Kpperase}$	CC	C	16 KB block preprogram and erase time	—	700	800	1500	ms
t_{Bank_D}	CC	C	64 KB block preprogram and erase time	—	1900	2300	4800	ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.

Table 29. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block over the operating temperature range (T_J)	16 KB blocks	100000	—	—	cycles
				32 KB blocks	10000	100000	—	cycles
				128 KB blocks	1000	100000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	—	years
				Blocks with 1001–10000 P/E cycles	10	—	—	
				Blocks with 10001–100000 P/E cycles	5	—	—	

1. Ambient temperature averaged over application duration. It is recommended not to exceed the product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 30. Flash memory read access timing

Symbol		C	Parameter	Conditions (1)	Max	Unit
f_{CFREAD}	CC	P	Maximum working frequency for reading code flash memory at given number of wait states in worst conditions	2 wait states	48	MHz
		C		0 wait states	20	
f_{DFREAD}	CC	P	Maximum working frequency for reading data flash memory at given number of wait states in worst conditions	6 wait states	48	MHz

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.11.2 Flash power supply DC characteristics

Table 31 shows the power supply DC characteristics on external supply.

Note: Power supply for data flash is actually provided by code flash; this means that data flash cannot work if code flash is not powered.

Table 31. Flash power supply DC electrical characteristics

Symbol		C	Parameter	Conditions(1)		Value			Unit
						Min	Typ	Max	
I_{CFREAD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on read access	Flash module read f_{CPU} = 48 MHz	Code flash	—	—	33	mA
I_{DFREAD}	CC	D			Data flash	—	—	4	mA
I_{CFMOD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on matrix modification (program/erase)	Program/Erase on-going while reading flash registers, f_{CPU} = 48 MHz	Code flash	—	—	33	mA
I_{DFMOD}	CC	D			Data flash	—	—	6	mA
I_{FLPW}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} during flash low-power mode	—	Code flash	—	—	910	µA
I_{CFPWD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} during flash power-down mode	—	Code flash	—	—	125	µA
I_{DFPWD}	CC	D			Data flash	—	—	25	µA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.11.3 Start-up/Switch-off timings

Table 32. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
$t_{FLARSTEXIT}$	CC	T	Delay for flash module to exit reset mode	Code flash	—	—	125	µs
				Data flash	—	—	150	µs

Table 39. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C		—	—	10	µA
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
t_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	V_{DD} = 5.0 V ± 10%		—	1.1	2.0	µs
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		–1	—	1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation in temperature and supply with respect to f_{FIRC} at T_A = 55 °C in high-frequency configuration	—		–5	—	5	%

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

Table 40. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100	—	150	
I_{SIRC}[2]	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
t_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_s is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll t_s$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s, a constraints on R_L sizing is obtained:

Equation 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Table 42. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
TUEX[7]	CC	T	Total unadjusted error for extended channel	Without current injection	–10		10	LSB
		T		With current injection	–12		12	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. Analog and digital V_{SS} **must** be common (to be tied together externally).
3. V_{AINx} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.
4. Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.
5. During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sampling time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.
6. This parameter does not include the sampling time t_S, but only the time for determining the digital result and the time to load the result's register with the conversion result.
7. Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.18 On-chip peripherals

4.18.1 Current consumption

Table 43. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Typical value[2]	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	500 Kbyte/s	Total (static + dynamic) consumption: – FlexCAN in loop-back mode – XTAL at 8 MHz used as CAN engine clock source – Message sending period is 580 µs	8 × f_{periph} + 85	µA
				125 Kbyte/s		8 × f_{periph} + 27	µA
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: – eMIOS channel OFF – Global prescaler enabled		29 × f_{periph}	µA
				Dynamic consumption: – It does not change varying the frequency (0.003 mA)		3	µA
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: – LIN mode – Baudrate: 20 Kbyte/s		5 × f_{periph} + 31	µA

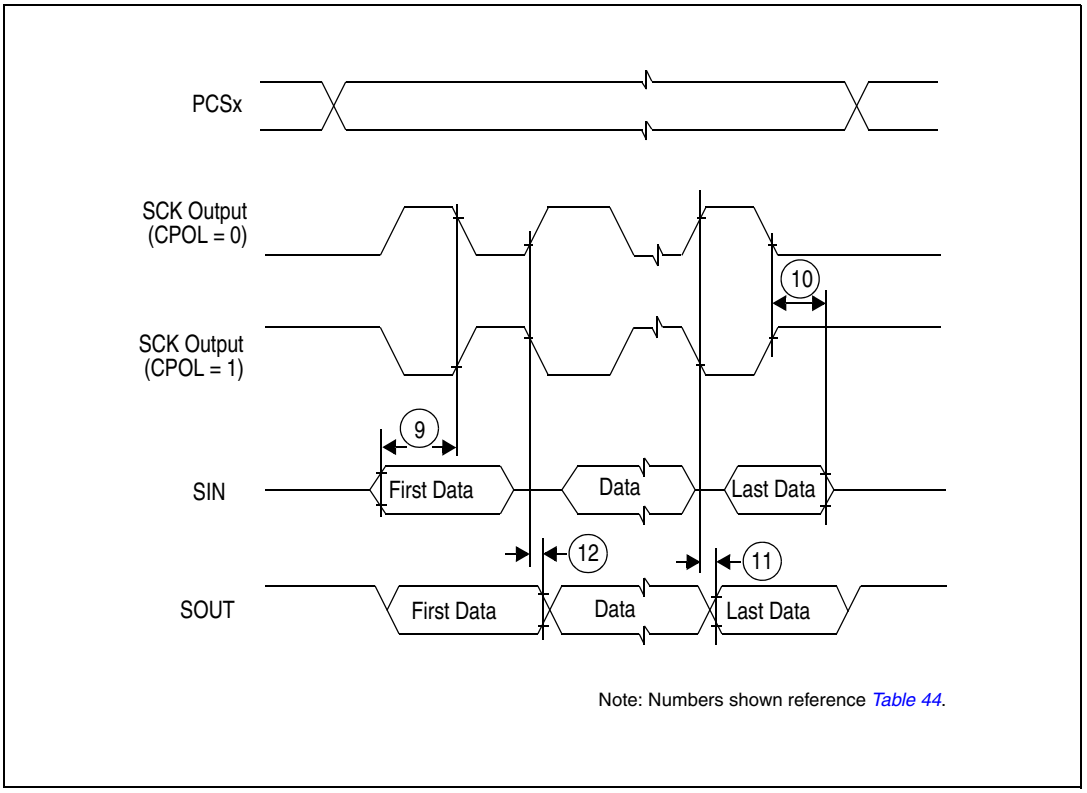

Figure 17. DSPI classic SPI timing – master, CPHA = 1

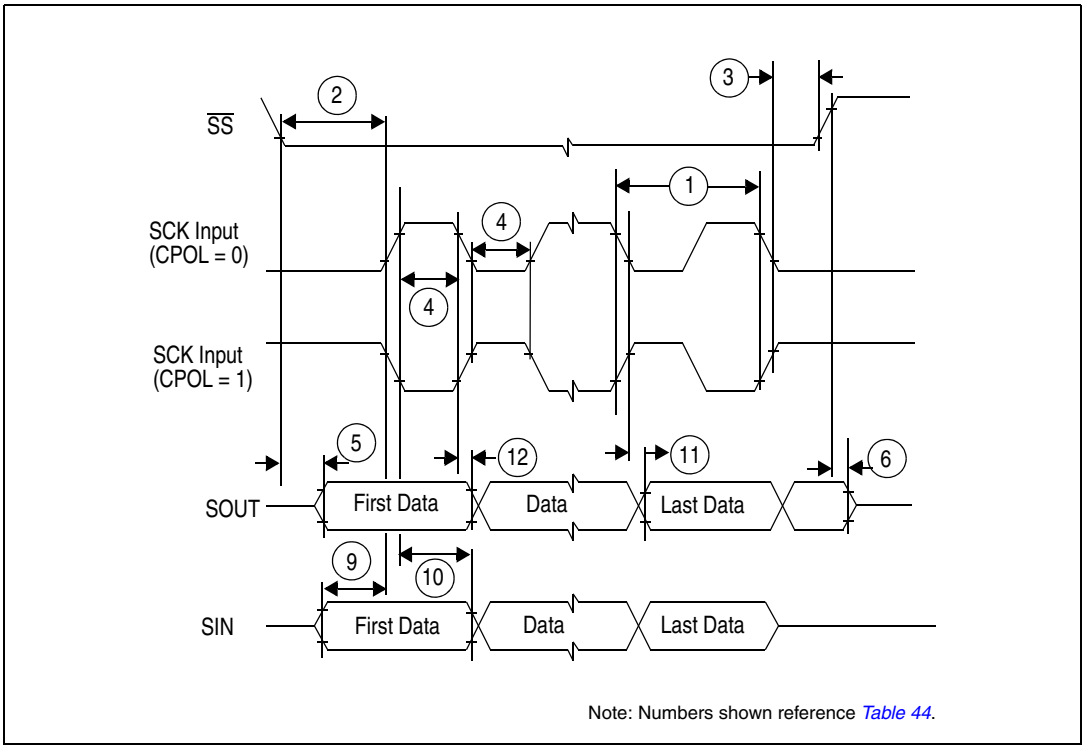

Figure 18. DSPI classic SPI timing – slave, CPHA = 0

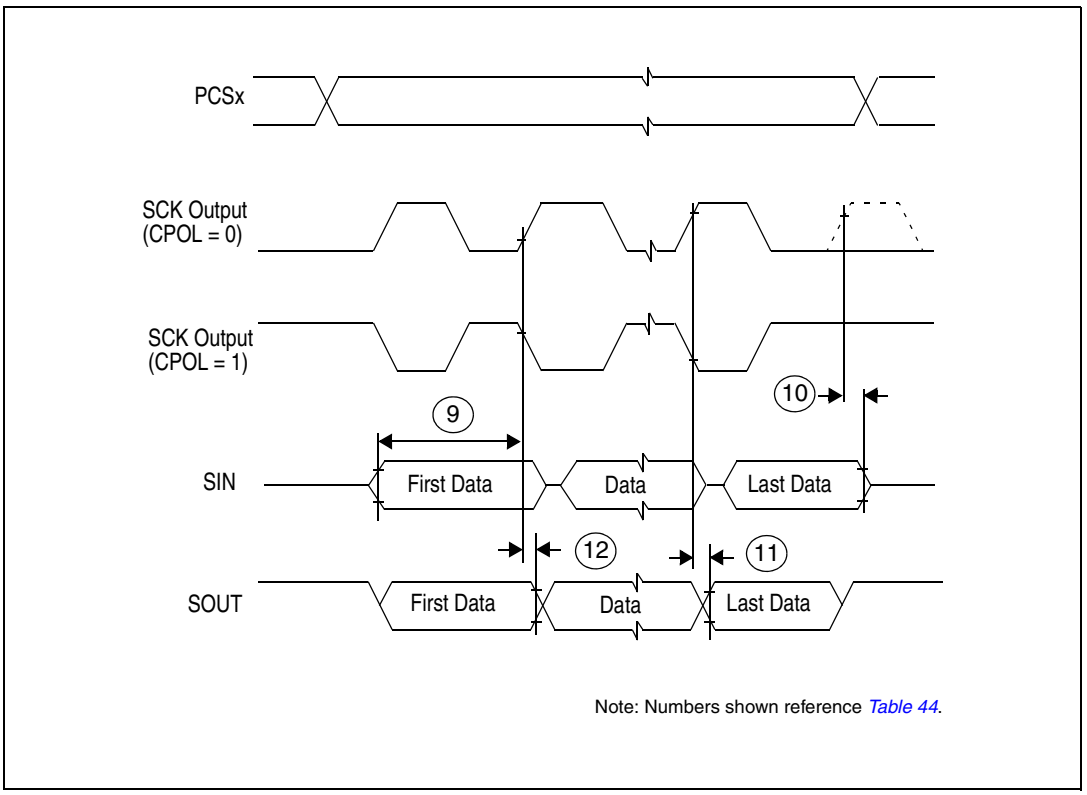

Figure 21. DSPI modified transfer format timing – master, CPHA = 1

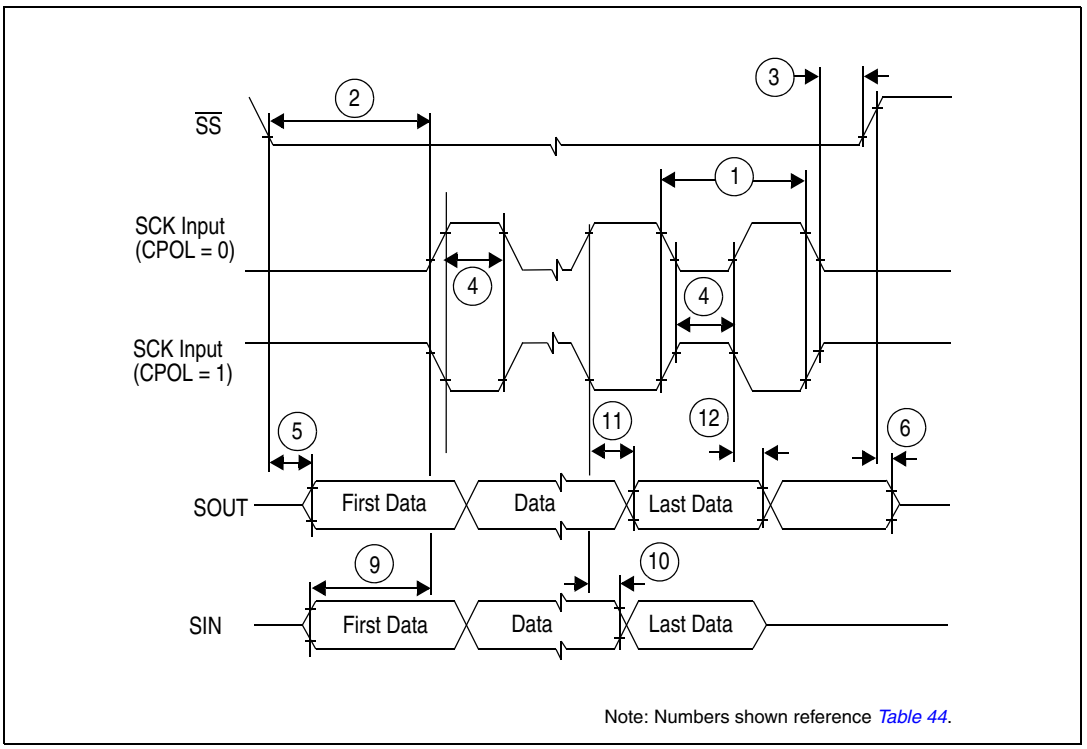

Figure 22. DSPI modified transfer format timing – slave, CPHA = 0

Table 46. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	**mm**			**inches**		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6 Ordering information

Table 48. Order codes

Order code	CPU	Memory		Package	Op. temp. (°C)	Speed (MHz)	Voltage	Packing
		Code flash / SRAM (KB)	Data flash					
SPC560D30L1B3E0X	e200z0h	128 / 12	4 x 16 KB	LQFP64	–40 to 105	32	3.3 / 5 V	Tape & Reel
SPC560D30L1C3E0X					–40 to 125			
SPC560D30L1B4E0X	e200z0h	128 / 12	4 x 16 KB	LQFP64	–40 to 105	48	3.3 / 5 V	Tape & Reel
SPC560D30L1C4E0X					–40 to 125			
SPC560D30L1B3E0X	e200z0h	128 / 12	4 x 16 KB	LQFP64	–40 to 105	32	3.3 / 5 V	Tape & Reel
SPC560D30L1C3E0X					–40 to 125			
SPC560D30L1B4E0X	e200z0h	128 / 12	4 x 16 KB	LQFP64	–40 to 105	48	3.3 / 5 V	Tape & Reel
SPC560D30L1C4E0X					–40 to 125			
SPC560D40L3B3E0X	e200z0h	256 / 16	4 x 16 KB	LQFP100	–40 to 105	32	3.3 / 5 V	Tape & Reel
SPC560D40L3C3E0X					–40 to 125			
SPC560D40L3B4E0X	e200z0h	256 / 16	4 x 16 KB	LQFP100	–40 to 105	48	3.3 / 5 V	Tape & Reel
SPC560D40L3C4E0X					–40 to 125			
SPC560D40L3B3E0X	e200z0h	256 / 16	4 x 16 KB	LQFP100	–40 to 105	32	3.3 / 5 V	Tape & Reel
SPC560D40L3C3E0X					–40 to 125			
SPC560D40L3B4E0X	e200z0h	256 / 16	4 x 16 KB	LQFP100	–40 to 105	48	3.3 / 5 V	Tape & Reel
SPC560D40L3C4E0X					–40 to 125			

Table 49. Order codes for engineering samples(1)

Order code	CPU	Memory		Package	Op. temp. (°C)	Speed (MHz)	Voltage	Packing
		Code flash / SRAM (KB)	Data flash					
SPC560D40L1-ENG	e200z0h	256 / 16	4 x 16 KB	LQFP64	–40 to 125	48	3.3 / 5 V	Tape & Reel
SPC560D40L3-ENG				LQFP100				

1. Engineering samples are suitable only for evaluation and development purpose but NOT for qualification and production. Their silicon version and maturity may vary until the product has reached qualification.

Table 51. Document revision history (continued)

Date	Revision	Changes
04-Feb-2013	6	Removed all instances of table footnote “All values need to be confirmed during device validation” *Section 4.1, Introduction*, removed Caution note. *Table 11 (Recommended operating conditions (3.3 V))*, added minimum value of T_{VDD} and footnote about it. *Table 12 (Recommended operating conditions (5.0 V))*, added minimum value of T_{VDD} and footnote about it. Updated *Section 4.17.2, Input impedance and ADC accuracy* In *Table 24*, changed $V_{LVDHV3L}$, $V_{LVDHV3BL}$ from 2.7 V to 2.6 V. Revised the *Table 28 (Flash module life)* Updated *Table 43, DSPI characteristics*, to add specifications 7 and 8, t_{PCSC} and t_{PASC}. Inserted *Figure 24*, *DSPI PCS strobe (PCSS) timing.*
17-Sep-2013	7	Updated Disclaimer.