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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560d40l3c4e0y

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions, please refer to *Table 6*.

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC1_X[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	67
Port C									
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	87
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F	Tristate	54	82
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 — — EIRQ[5]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	M	Tristate	50	78
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 —	GPIO[35] CS0_1 MA[0] — EIRQ[6]	SIUL DSPI_1 ADC — SIUL	I/O I/O O — I	S	Tristate	49	77
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 EIRQ[18]	SIUL — — — DSPI_1 SIUL	I/O — — — I I	M	Tristate	62	92
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 — — EIRQ[7]	SIUL DSPI_1 — — SIUL	I/O O — — I	M	Tristate	61	91
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	25

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction [2]	Pad type	RESET configuration	Pin number	
								LQFP64	LQFP100
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC SIUL	I/O I/O O O I	M	Tristate	—	95
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC SIUL	I/O I/O O O I	M	Tristate	—	96
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] — E0UC[22] —	SIUL — eMIOS_0 —	I/O — I/O —	M	Tristate	—	9
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 —	GPIO[73] — E0UC[23] — WKPU[7][3]	SIUL — eMIOS_0 — WKPU	I/O — I/O — I	S	Tristate	—	10
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] — CS3_1 — EIRQ[10]	SIUL — DSPI_1 — SIUL	I/O — O — I	S	Tristate	—	11
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 —	GPIO[75] E0UC[24] CS4_1 — WKPU[14][3]	SIUL eMIOS_0 DSPI_1 — WKPU	I/O I/O O — I	S	Tristate	—	13
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — —	GPIO[76] — — — ADC1_S[7] EIRQ[11]	SIUL — — — ADC SIUL	I/O — — — I I	S	Tristate	—	76
Port H									

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 7* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 7. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.4 Absolute maximum ratings

Table 11. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}	SR	Voltage on VDD_BV (regulator supply) pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment(1)	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
I_{CORELV}	SR	Low voltage static current sink through VDD_BV	—	—	150	mA
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

1. Supply segments are described in *Section 4.7.5, I/O pad current specification*.

Note: Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

Equation 1 $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

Equation 2 $P_D = K / (T_J + 273\ °C)$

Therefore, solving equations *1* and *2*:

Equation 3 $K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2$

Where:

K is a constant for the particular part, which may be determined from *Equation 3* by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations *1* and *2* iteratively for any value of T_A.

4.7 I/O pad electrical characteristics

4.7.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Input only pads—These pads are associated to ADC channels (ADC_P[X]) providing low input leakage.

Medium pads can use slow configuration to reduce electromagnetic emission except for PC[1], that is medium only, at the cost of reducing AC performance.

4.7.2 I/O input DC characteristics

Table 15 provides input DC electrical characteristics as described in *Figure 4*.

Table 21. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 22 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

Table 22. I/O weight[1]

Pad	LQFP100/LQFP64			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PB[3]	9%	9%	10%	10%
PC[9]	8%	8%	10%	10%

Table 22. I/O weight[1] (continued)

Pad	LQFP100/LQFP64			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PC[14]	8%	8%	10%	10%
PC[15]	8%	11%	9%	10%
PA[2]	8%	8%	9%	9%
PE[0]	7%	7%	9%	9%
PA[1]	7%	7%	8%	8%
PE[1]	7%	10%	8%	8%
PE[8]	6%	9%	8%	8%
PE[9]	6%	6%	7%	7%
PE[10]	6%	6%	7%	7%
PA[0]	5%	7%	6%	7%
PE[11]	5%	5%	6%	6%
PC[11]	7%	7%	9%	9%
PC[10]	8%	11%	9%	10%
PB[0]	8%	11%	9%	10%
PB[1]	8%	8%	10%	10%
PC[6]	8%	8%	10%	10%
PC[7]	8%	8%	10%	10%
PA[15]	8%	11%	9%	10%
PA[14]	7%	11%	9%	9%
PA[4]	7%	7%	8%	8%
PA[13]	7%	10%	8%	9%
PA[12]	7%	7%	8%	8%
PB[9]	1%	1%	1%	1%
PB[8]	1%	1%	1%	1%
PB[10]	5%	5%	6%	6%
PD[0]	1%	1%	1%	1%
PD[1]	1%	1%	1%	1%
PD[2]	1%	1%	1%	1%
PD[3]	1%	1%	1%	1%
PD[4]	1%	1%	1%	1%
PD[5]	1%	1%	1%	1%
PD[6]	1%	1%	1%	1%

6. The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

4.9.2 Low voltage detector electrical characteristics

The device implements a power-on reset (POR) module to ensure correct power-up initialization, as well as five low voltage detectors (LVDs) to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV3B monitors V_{DD_BV} to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27_VREG in device reference manual)
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual)
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

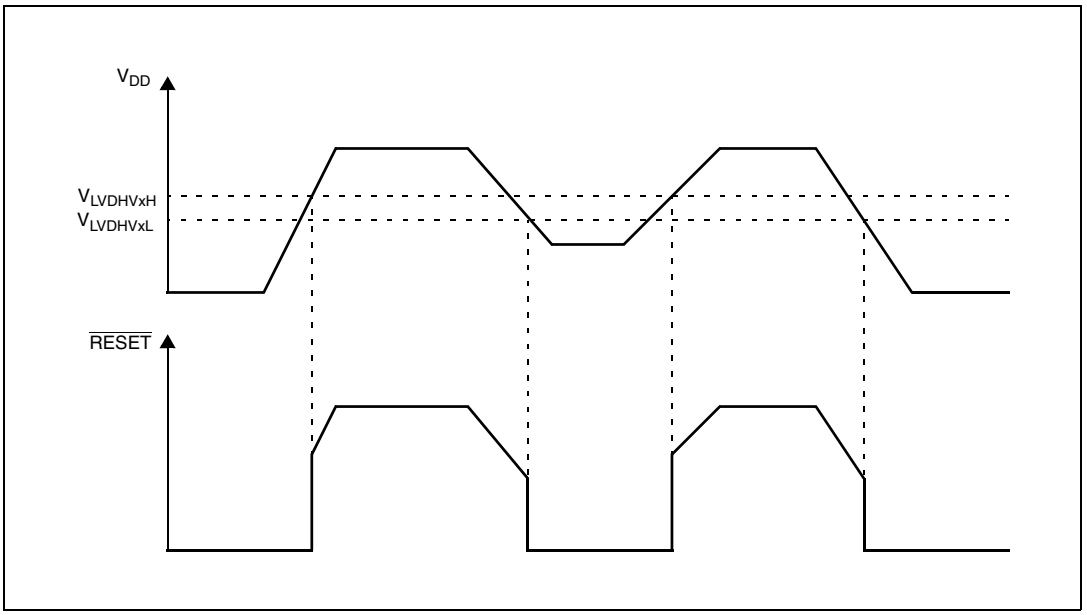


Figure 8. Low voltage detector vs reset

Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

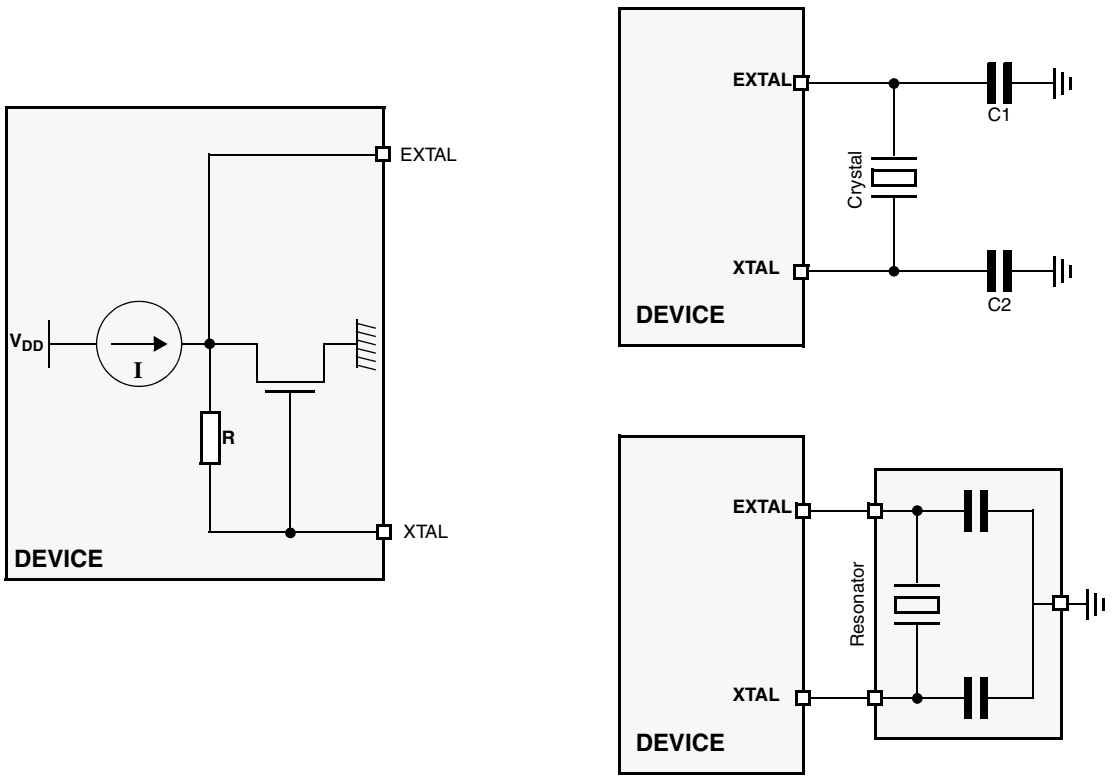
Table 35. Latch-up results

Symbol		C	Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

4.13 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. *Figure 9* describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 36 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.



Notes:
1. XTAL/EXTAL must not be directly used to drive external circuits
2. A series resistor may be required, according to crystal oscillator supplier recommendations.

Figure 9. Crystal oscillator and resonator connection scheme

4.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 38. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	48	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[2]	—	40	—	60	%
f_{PLLOUT}	CC	D	FMPLL output clock frequency	—	16	—	48	MHz
f_{VCO}[3]	CC	P	VCO frequency without frequency modulation	—	256	—	512	MHz
			VCO frequency with frequency modulation	—	245	—	533	
f_{CPU}	SR	—	System clock frequency	—	—	—	48	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 48 MHz, 4000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
3. Frequency modulation is considered ±4%.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 39. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[2]	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA

4.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

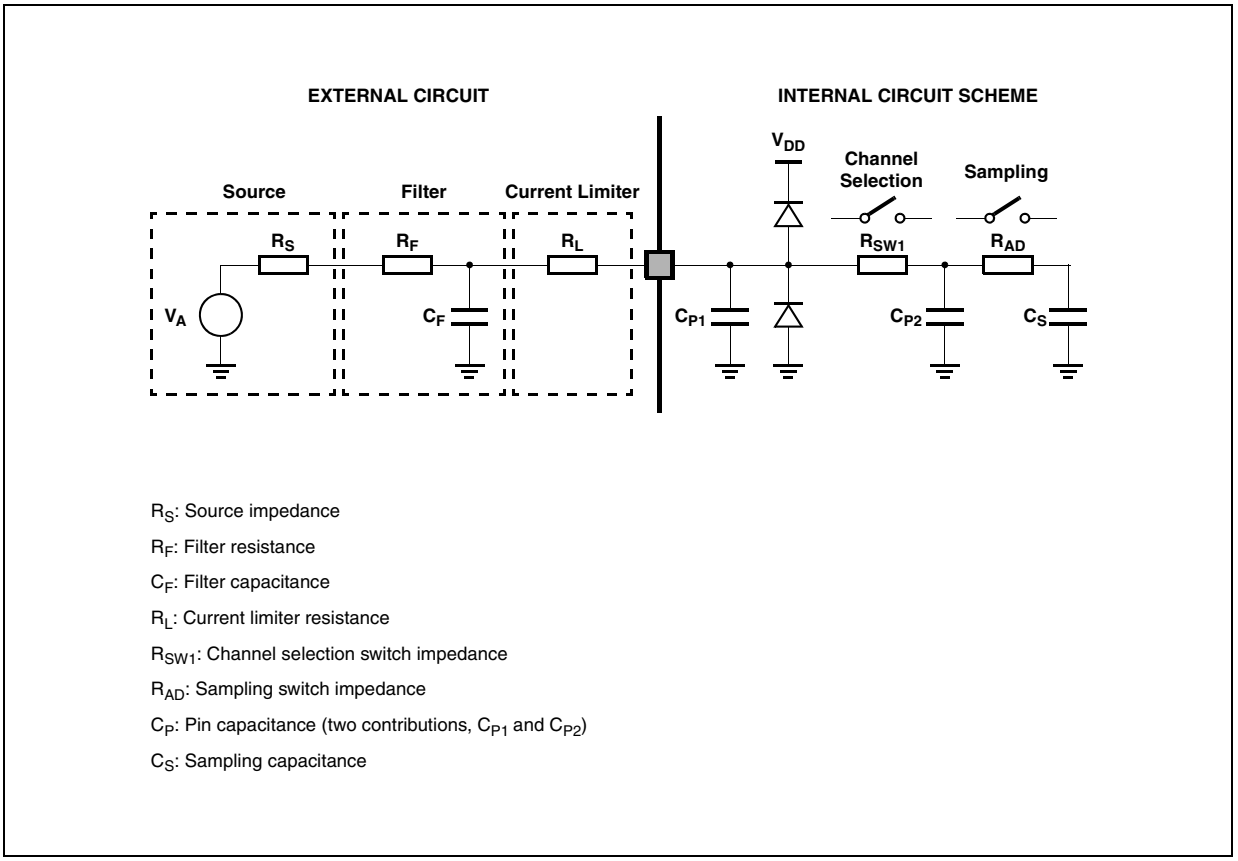
A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being C_S and C_{p2} substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{p2} equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (f_c × (C_S+C_{p2})), where f_c represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{p2}) and the sum of R_S + R_F, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on a resistive path.



R_S: Source impedance

R_F: Filter resistance

C_F: Filter capacitance

R_L: Current limiter resistance

R_{SW1}: Channel selection switch impedance

R_{AD}: Sampling switch impedance

C_P: Pin capacitance (two contributions, C_{P1} and C_{P2})

C_S: Sampling capacitance

Figure 12. Input equivalent circuit (precise channels)

Equation 12

$$C_F > 2048 \bullet C_S$$

4.17.3 ADC electrical characteristics

Table 41. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 42. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC} – 0.1	—	V_{DD_ADC} + 0.1	V
f_{ADC}	SR	—	ADC analog frequency	V_{DD} = 5.0 V	3.33	—	32 + 4%	MHz
				V_{DD} = 3.3 V	3.33	—	20 + 4%	
Δ_{ADC_SYS}	SR	—	ADC clock duty cycle (ipg_clk)	ADCLKSEL = 1[4]	45	—	55	%
t_{ADC_PU}	SR	—	ADC power up delay	—	—	—	1.5	µs
t_s	CC	T	Sampling time[5] V_{DD} = 3.3 V	f_{ADC} = 20 MHz, INPSAMP = 12	600	—	—	ns
				f_{ADC} = 3.33 MHz, INPSAMP = 255	—	—	76.2	µs
		T	Sampling time[5] V_{DD} = 5.0 V	f_{ADC} = 24 MHz, INPSAMP = 13	500	—	—	ns
				f_{ADC} = 3.33 MHz, INPSAMP = 255	—	—	76.2	µs

Table 43. On-chip peripherals current consumption(1) (continued)

Symbol		C	Parameter	Conditions		Typical value(2)	Unit
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on V_{DD_BV}	Ballast static consumption (only clocked)		1	µA
				Ballast dynamic consumption (continuous communication): – Baudrate: 2 Mbit/s – Transmission every 8 µs – Frame: 16 bits		16 × f_{periph}	µA
$I_{DD\_BV(ADC)}$	CC	T	ADC supply current on V_{DD_BV}	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	41 × f_{periph}	µA
					Ballast dynamic consumption (continuous conversion)(3)	5 × f_{periph}	µA
$I_{DD\_HV\_ADC(ADC)}$	CC	T	ADC supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	2 × f_{periph}	µA
					Analog dynamic consumption (continuous conversion)	75 × f_{periph} + 32	µA
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	8.21	mA
$I_{DD\_HV(PLL)}$	CC	T	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	30 × f_{periph}	µA

1. Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 48 MHz
2. f_{periph} is an absolute value.
3. During the conversion, the total current consumption is given from the sum of the static and dynamic consumption, i.e., (41 + 5) × f_{periph}.

4.18.2 DSPI characteristics

Table 44. DSPI characteristics(1)

No.	Symbol		C	Parameter		DSPI0/DSPI1			Unit
						Min	Typ	Max	
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	
			D		Master mode (MTFE = 1)	83	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	MHz

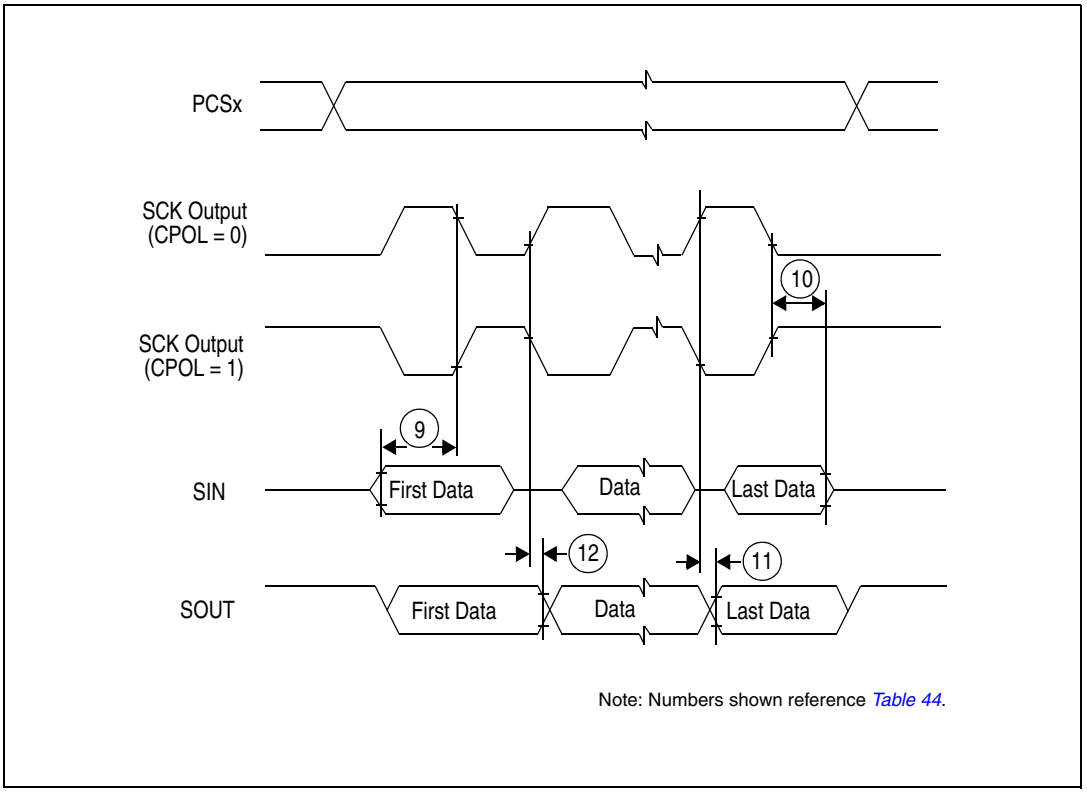


Figure 17. DSPI classic SPI timing – master, CPHA = 1

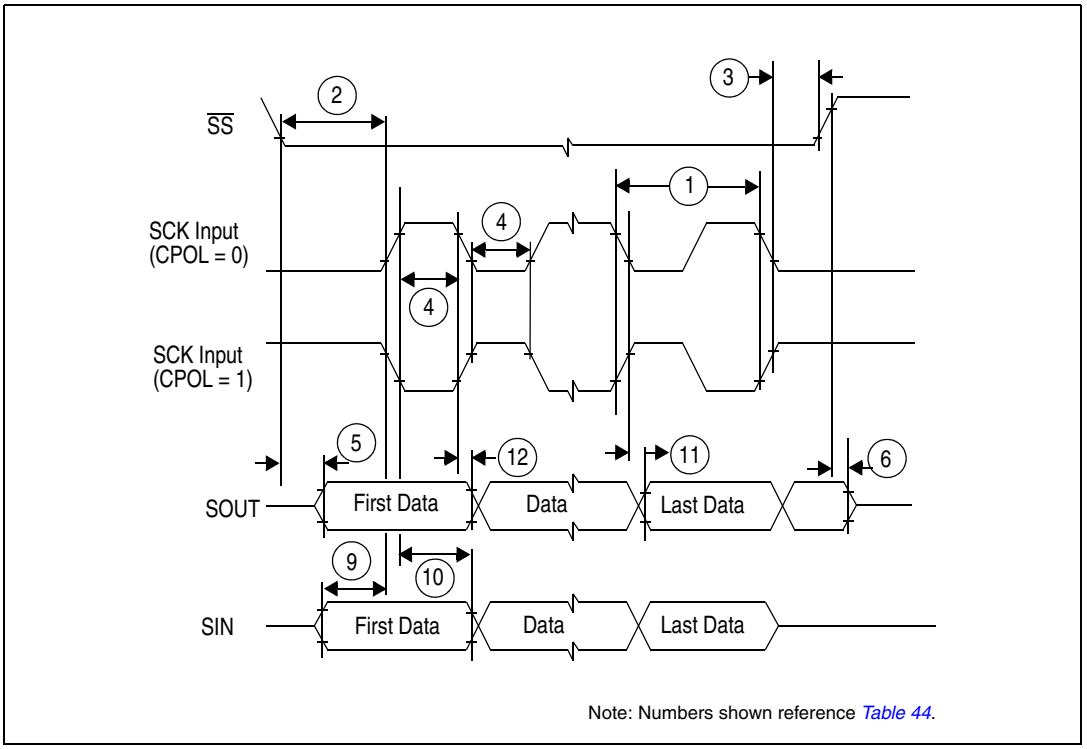


Figure 18. DSPI classic SPI timing – slave, CPHA = 0

5 Package characteristics

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.2 Package mechanical data

5.2.1 LQFP100

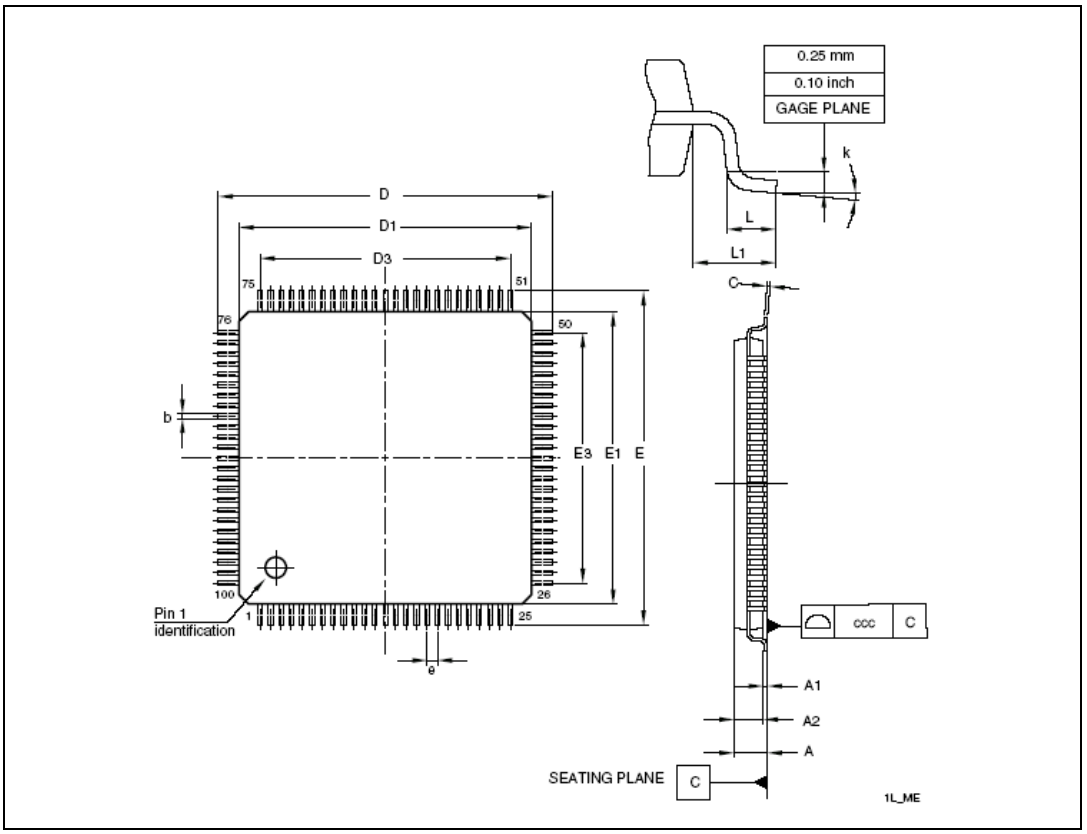


Figure 26. LQFP100 mechanical drawing

Table 51. Document revision history (continued)

Date	Revision	Changes
04-Feb-2013	6	Removed all instances of table footnote “All values need to be confirmed during device validation” *Section 4.1, Introduction*, removed Caution note. *Table 11 (Recommended operating conditions (3.3 V))*, added minimum value of T_{VDD} and footnote about it. *Table 12 (Recommended operating conditions (5.0 V))*, added minimum value of T_{VDD} and footnote about it. Updated *Section 4.17.2, Input impedance and ADC accuracy* In *Table 24*, changed $V_{LVDHV3L}$, $V_{LVDHV3BL}$ from 2.7 V to 2.6 V. Revised the *Table 28 (Flash module life)* Updated *Table 43, DSPI characteristics*, to add specifications 7 and 8, t_{PCSC} and t_{PASC}. Inserted *Figure 24*, *DSPI PCS strobe (PCSS) timing.*
17-Sep-2013	7	Updated Disclaimer.

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