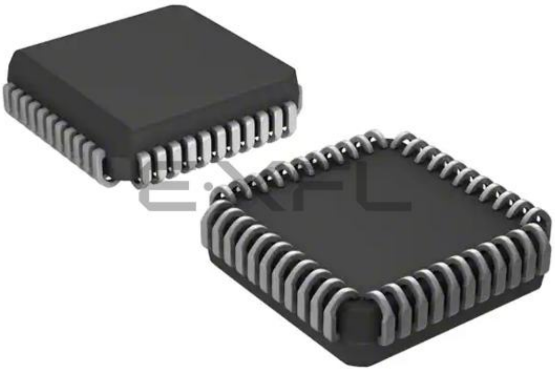
NXP USA Inc. - P89V51RB2FA,529 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89v51rb2fa-529

5.2 Pin description

Table 3. P89V51RB2/RC2/RD2 pin description

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
P0.0 to P0.7				I/O	**Port 0:** Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have ‘1’s written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to ‘1’s. Port 0 also receives the code bytes during the external host mode programming, and outputs the code bytes during the external host mode verification. External pull-ups are required during program verification or as a general purpose I/O port.
P0.0/AD0	39	37	43	I/O	**P0.0** — Port 0 bit 0.
				I/O	**AD0** — Address/data bit 0.
P0.1/AD1	38	36	42	I/O	**P0.1** — Port 0 bit 1.
				I/O	**AD1** — Address/data bit 1.
P0.2/AD2	37	35	41	I/O	**P0.2** — Port 0 bit 2.
				I/O	**AD2** — Address/data bit 2.
P0.3/AD3	36	34	40	I/O	**P0.3** — Port 0 bit 3.
				I/O	**AD3** — Address/data bit 3.
P0.4/AD4	35	33	39	I/O	**P0.4** — Port 0 bit 4.
				I/O	**AD4** — Address/data bit 4.
P0.5/AD5	34	32	38	I/O	**P0.5** — Port 0 bit 5.
				I/O	**AD5** — Address/data bit 5.
P0.6/AD6	33	31	37	I/O	**P0.6** — Port 0 bit 6.
				I/O	**AD6** — Address/data bit 6.
P0.7/AD7	32	30	36	I/O	**P0.7** — Port 0 bit 7.
				I/O	**AD7** — Address/data bit 7.
P1.0 to P1.7				I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 pins are pulled high by the internal pull-ups when ‘1’s are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. P1.5, P1.6, P1.7 have high current drive of 16 mA. Port 1 also receives the low-order address bytes during the external host mode programming and verification.
P1.0/T2	1	40	2	I/O	**P1.0** — Port 1 bit 0.
				I/O	**T2** — External count input to Timer/counter 2 or Clock-out from Timer/counter 2.
P1.1/T2EX	2	41	3	I/O	**P1.1** — Port 1 bit 1.
				I	**T2EX**: Timer/counter 2 capture/reload trigger and direction control.

Table 3. P89V51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
P1.2/ECI	3	42	4	I/O	**P1.2** — Port 1 bit 2.
				I	**ECI** — External clock input. This signal is the external clock input for the PCA.
P1.3/CEX0	4	43	5	I/O	**P1.3** — Port 1 bit 3.
				I/O	**CEX0** — Capture/compare external I/O for PCA Module 0. Each capture/compare module connects to a Port 1 pin for external I/O. When not used by the PCA, this pin can handle standard I/O.
P1.4/$\overline{SS}$/CEX1	5	44	6	I/O	**P1.4** — Port 1 bit 4.
				I	**$\overline{SS}$** — Slave port select input for SPI.
				I/O	**CEX1** — Capture/compare external I/O for PCA Module 1.
P1.5/MOSI/ CEX2	6	1	7	I/O	**P1.5** — Port 1 bit 5.
				I/O	**MOSI** — Master Output Slave Input for SPI.
				I/O	**CEX2** — Capture/compare external I/O for PCA Module 2.
P1.6/MISO/ CEX3	7	2	8	I/O	**P1.6** — Port 1 bit 6.
				I/O	**MISO** — Master Input Slave Output for SPI.
				I/O	**CEX3** — Capture/compare external I/O for PCA Module 3.
P1.7/SPICLK/ CEX4	8	3	9	I/O	**P1.7** — Port 1 bit 7.
				I/O	**SPICLK** — Serial clock input/output for SPI.
				I/O	**CEX4** — Capture/compare external I/O for PCA Module 4.
P2.0 to P2.7				I/O with internal pull-up	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins are pulled HIGH by the internal pull-ups when ‘1’s are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to ‘1’s. Port 2 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P2.0/A8	21	18	24	I/O	**P2.0** — Port 2 bit 0.
				O	**A8** — Address bit 8.
P2.1/A9	22	19	25	I/O	**P2.1** — Port 2 bit 1.
				O	**A9** — Address bit 9.
P2.2/A10	23	20	26	I/O	**P2.2** — Port 2 bit 2.
				O	**A10** — Address bit 10.
P2.3/A11	24	21	27	I/O	**P2.3** — Port 2 bit 3.
				O	**A11** — Address bit 11.
P2.4/A12	25	22	28	I/O	**P2.4** — Port 2 bit 4.
				O	**A12** — Address bit 12.

Table 3. P89V51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
P2.5/A13	26	23	29	I/O	**P2.5** — Port 2 bit 5.
				O	**A13** — Address bit 13.
P2.6/A14	27	24	30	I/O	**P2.6** — Port 2 bit 6.
				O	**A14** — Address bit 14.
P2.7/A15	28	25	31	I/O	**P2.7** — Port 2 bit 7.
				O	**A15** — Address bit 15.
P3.0 to P3.7				I/O with internal pull-up	**Port 3**: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins are pulled HIGH by the internal pull-ups when ‘1’s are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 3 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3.0/RXD	10	5	11	I	**P3.0** — Port 3 bit 0.
				I	**RXD** — Serial input port.
P3.1/TXD	11	7	13	O	**P3.1** — Port 3 bit 1.
				O	**TXD** — Serial output port.
P3.2/$\overline{\text{INT0}}$	12	8	14	I	**P3.2** — Port 3 bit 2.
				I	**$\overline{\text{INT0}}$** — External interrupt 0 input.
P3.3/$\overline{\text{INT1}}$	13	9	15	I	**P3.3** — Port 3 bit 3.
				I	**$\overline{\text{INT1}}$** — External interrupt 1 input.
P3.4/T0	14	10	16	I/O	**P3.4** — Port 3 bit 4.
				I	**T0** — External count input to Timer/counter 0.
P3.5/T1	15	11	17	I/O	**P3.5** — Port 3 bit 5.
				I	**T1** — External count input to Timer/counter 1.
P3.6/$\overline{\text{WR}}$	16	12	18	O	**P3.6** — Port 3 bit 6.
				O	**$\overline{\text{WR}}$** — External data memory write strobe.
P3.7/$\overline{\text{RD}}$	17	13	19	O	**P3.7** — Port 3 bit 7.
				O	**$\overline{\text{RD}}$** — External data memory read strobe.
$\overline{\text{PSEN}}$	29	26	32	I/O	**Program Store Enable**: $\overline{\text{PSEN}}$ is the read strobe for external program memory. When the device is executing from internal program memory, $\overline{\text{PSEN}}$ is inactive (HIGH). When the device is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. A forced HIGH-to-LOW input transition on the $\overline{\text{PSEN}}$ pin while the RST input is continually held HIGH for more than 10 machine cycles will cause the device to enter external host mode programming.

Table 3. P89V51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
RST	9	4	10	I	**Reset**: While the oscillator is running, a HIGH logic state on this pin for two machine cycles will reset the device. If the $\overline{\text{PSEN}}$ pin is driven by a HIGH-to-LOW input transition while the RST input pin is held HIGH, the device will enter the external host mode, otherwise the device will enter the normal operation mode.
$\overline{\text{EA}}$	31	29	35	I	**External Access Enable**: $\overline{\text{EA}}$ must be connected to V_{SS} in order to enable the device to fetch code from the external program memory. $\overline{\text{EA}}$ must be strapped to V_{DD} for internal program execution. The $\overline{\text{EA}}$ pin can tolerate a high voltage of 12 V.
ALE/$\overline{\text{PROG}}$	30	27	33	I/O	**Address Latch Enable:** ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input ($\overline{\text{PROG}}$) for flash programming. Normally the ALE[1] is emitted at a constant rate of $\frac{1}{6}$ the crystal frequency[2] and can be used for external timing and clocking. One ALE pulse is skipped during each access to external data memory. However, if AO is set to '1', ALE is disabled.
n.c.	-	6, 17, 28, 39	1, 12, 23, 34	I/O	not connected
XTAL1	19	15	21	I	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	14	20	O	**Crystal 2:** Output from the inverting oscillator amplifier.
V_{DD}	40	38	44	I	**Power supply**
V_{SS}	20	16	22	I	**Ground**

[1] ALE loading issue: When ALE pin experiences higher loading (>30 pF) during the reset, the microcontroller may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3 kΩ to 50 kΩ to V_{DD}, e.g., for ALE pin.

[2] For 6-clock mode, ALE is emitted at $\frac{1}{3}$ of crystal frequency.

to work during initial power up, before the voltage reaches the brownout detection level. The POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain active until cleared by software.

Following a power-on or external reset the P89V51RB2/RC2/RD2 will force the SWR and BSEL bits (FCF[1:0]) = 00. This causes the boot block to be mapped into the lower 8 kB of code memory and the device will execute the ISP code in the boot block and attempt to autobaud to the host. If the autobaud is successful the device will remain in ISP mode. If, after approximately 400 ms, the autobaud is unsuccessful the boot block code will check to see if the SoftICE flag is set (from a previous programming operation). If the SoftICE flag is set the device will enter SoftICE mode. If the SoftICE flag is cleared, the boot code will execute a software reset causing the device to execute the user code from block 0 starting at address 0000H. Note that an external reset applied to the RST pin has the same effect as a power-on reset.

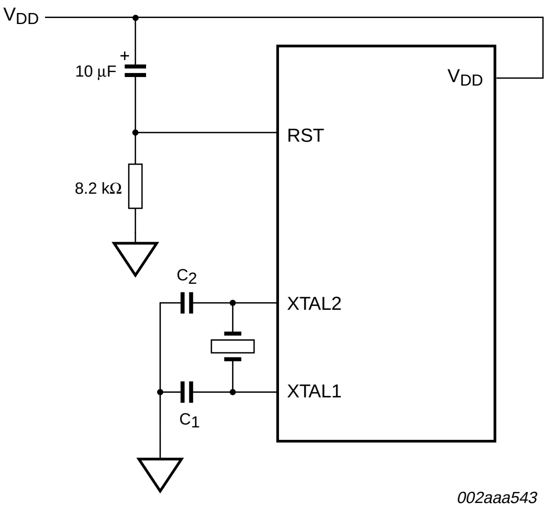


Fig 5. Power-on reset circuit

6.2.3 Software reset

A software reset is executed by changing the SWR bit (FCF.1) from ‘0’ to ‘1’. A software reset will reset the program counter to address 0000H and force both the SWR and BSEL bits (FCF[1:0]) = 10. This will result in the lower 8 kB of the user code memory being mapped into the user code memory space. Thus the user's code will be executed starting at address 0000H. A software reset will not change WDTC.2 or RAM data. Other SFRs will be set to their reset values.

6.2.4 Brownout detect reset

The device includes a brownout detection circuit to protect the system from severe supply voltage fluctuations. The P89V51RB2/RC2/RD2's brownout detection threshold is 2.35 V. When V_{DD} drops below this voltage threshold, the brownout detect triggers the circuit to generate a brownout interrupt but the CPU still runs until the supplied voltage returns to the brownout detection voltage V_{BOD}. The default operation for a brownout detection is to cause a processor reset.

V_{DD} must stay below V_{BOD} at least four oscillator clock periods before the brownout detection circuit will respond.

Brownout interrupt can be enabled by setting the EBO bit (IEA.3). If EBO bit is set and a brownout condition occurs, a brownout interrupt will be generated to execute the program at location 004BH. It is required that the EBO bit be cleared by software after the brownout interrupt is serviced. Clearing EBO bit when the brownout condition is active will properly reset the device. If brownout interrupt is not enabled, a brownout condition will reset the program to resume execution at location 0000H. A brownout detect reset will clear the BSEL bit (FCF.0) but will not change the SWR bit (FCF.1) and therefore will not change the banking of the lower 8 kB of user code memory space.

6.2.5 Watchdog reset

Like a brownout detect reset, the watchdog timer reset will clear the BSEL bit (FCF.0) but will not change the SWR bit (FCF.1) and therefore will not change the banking of the lower 8 kB of user code memory space.

The state of the SWR and BSEL bits after different types of resets is shown in Table 6. This results in the code memory bank selections as shown.

Table 6. Effects of reset sources on bank selection

Reset source	SWR bit result (FCF.1)	BSEL bit result (FCF.0)	Addresses from 0000H to 1FFFH	Addresses above 1FFFH
External reset	0	0	Boot code (in block 1)	User code (in block 0)
Power-on reset				
Watchdog reset	x	0	Retains state of SWR bit. If SWR, BSEL = 00 then uses boot code. If SWR, BSEL = 10 then uses user code.	
Brownout detect reset				
Software reset	1	0	User code (in block 0)	

6.2.6 Data RAM memory

The data RAM has 1024 B of internal memory. The device can also address up to 64 kB for external data memory.

6.2.7 Expanded data RAM addressing

The P89V51RB2/RC2/RD2 has 1 kB of RAM. See Figure 6 “Internal and external data memory structure” on page 19.

The device has four sections of internal data memory:

1. The lower 128 B of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 B of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 768 B (00H to 2FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit (see ‘Auxiliary function Register’ (AUXR) in Table 4 “Special function registers” on page 11).

Since the upper 128 B occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

Table 7. AUXR - Auxiliary register (address 8EH) bit allocation

Not bit addressable; Reset value 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	EXTRAM	AO

Table 8. AUXR - Auxiliary register (address 8EH) bit description

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to ‘0’ by user programs.
1	EXTRAM	Internal/External RAM access using MOVX @Ri/@DPTR. When ‘0’, core attempts to access internal XRAM with address specified in MOVX instruction. If address supplied with this instruction exceeds on-chip available XRAM, off-chip XRAM is going to be selected and accessed. When ‘1’, every MOVX @Ri/@DPTR instruction targets external data memory by default.
0	AO	ALE off: disables/enables ALE. AO = 0 results in ALE emitted at a constant rate of $\frac{1}{2}$ the oscillator frequency. In case of AO = 1, ALE is active only during a MOVX or MOVC.

When instructions access addresses in the upper 128 B (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

MOV@R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in ‘#data’ is written to RAM location 90H rather than port 1.

Direct Access:

MOV90H, #data; write data to P1

Data in ‘#data’ is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 B of memory is physically located on the chip and logically occupies the first 768 B of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 ($\overline{\text{WR}}$), P3.7 ($\overline{\text{RD}}$), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

MOVX@DPTR, A DPTR contains 0A0H

DPTR points to 0A0H and data in ‘A’ is written to address 0A0H of the expanded RAM rather than external memory. Access to external memory higher than 2FFH using the MOVX instruction will access external memory (0300H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX @DPTR generates a 16-bit address. This allows external addressing up the 64 kB. Port 2 provides the high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary read and write signals (P3.6 - $\overline{\text{WR}}$ and P3.7 - $\overline{\text{RD}}$) for external memory use. Table 9 shows external data memory $\overline{\text{RD}}$, $\overline{\text{WR}}$ operation with EXTRAM bit.

The stack pointer (SP) can be located anywhere within the 256 B of internal RAM (lower 128 B and upper 128 B). The stack pointer may not be located in any part of the expanded RAM.

Table 9. External data memory $\overline{\text{RD}}$, $\overline{\text{WR}}$ with EXTRAM bit[1]

AUXR	MOVX @DPTR, A or MOVX A, @DPTR		MOVX @Ri, A or MOVX A, @Ri
	ADDR < 0300H	ADDR ≥ 0300H	ADDR = any
EXTRAM = 0	$\overline{\text{RD}}$/$\overline{\text{WR}}$ not asserted	$\overline{\text{RD}}$/$\overline{\text{WR}}$ asserted	$\overline{\text{RD}}$/$\overline{\text{WR}}$ not asserted
EXTRAM = 1	$\overline{\text{RD}}$/$\overline{\text{WR}}$ asserted	$\overline{\text{RD}}$/$\overline{\text{WR}}$ asserted	$\overline{\text{RD}}$/$\overline{\text{WR}}$ asserted

[1] Access limited to ERAM address within OSPI to 0FFH; cannot access 100H to 02FFH.

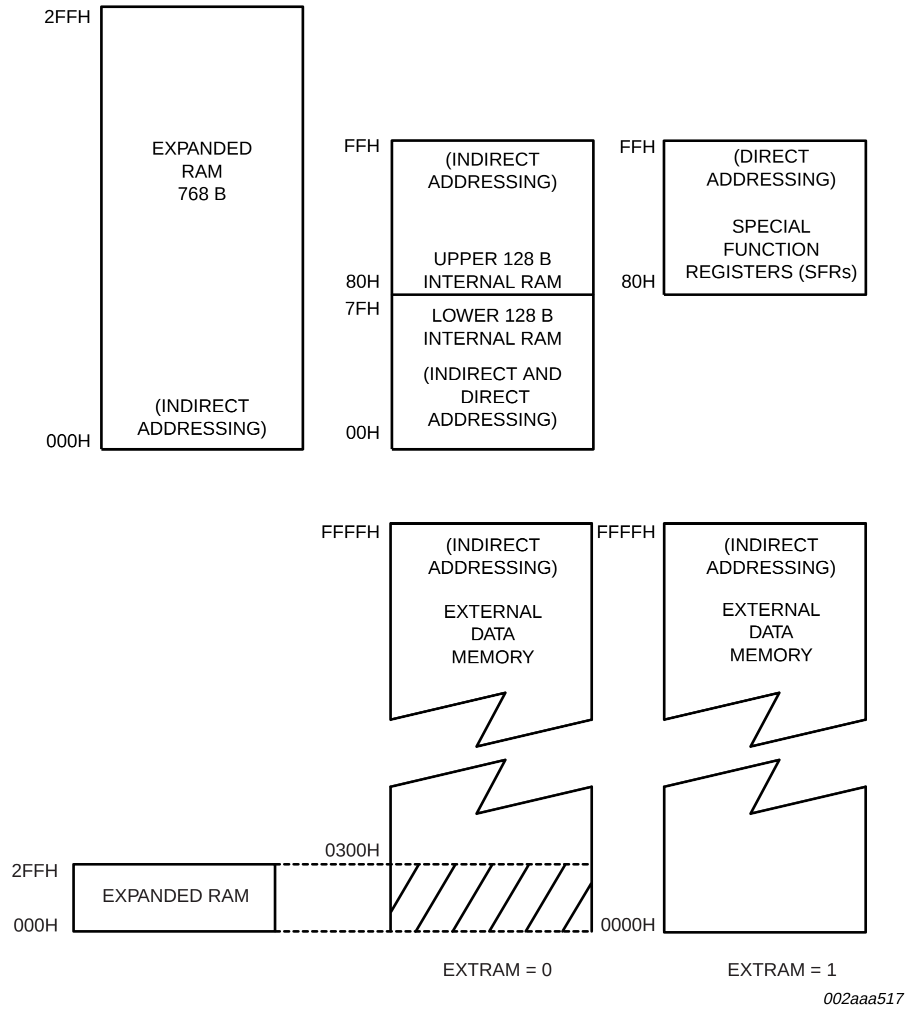


Fig 6. Internal and external data memory structure

6.2.8 Dual data pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS = 0, DPTR0 is selected; when DPS = 1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1 (see Figure 7).

Table 12. ISP hex record formats *…continued*

Record type	Command/data function
05	Miscellaneous Read Functions :02xxxx05ffsscc Where: 02 = number of bytes in the record xxxx = required field but value is a 'don't care' 05 = function code for misc read ffss = subfunction and selection code 0000 = read manufacturer id 0001 = read device id 1 0002 = read boot code version 0700 = read security bit (00 SoftICE serial number match 0 SB 0 Double Clock) cc = checksum Example: :020000050000F9 (display manufacturer id)
06	Direct Load of Baud Rate :02xxxx06HHLLcc Where: 02 = number of bytes in the record xxxx = required field but value is a 'don't care' HH = high byte of timer LL = low byte of timer cc = checksum Example: :02000006FFFFcc (load T2 = FFFF)
07	Reset serial number, erase user code, clear SoftICE mode :xxxxxx07cc Where: xxxxxx = required field but value is a 'don't care' 07 = reset serial number function cc = checksum Example: :00000007F9
08	Verify serial number :nnxxxx08ss..sscc Where: xxxxxx = required field but value is a 'don't care' 08 = verify serial number function ss..ss = serial number contents cc = checksum Example: :03000008010203EF (verify s/n = 010203)

Table 12. ISP hex record formats *…continued*

Record type	Command/data function
09	Write serial number :nnxxxx09ss..sscc Where: xxxxxx = required field but value is a ‘don’t care’ 09 = write serial number function ss..ss = serial number contents cc = checksum Example: :03000009010203EE (write s/n = 010203)
0A	Display serial number :xxxxxx0Acc Where: xxxxxx = required field but value is a ‘don’t care’ 0A = display serial number function cc = checksum Example: :0000000AF6
0B	Reset and run user code :xxxxxx0Bcc Where: xxxxxx = required field but value is a ‘don’t care’ 0B = Reset and run user code cc = checksum Example: :0000000BF5

6.3.5 Using the serial number

This device has the option of storing a 31 B serial number along with the length of the serial number (for a total of 32 B) in a non-volatile memory space. When ISP mode is entered, the serial number length is evaluated to determine if the serial number is in use. If the length of the serial number is programmed to either 00H or FFH, the serial number is considered not in use. If the serial number is in use, reading, programming, or erasing of the user code memory or the serial number is blocked until the user transmits a ‘verify serial number’ record containing a serial number and length that matches the serial number and length previously stored in the device. The user can reset the serial number to all zeros and set the length to zero by sending the ‘reset serial number' record. In addition, the ‘reset serial number’ record will also erase all user code.

6.3.6 IAP method

Several IAP calls are available for use by an application program to permit selective erasing, reading and programming of flash sectors, security bit, configuration bytes, and device id. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller’s registers before making a call to PGM_MTP at 1FF0H. The IAP calls are shown in Table 13.

Table 21. T2CON - Timer/counter 2 control register (address C8H) bit description *…continued*

Bit	Symbol	Description
4	TCLK	Transmit clock flag. When set, causes the UART to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	Start/stop control for Timer 2. A logic ‘1’ enables the timer to run.
1	$C/\overline{T}2$	Timer or counter select. (Timer 2) 0 = internal timer (f_{osc} / 6) 1 = external event counter (falling edge triggered; external clock’s maximum rate = f_{osc} / 12
0	$CP/\overline{RL}2$	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 22. T2MOD - Timer 2 mode control register (address C9H) bit allocation

Not bit addressable; Reset value: XX00 0000B

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T2OE	DCEN

Table 23. T2MOD - Timer 2 mode control register (address C9H) bit description

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to ‘0’ by user programs.
1	T2OE	Timer 2 Output Enable bit. Used in programmable clock-out mode only.
0	DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

6.5.1 Capture mode

In the Capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0 Timer 2 is a 16-bit timer or counter (as selected by $C/\overline{T}2$ in T2CON) which upon overflowing sets bit TF2, the Timer 2 overflow bit.

The capture mode is illustrated in Figure 12.

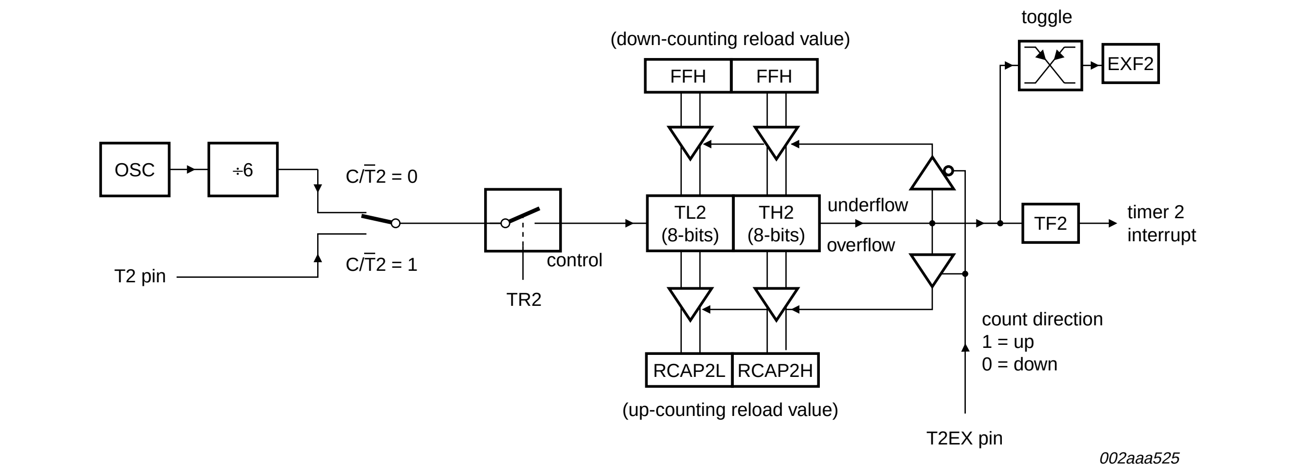


Fig 14. Timer 2 in Auto Reload mode (DCEN = 1)

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2. The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed.

6.5.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1.0). This pin, besides being a regular I/O pin, has two additional functions. It can be programmed:

1. To input the external clock for Timer/counter 2, or
2. To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the Timer/counter 2 as a clock generator, bit C/T̄2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{OscillatorFrequency}{2 \times (65536 \angle (RCAP2H,\ RCAP2L))} \qquad (2)$$

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator.

6.5.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART) transmit and receive baud rates to be derived from either Timer 1 or Timer 2 (See Section 6.6 “UARTs” on page 37 for details). When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When

Table 37. CMOD - PCA counter mode register (address D9H) count pulse select

CPS1	CPS0	Select PCA input
0	0	0 Internal clock, f_{osc} / 6
0	1	1 Internal clock, f_{osc} / 2
1	0	2 Timer 0 overflow
1	1	3 External clock at ECI/P1.2 pin (max rate = f_{osc} / 4)

Table 38. CCON - PCA counter control register (address 0D8H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0

Table 39. CCON - PCA counter control register (address 0D8H) bit description

Bit	Symbol	Description
7	CF	PCA counter overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
6	CR	PCA counter run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
5	-	Reserved for future use. Should be set to ‘0’ by user programs.
4	CCF4	PCA Module 4 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
3	CCF3	PCA Module 3 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
2	CCF2	PCA Module 2 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
1	CCF1	PCA Module 1 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
0	CCF0	PCA Module 0 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.

Table 40. CCAPMn - PCA modules compare/capture register (address CCAPM0 0DAH, CCAPM1 0DBH, CCAPM2 0DCH, CCAPM3 0DDH, CCAPM4 0DEH) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn

Table 41. CCAPMn - PCA modules compare/capture register (address CCAPM0 0DAH, CCAPM1 0DBH, CCAPM2 0DCH, CCAPM3 0DDH, CCAPM4 0DEH) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to ‘0’ by user programs.
6	ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
5	CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
4	CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
3	MATn	Match. When MATn = 1 a match of the PCA counter with this module’s compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.

6.10 Security bit

The Security Bit protects against software piracy and prevents the contents of the flash from being read by unauthorized parties in Parallel Programmer mode. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory.

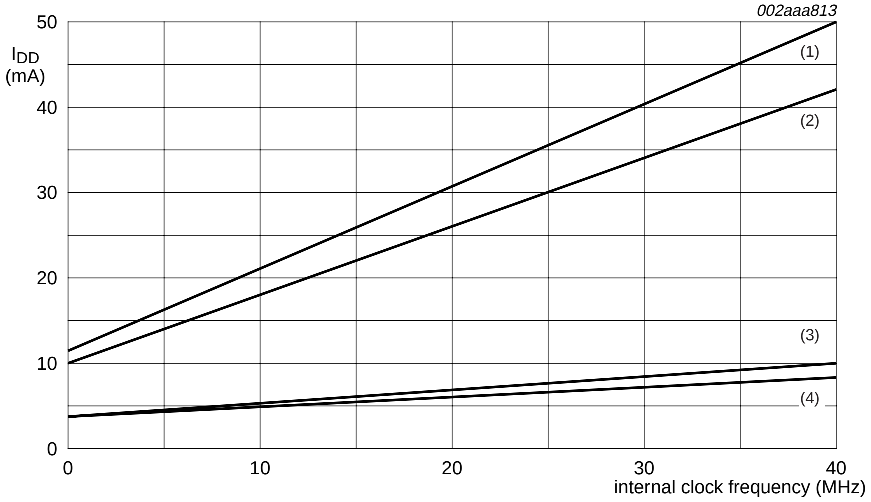
When the Security Bit is activated all parallel programming commands except for Chip-Erase are ignored (thus the device cannot be read). However, ISP reading, writing, or erasing of the user's code can still be performed if the serial number and length has not been programmed. **Therefore, when a user requests to program the Security Bit, the programmer should prompt the user and program a serial number into the device.**

6.11 Interrupt priority and polling sequence

The device supports eight interrupt sources under a four level priority scheme. Table 43 summarizes the polling sequence of the supported interrupts. Note that the SPI serial interface and the UART share the same interrupt vector. (See Figure 27).

Table 43. Interrupt polling sequence

Description	Interrupt flag	Vector address	Interrupt enable	Interrupt priority	Service priority	Wake-up power-down
Ext. Int0	IE0	0003H	EX0	PX0/H	1 (highest)	yes
Brownout	-	004BH	EBO	PBO/H	2	no
T0	TF0	000BH	ET0	PT0/H	3	no
Ext. Int1	IE1	0013H	EX1	PX1/H	4	yes
T1	TF1	001BH	ET1	PT1/H	5	no
PCA	CF/CCFn	0033H	EC	PPCH	6	no
UART/SPI	TI/RI/SPIF	0023H	ES	PS/H	7	no
T2	TF2, EXF2	002BH	ET2	PT2/H	8	no



(1) Maximum active I_{DD}

(2) Maximum idle I_{DD}

(3) Typical active I_{DD}

(4) Typical idle I_{DD}

Fig 30. I_{DD} vs. frequency

9.1 Explanation of symbols

Each timing symbol has 5 characters. The first character is always a ‘T’ (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A — Address

C — Clock

D — Input data

H — Logic level HIGH

I — Instruction (program memory contents)

L — Logic level LOW or ALE

P — $\overline{\text{PSEN}}$

Q — Output data

R — $\overline{\text{RD}}$ signal

T — Time

V — Valid

W — $\overline{\text{WR}}$ signal

X — No longer a valid logic level

Z — High impedance (Float)

Example:

t_{AVLL} = Address valid to ALE LOW time

t_{LLPL} = ALE LOW to $\overline{\text{PSEN}}$ LOW time

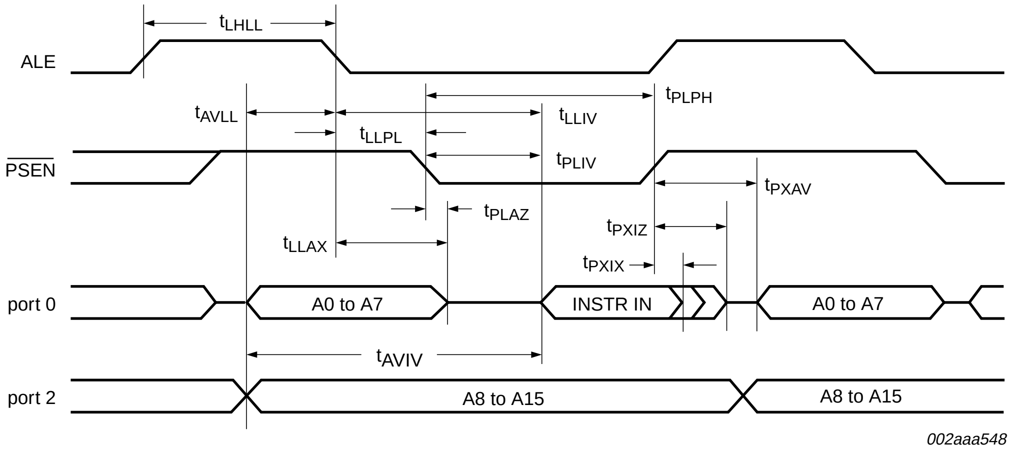


Fig 31. External program memory read cycle

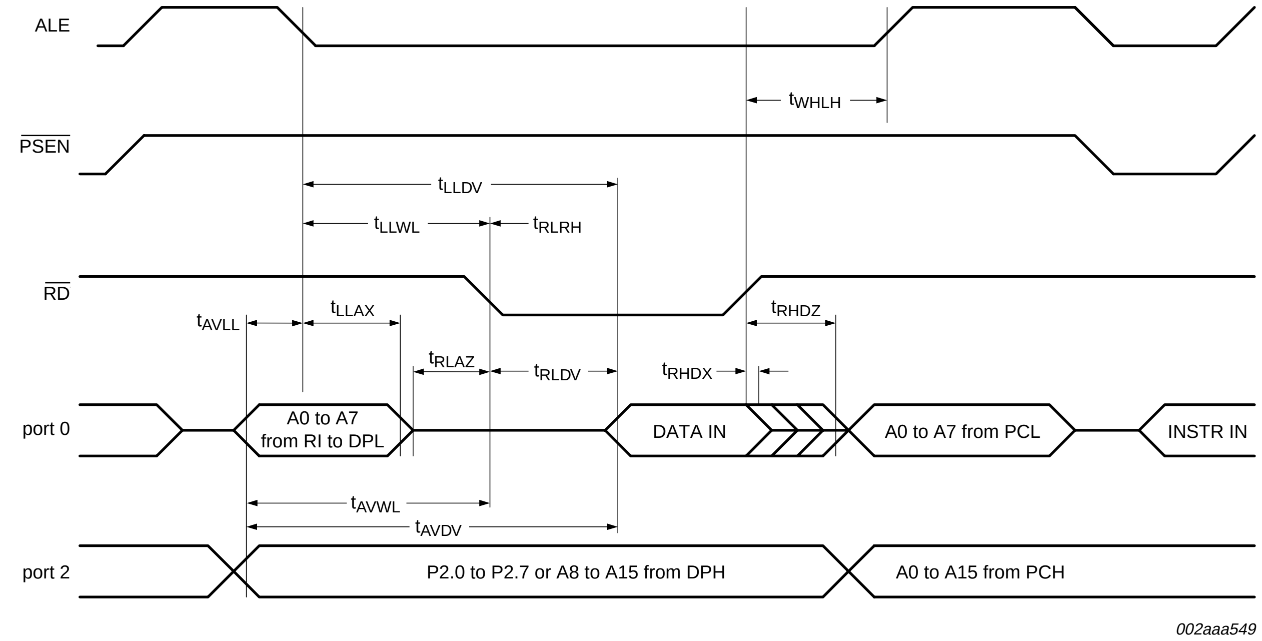


Fig 32. External data memory read cycle

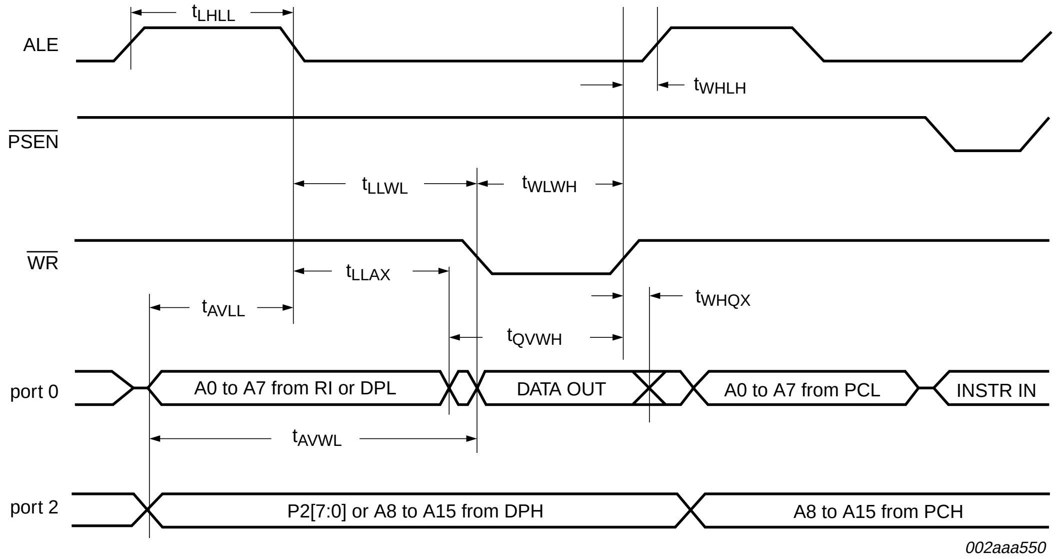


Fig 33. External data memory write cycle

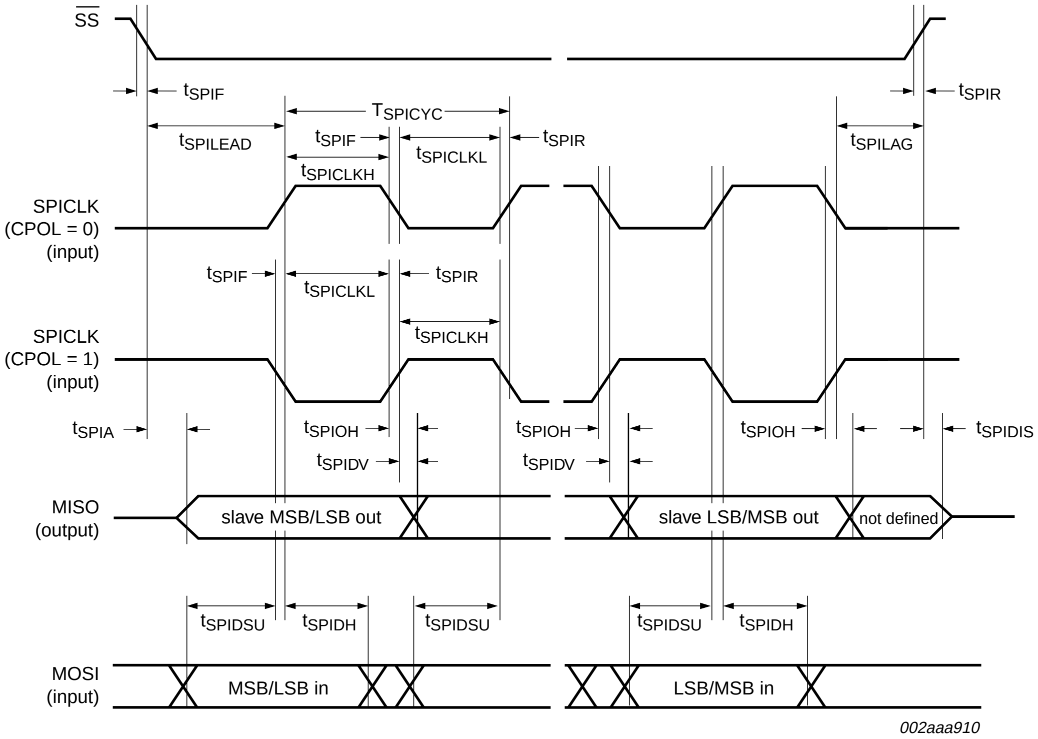


Fig 38. SPI slave timing (CPHA = 0)

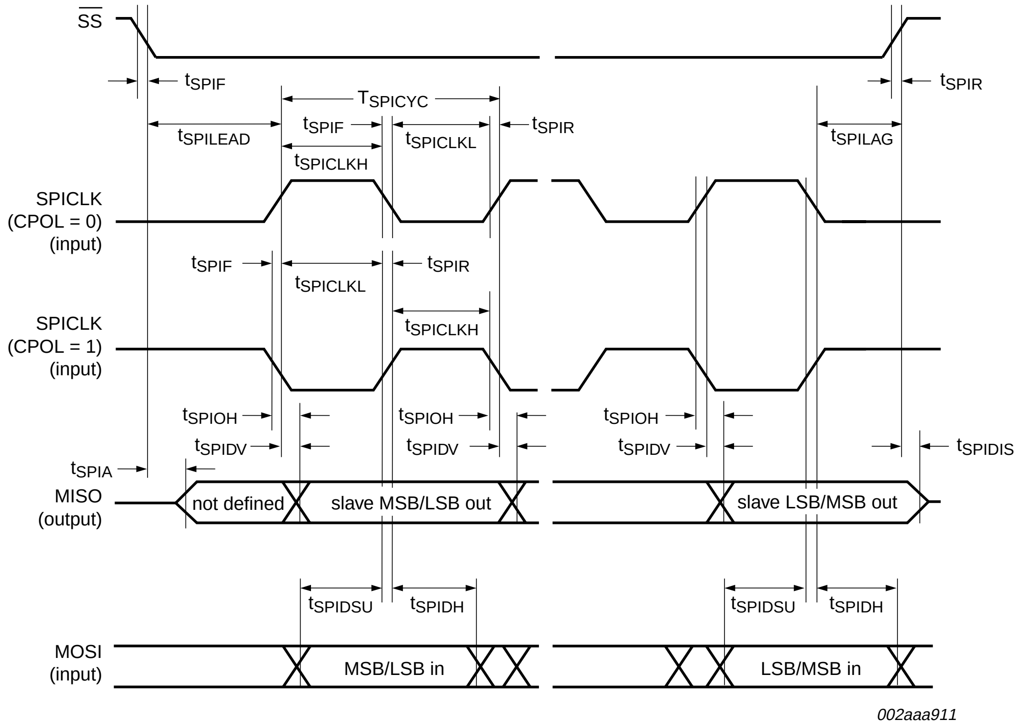
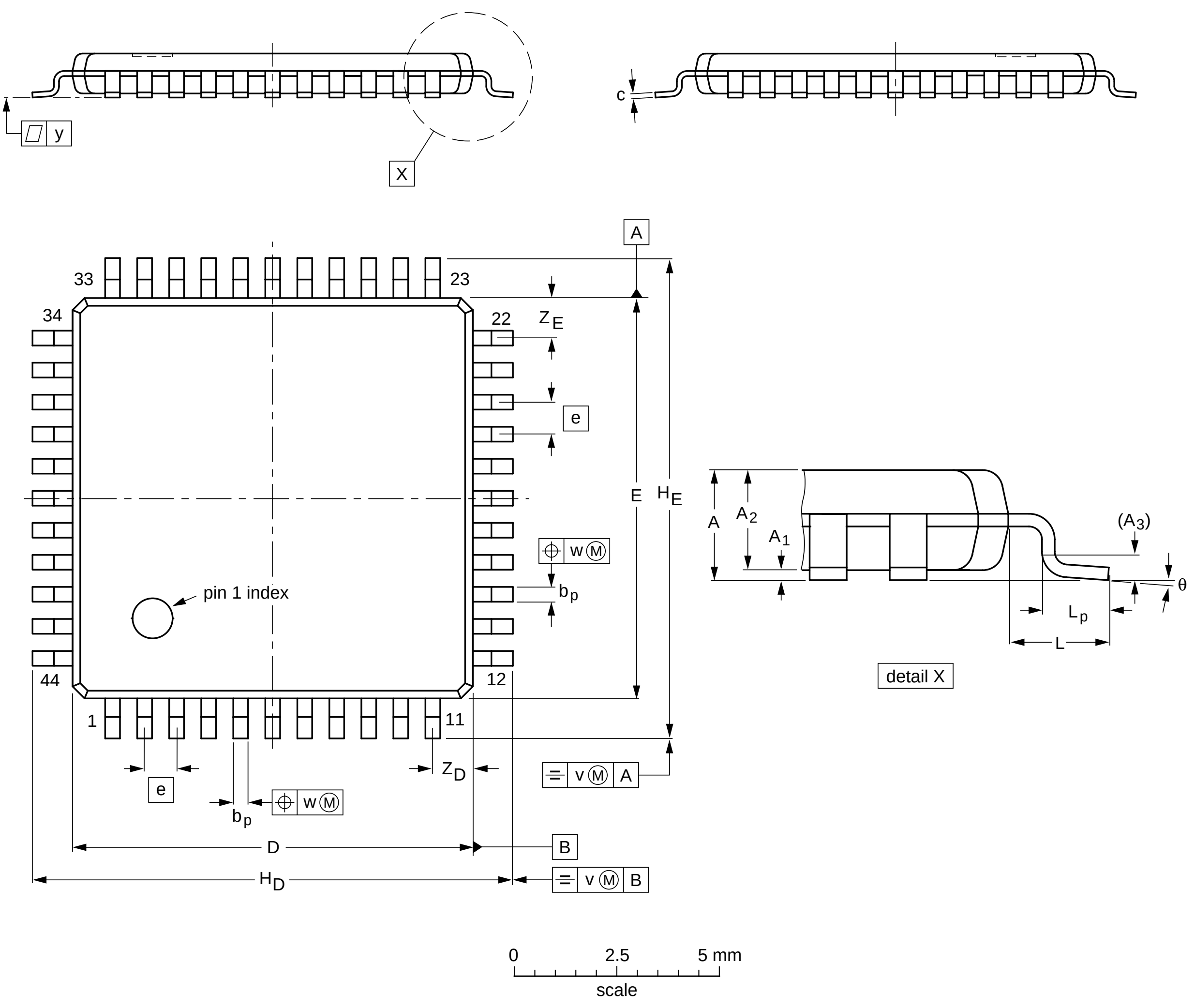


Fig 39. SPI slave timing (CPHA = 1)

TQFP44: plastic thin quad flat package; 44 leads; body 10 x 10 x 1.0 mm SOT376-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.45 0.30	0.18 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT376-1	137E08	MS-026				~~00-01-19~~ 02-03-14

Fig 45. SOT376-1 (TQFP44) package outline