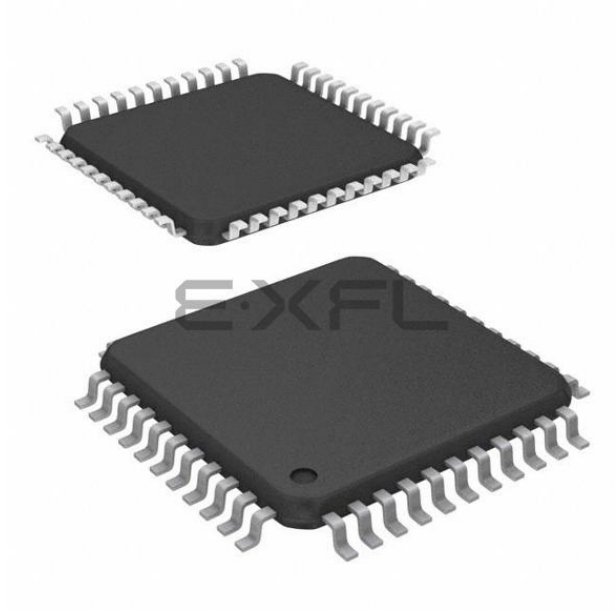

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89v51rc2fbc-557

Table 3. P89V51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
P2.5/A13	26	23	29	I/O	**P2.5 —** Port 2 bit 5.
				O	**A13 —** Address bit 13.
P2.6/A14	27	24	30	I/O	**P2.6 —** Port 2 bit 6.
				O	**A14 —** Address bit 14.
P2.7/A15	28	25	31	I/O	**P2.7 —** Port 2 bit 7.
				O	**A15 —** Address bit 15.
P3.0 to P3.7				I/O with internal pull-up	**Port 3**: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins are pulled HIGH by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 3 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P3.0/RXD	10	5	11	I	**P3.0 —** Port 3 bit 0.
				I	**RXD —** Serial input port.
P3.1/TXD	11	7	13	O	**P3.1 —** Port 3 bit 1.
				O	**TXD —** Serial output port.
P3.2/$\overline{\text{INT0}}$	12	8	14	I	**P3.2 —** Port 3 bit 2.
				I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
P3.3/$\overline{\text{INT1}}$	13	9	15	I	**P3.3 —** Port 3 bit 3.
				I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P3.4/T0	14	10	16	I/O	**P3.4 —** Port 3 bit 4.
				I	**T0 —** External count input to Timer/counter 0.
P3.5/T1	15	11	17	I/O	**P3.5 —** Port 3 bit 5.
				I	**T1 —** External count input to Timer/counter 1.
P3.6/$\overline{\text{WR}}$	16	12	18	O	**P3.6 —** Port 3 bit 6.
				O	**$\overline{\text{WR}}$ —** External data memory write strobe.
P3.7/$\overline{\text{RD}}$	17	13	19	O	**P3.7 —** Port 3 bit 7.
				O	**$\overline{\text{RD}}$ —** External data memory read strobe.
$\overline{\text{PSEN}}$	29	26	32	I/O	**Program Store Enable**: $\overline{\text{PSEN}}$ is the read strobe for external program memory. When the device is executing from internal program memory, $\overline{\text{PSEN}}$ is inactive (HIGH). When the device is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. A forced HIGH-to-LOW input transition on the $\overline{\text{PSEN}}$ pin while the RST input is continually held HIGH for more than 10 machine cycles will cause the device to enter external host mode programming.

Table 4. Special function registers *…continued*

** indicates SFRs that are bit addressable*

Name	Description	SFR address	Bit functions and addresses							
			MSB							LSB
SADDR	Serial Port Address Register	A9H								
SADEN	Serial Port Address Enable	B9H								
		Bit address	**87**[1]	**86**[1]	**85**[1]	**84**[1]	**83**[1]	**82**[1]	**81**[1]	**80**[1]
SPCTL	SPI Control Register	D5H	SPIE	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
SPCFG	SPI Configuration Register	AAH	SPIF	SPWCOL	-	-	-	-	-	-
SPDAT	SPI Data	86H								
SP	Stack Pointer	81H								
		Bit address	**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**
TCON*	Timer Control Register	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
		Bit address	**CF**	**CE**	**CD**	**CC**	**CB**	**CA**	**C9**	**C8**
T2CON*	Timer2 Control Register	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
T2MOD	Timer2 Mode Control	C9H	-	-	ENT2				T2OE	DCEN
TH0	Timer 0 HIGH	8CH								
TH1	Timer 1 HIGH	8DH								
TH2	Timer 2 HIGH	CDH								
TL0	Timer 0 LOW	8AH								
TL1	Timer 1 LOW	8BH								
TL2	Timer 2 LOW	CCH								
TMOD	Timer 0 and 1 Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0
WDTC	Watchdog Timer Control	C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT
WDTD	Watchdog Timer Data/Reload	85H								

[1] Unimplemented bits in SFRs (labeled '-') are 'X's (unknown) at all times. Unless otherwise specified, '1's should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

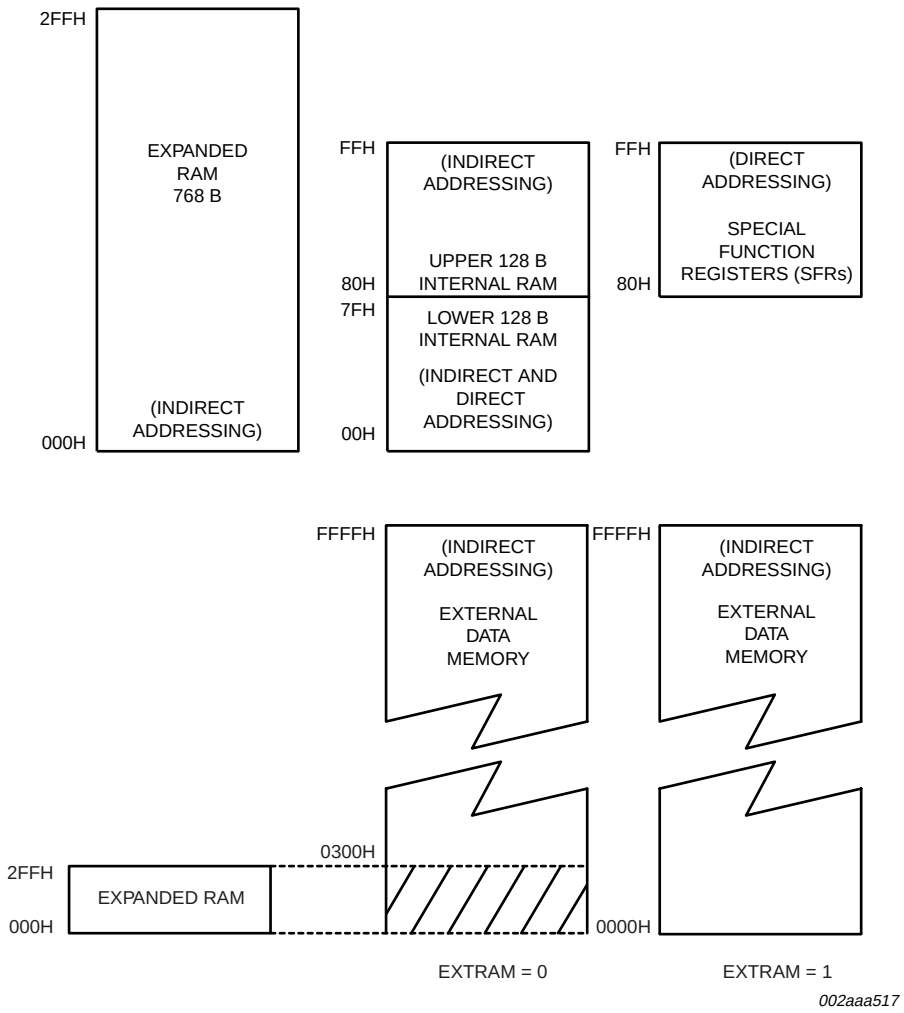


Fig 6. Internal and external data memory structure

6.2.8 Dual data pointers

The device has two 16-bit data pointers. The DPTR Select (DPS) bit in AUXR1 determines which of the two data pointers is accessed. When DPS = 0, DPTR0 is selected; when DPS = 1, DPTR1 is selected. Quickly switching between the two data pointers can be accomplished by a single INC instruction on AUXR1 (see Figure 7).

Table 12. ISP hex record formats *…continued*

Record type	Command/data function
05	Miscellaneous Read Functions :02xxxx05ffsscc Where: 02 = number of bytes in the record xxxx = required field but value is a 'don't care' 05 = function code for misc read ffss = subfunction and selection code 0000 = read manufacturer id 0001 = read device id 1 0002 = read boot code version 0700 = read security bit (00 SoftICE serial number match 0 SB 0 Double Clock) cc = checksum Example: :020000050000F9 (display manufacturer id)
06	Direct Load of Baud Rate :02xxxx06HHLLcc Where: 02 = number of bytes in the record xxxx = required field but value is a 'don't care' HH = high byte of timer LL = low byte of timer cc = checksum Example: :02000006FFFFcc (load T2 = FFFF)
07	Reset serial number, erase user code, clear SoftICE mode :xxxxxx07cc Where: xxxxxx = required field but value is a 'don't care' 07 = reset serial number function cc = checksum Example: :00000007F9
08	Verify serial number :nnxxxx08ss..sscc Where: xxxxxx = required field but value is a 'don't care' 08 = verify serial number function ss..ss = serial number contents cc = checksum Example: :03000008010203EF (verify s/n = 010203)

Table 14. TMOD - Timer/counter mode control register (address 89H) bit allocation

Not bit addressable; Reset value: 0000 0000B; Reset source(s): any source

Bit	7	6	5	4	3	2	1	0
Symbol	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0

Table 15. TMOD - Timer/counter mode control register (address 89H) bit description

Bit	Symbol	Description
	T1/T0	Bits controlling Timer1/Timer0
	GATE	Gating control when set. Timer/counter 'x' is enabled only while 'INTx' pin is HIGH and 'TRx' control pin is set. When cleared, Timer 'x' is enabled whenever 'TRx' control bit is set.
	C/$\overline{T}$	Gating Timer or Counter Selector cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from 'Tx' input pin).

Table 16. TMOD - Timer/counter mode control register (address 89H) M1/M0 operating mode

M1	M0	Operating mode	
0	0	0	8048 timer 'TLx' serves as 5-bit prescaler
0	1	1	16-bit Timer/counter 'THx' and 'TLx' are cascaded; there is no prescaler.
1	0	2	8-bit auto-reload Timer/counter 'THx' holds a value which is to be reloaded into 'TLx' each time it overflows.
1	1	3	(Timer 0) TL0 is an 8-bit Timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/counter 1 stopped.

Table 17. TCON - Timer/counter control register (address 88H) bit allocation

Bit addressable; Reset value: 0000 0000B; Reset source(s): any reset

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 18. TCON - Timer/counter control register (address 88H) bit description

Bit	Symbol	Description
7	TF1	Timer 1 overflow flag. Set by hardware on Timer/counter overflow. Cleared by hardware when the processor vectors to Timer 1 Interrupt routine, or by software.
6	TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/counter 1 on/off.
5	TF0	Timer 0 overflow flag. Set by hardware on Timer/counter overflow. Cleared by hardware when the processor vectors to Timer 0 Interrupt routine, or by software.
4	TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/counter 0 on/off.
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge/low level is detected. Cleared by hardware when the interrupt is processed, or by software.

Table 18. TCON - Timer/counter control register (address 88H) bit description *...continued*

Bit	Symbol	Description
2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level that triggers external interrupt 1.
1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge/low level is detected. Cleared by hardware when the interrupt is processed, or by software.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level that triggers external interrupt 0.

6.4.1 Mode 0

Putting either Timer into mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a fixed divide-by-32 prescaler. Figure 8 shows mode 0 operation.

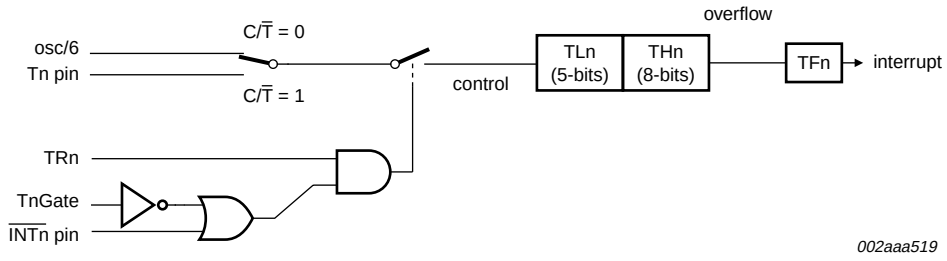


Fig 8. Timer/counter 0 or 1 in mode 0 (13-bit counter)

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The count input is enabled to the Timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the Special Function Register TCON (Figure 7). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 and Timer 1 (see Figure 8). There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

6.4.2 Mode 1

Mode 1 is the same as mode 0, except that all 16 bits of the timer register (THn and TLn) are used. See Figure 9.

Table 21. T2CON - Timer/counter 2 control register (address C8H) bit description *...continued*

Bit	Symbol	Description
4	TCLK	Transmit clock flag. When set, causes the UART to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
3	EXEN2	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	Start/stop control for Timer 2. A logic '1' enables the timer to run.
1	C/$\overline{T}$2	Timer or counter select. (Timer 2) 0 = internal timer (f_{osc} / 6) 1 = external event counter (falling edge triggered; external clock's maximum rate = f_{osc} / 12
0	CP/$\overline{RL}$2	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 22. T2MOD - Timer 2 mode control register (address C9H) bit allocation

Not bit addressable; Reset value: XX00 0000B

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T2OE	DCEN

Table 23. T2MOD - Timer 2 mode control register (address C9H) bit description

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to '0' by user programs.
1	T2OE	Timer 2 Output Enable bit. Used in programmable clock-out mode only.
0	DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

6.5.1 Capture mode

In the Capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0 Timer 2 is a 16-bit timer or counter (as selected by C/$\overline{T}$2 in T2CON) which upon overflowing sets bit TF2, the Timer 2 overflow bit.

The capture mode is illustrated in Figure 12.

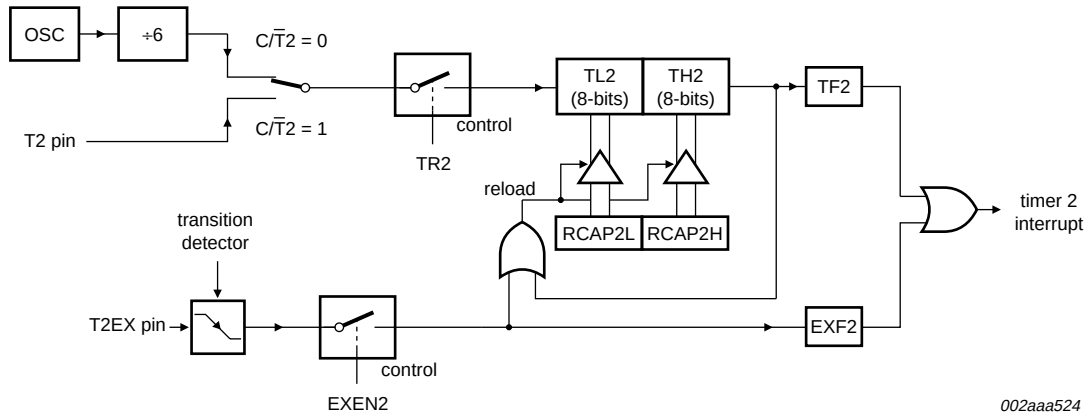


Fig 13. Timer 2 in auto-reload mode (DCEN = 0)

In this mode, there are two options selected by bit EXEN2 in T2CON register. If EXEN2 = 0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

Auto reload frequency when Timer 2 is counting up can be determined from this formula:

$$\frac{SupplyFrequency}{(65536 \angle (RCAP2H, RCAP2L))} \quad (1)$$

Where SupplyFrequency is either f_{osc} (C/$\overline{T2}$ = 0) or frequency of signal on T2 pin (C/$\overline{T2}$ = 1).

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 is ‘1’.

Microcontroller’s hardware will need three consecutive machine cycles in order to recognize falling edge on T2EX and set EXF2 = 1: in the first machine cycle pin T2EX has to be sampled as ‘1’; in the second machine cycle it has to be sampled as ‘0’, and in the third machine cycle EXF2 will be set to ‘1’.

In Figure 14, DCEN = 1 and Timer 2 is enabled to count up or down. This mode allows pin T2EX to control the direction of count. When a logic ‘1’ is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

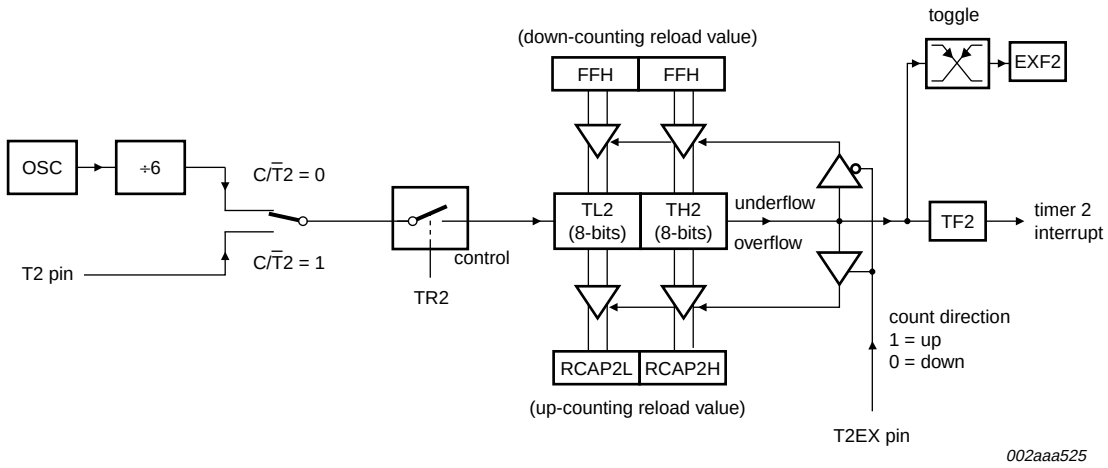


Fig 14. Timer 2 in Auto Reload mode (DCEN = 1)

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2. The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed.

6.5.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1.0). This pin, besides being a regular I/O pin, has two additional functions. It can be programmed:

1. To input the external clock for Timer/counter 2, or
2. To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the Timer/counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{OscillatorFrequency}{2\times(65536\angle(RCAP2H,RCAP2L))} \quad (2)$$

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator.

6.5.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART) transmit and receive baud rates to be derived from either Timer 1 or Timer 2 (See Section 6.6 “UARTs” on page 37 for details). When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When

Table 26. SCON - Serial port control register (address 98H) bit description *...continued*

Bit	Symbol	Description
2	RB8	In modes 2 and 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is undefined.
1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the stop bit in the other modes, in any serial transmission. Must be cleared by software.
0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or approximately halfway through the stop bit time in all other modes. (See SM2 for exceptions). Must be cleared by software.

Table 27. SCON - Serial port control register (address 98H) SM0/SM1 mode definition

SM0, SM1	UART mode	Baud rate
0 0	0: shift register	CPU clock / 6
0 1	1: 8-bit UART	variable
1 0	2: 9-bit UART	CPU clock / 32 or CPU clock / 16
1 1	3: 9-bit UART	variable

6.6.5 Framing error

Framing error (FE) is reported in the SCON.7 bit if SMOD0 (PCON.6) = 1. If SMOD0 = 0, SCON.7 is the SM0 bit for the UART, it is recommended that SM0 is set up before SMOD0 is set to '1'.

6.6.6 More about UART mode 1

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset to align its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: (a) RI = 0, and (b) either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated.

6.6.7 More about UART modes 2 and 3

Reception is performed in the same manner as in mode 1.

Table 29. SPCR - SPI control register (address D5H) bit description *...continued*

Bit	Symbol	Description
2	CPHA	Clock Phase control bit. 1 = shift triggered on the trailing edge of the clock; 0 = shift triggered on the leading edge of the clock.
1	SPR1	SPI Clock Rate Select bit 1. Along with SPR0 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave. See Table 30 below.
0	SPR0	SPI Clock Rate Select bit 0. Along with SPR1 controls the SPICLK rate of the device when a master. SPR1 and SPR0 have no effect on the slave. See Table 30 below.

Table 30. SPCR - SPI control register (address D5H) clock rate selection

SPR1	SPR0	SPICLK = f_{osc} divided by
0	0	4
0	1	16
1	0	64
1	1	128

Table 31. SPSR - SPI status register (address AAH) bit allocation

Bit addressable; Reset source(s): any reset; Reset value: 0000 0000B

Bit	7	6	5	4	3	2	1	0
Symbol	SPIF	WCOL	-	-	-	-	-	-

Table 32. SPSR - SPI status register (address AAH) bit description

Bit	Symbol	Description
7	SPIF	SPI interrupt flag. Upon completion of data transfer, this bit is set to '1'. If SPIE = 1 and ES = 1, an interrupt is then generated. This bit is cleared by software.
6	WCOL	Write Collision Flag. Set if the SPI data register is written to during data transfer. This bit is cleared by software.
5 to 0	-	Reserved for future use. Should be set to '0' by user programs.

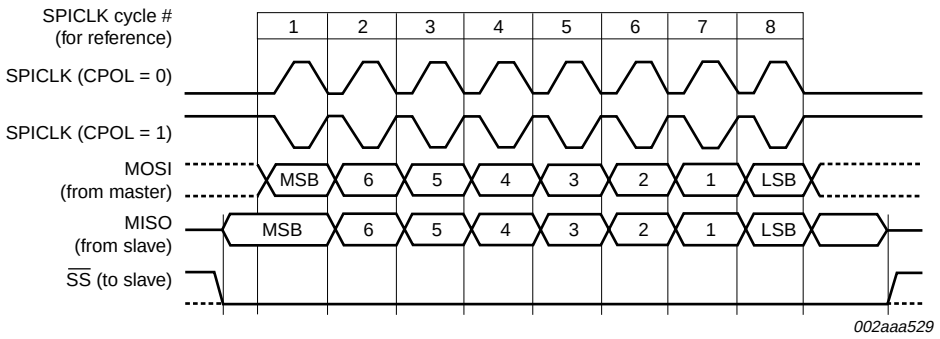


Fig 18. SPI transfer format with CPHA = 0

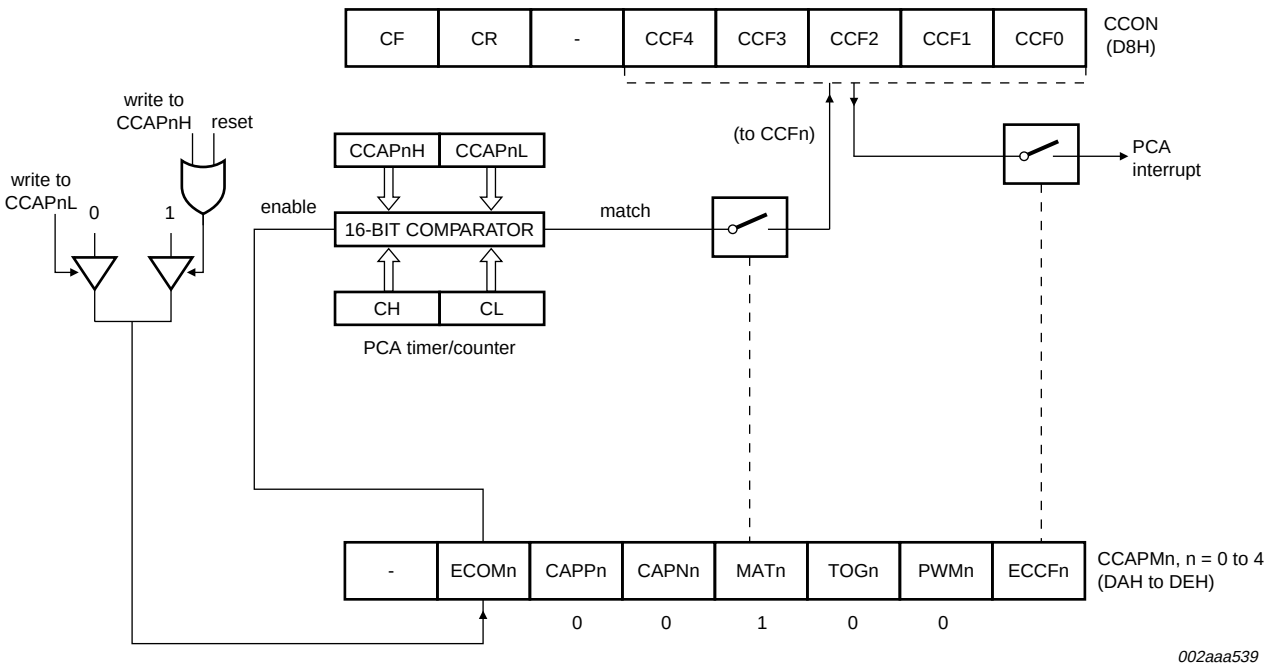


Fig 24. PCA compare mode

6.9.3 High-speed output mode

In this mode (Figure 25) the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set.

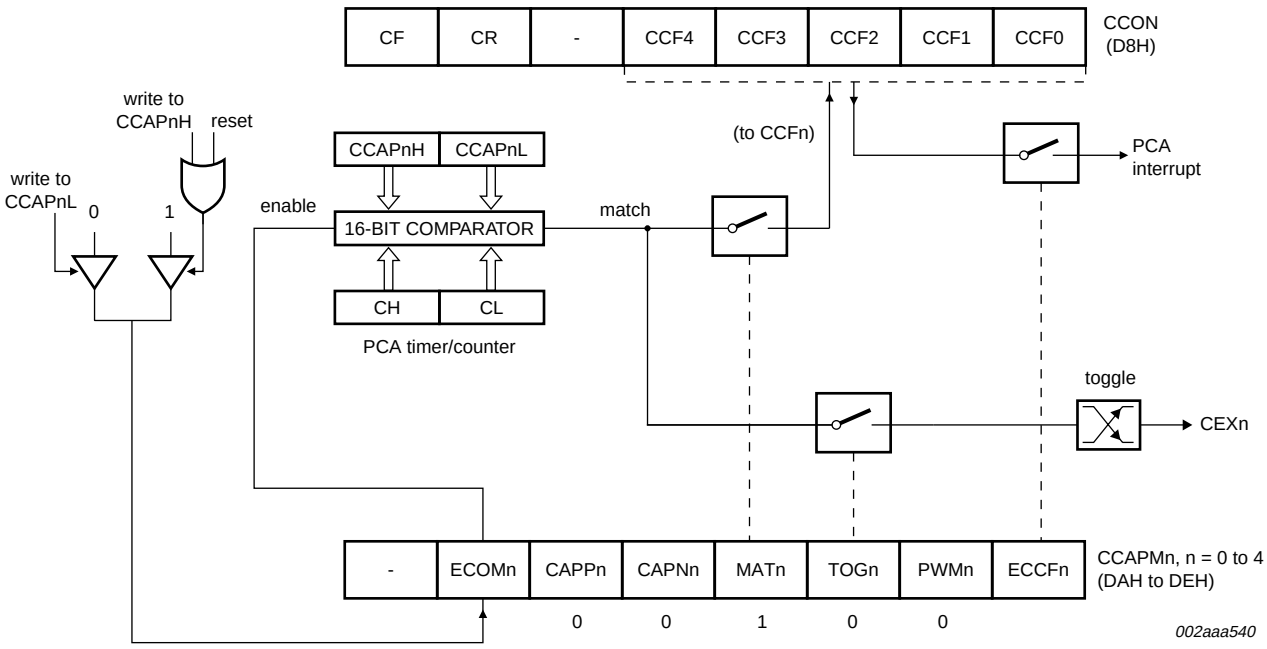


Fig 25. PCA high-speed output mode

6.9.4 PWM mode

All of the PCA modules can be used as PWM outputs (Figure 26). Output frequency depends on the source for the PCA timer.

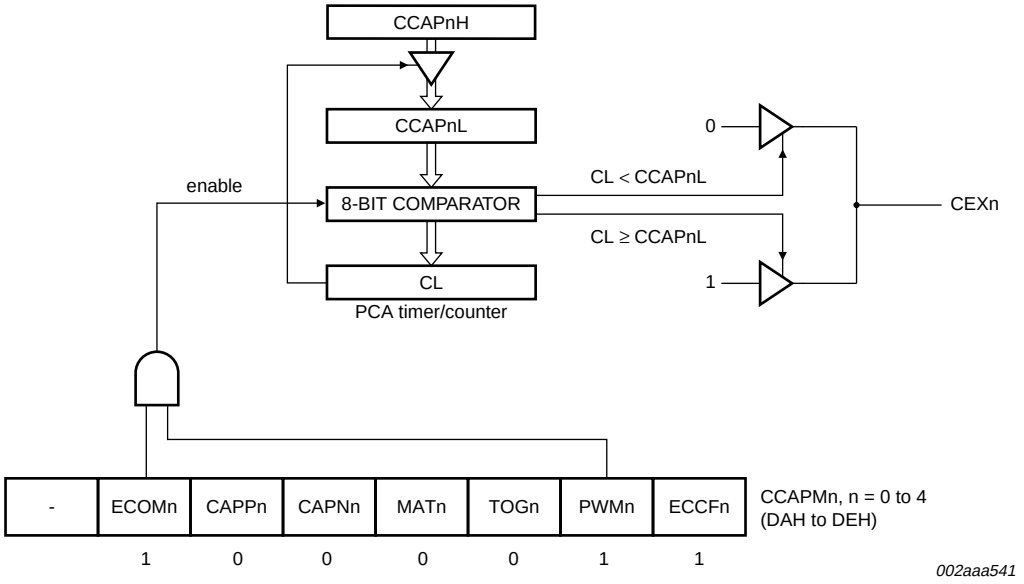


Fig 26. PCA PWM mode

All of the modules will have the same frequency of output because they all share one and only PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPnL. When the value of the PCA CL SFR is less than the

Table 62. Static characteristics *...continued*

T_a = 0 °C to +70 °C or −40 °C to +85 °C; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	V_{DD} = 4.5 V; ports 1, 2, 3, ALE, $\overline{PSEN}$	[5]				
		I_{OH} = −10 µA		V_{DD} − 0.3	-	-	V
		I_{OH} = −30 µA		V_{DD} − 0.7	-	-	V
		I_{OH} = −60 µA		V_{DD} − 1.5	-	-	V
		V_{DD} = 4.5 V; port 0 in External Bus mode					
		I_{OH} = −200 µA		V_{DD} − 0.3	-	-	V
		I_{OH} = −3.2 mA		V_{DD} − 0.7	-	-	V
V_{bo}	brownout trip voltage			3.85	-	4.15	V
I_{IL}	LOW-level input current	V_I = 0.4 V; ports 1, 2, 3		-	-	−75	µA
I_{THL}	HIGH-LOW transition current	V_I = 2 V; ports 1, 2, 3	[6]	-	-	−650	µA
I_{LI}	input leakage current	0.45 V < V_I < V_{DD} − 0.3 V; port 0		-	-	±10	µA
R_{pd}	pull-down resistance	on pin RST		40	-	225	kΩ
C_{iss}	input capacitance	1 MHz; T_a = 25 °C; V_I = 0 V	[7]	-	-	15	pF
$I_{DD(oper)}$	operating supply current	f_{osc} = 12 MHz		-	-	23	mA
		f_{osc} = 40 MHz		-	-	50	mA
$I_{DD(idle)}$	Idle mode supply current	f_{osc} = 12 MHz		-	-	20	mA
		f_{osc} = 40 MHz		-	-	42	mA
$I_{DD(pd)}$	Power-down mode supply current	minimum V_{DD} = 2 V					
		T_a = 0 °C to +70 °C		-	-	80	µA
		T_a = −40 °C to +85 °C		-	-	90	µA

[1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

[2] Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

a) Maximum I_{OL} per 8-bit port: 26 mA

b) Maximum I_{OL} total for all outputs: 71 mA

c) If I_{OL} exceeds the test condition, V_{OH} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[3] Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and Ports 1 and 3. The noise due to external bus capacitance discharging into the Port 0 and 2 pins when the pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

[4] Load capacitance for Port 0, ALE and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

[5] Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{DD} − 0.7 V specification when the address bits are stabilizing.

[6] Pins of Ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_I is approximately 2 V.

[7] Pin capacitance is characterized but not tested. $\overline{EA}$ = 25 pF (max).

9. Dynamic characteristics

Table 63. Dynamic characteristics

Over operating conditions: load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF

T_a = 0 °C to +70 °C or −40 °C to +85 °C; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	X1 mode	0	-	40	MHz
		X2 mode	0	-	20	MHz
		IAP	0.25	-	40	MHz
t_{LHLL}	ALE pulse width		$2T_{cy(clk)} - 15$	-	-	ns
t_{AVLL}	address valid to ALE LOW time		$T_{cy(clk)} - 15$	-	-	ns
t_{LLAX}	address hold after ALE LOW time		$T_{cy(clk)} - 15$	-	-	ns
t_{LLIV}	ALE LOW to valid instruction in time		-	-	$4T_{cy(clk)} - 45$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW time		$T_{cy(clk)} - 15$	-	-	ns
t_{PLPH}	$\overline{PSEN}$ pulse width		$3T_{cy(clk)} - 15$	-	-	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in time		-	-	$3T_{cy(clk)} - 50$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$ time		0	-	-	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$ time		-	-	$T_{cy(clk)} - 15$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid time		$T_{cy(clk)} - 8$	-	-	ns
t_{AVIV}	address to valid instruction in time		-	-	$5T_{cy(clk)} - 60$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float time		-	-	10	ns
t_{RLRH}	$\overline{RD}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	-	ns
t_{WLWH}	$\overline{WR}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	-	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in time		-	-	$5T_{cy(clk)} - 50$	ns
t_{RHDX}	data hold after $\overline{RD}$ time		0	-	-	ns
t_{RHDZ}	data float after $\overline{RD}$ time		-	-	$2T_{cy(clk)} - 12$	ns
t_{LLDV}	ALE LOW to valid data in time		-	-	$8T_{cy(clk)} - 50$	ns
t_{AVDV}	address to valid data in time		-	-	$9T_{cy(clk)} - 75$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW time		$3T_{cy(clk)} - 15$	-	$3T_{cy(clk)} + 15$	ns
t_{AVWL}	address to $\overline{RD}$ or $\overline{WR}$ LOW time		$4T_{cy(clk)} - 30$	-	-	ns
t_{WHQX}	data hold after $\overline{WR}$ time		$T_{cy(clk)} - 20$	-	-	ns
t_{QVWH}	data output valid to $\overline{WR}$ HIGH time		$7T_{cy(clk)} - 50$	-	-	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float time		-	-	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH time		$T_{cy(clk)} - 15$	-	$T_{cy(clk)} + 15$	ns

[1] $T_{cy(clk)} = 1 / f_{osc}$.

[2] Calculated values are for 6-clock mode only.

Table 64. External clock drive

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
f_{osc}	oscillator frequency	-	-	0	40	MHz
$T_{cy(clk)}$	clock cycle time	25	-	-	-	ns
t_{CHCX}	clock HIGH time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCX}	clock LOW time	8.75	-	$0.35T_{cy(clk)}$	$0.65T_{cy(clk)}$	ns
t_{CLCH}	clock rise time	-	10	-	-	ns
t_{CHCL}	clock fall time	-	10	-	-	ns

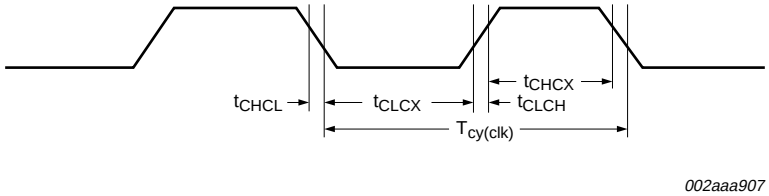


Fig 34. External clock drive waveform (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

Table 65. Serial port timing

Symbol	Parameter	Oscillator				Unit
		40 MHz		Variable		
		Min	Max	Min	Max	
T_{XLXL}	serial port clock cycle time	0.3	-	$12T_{cy(clk)}$	-	µs
t_{QVXH}	output data set-up to clock rising edge time	117	-	$10T_{cy(clk)} - 133$	-	ns
t_{XHQX}	output data hold after clock rising edge time	0	-	$2T_{cy(clk)} - 50$	-	ns
t_{XHDX}	input data hold after clock rising edge time	0	-	0	-	ns
t_{XHDV}	input data valid to clock rising edge time	-	117	-	$10T_{cy(clk)} - 133$	ns

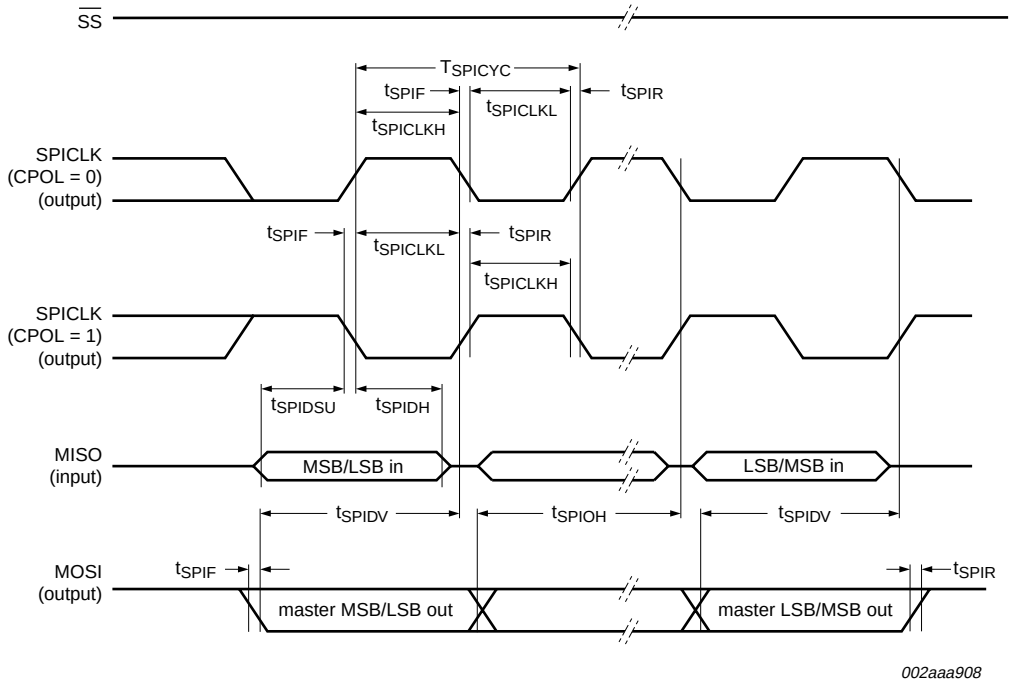


Fig 36. SPI master timing (CPHA = 0)

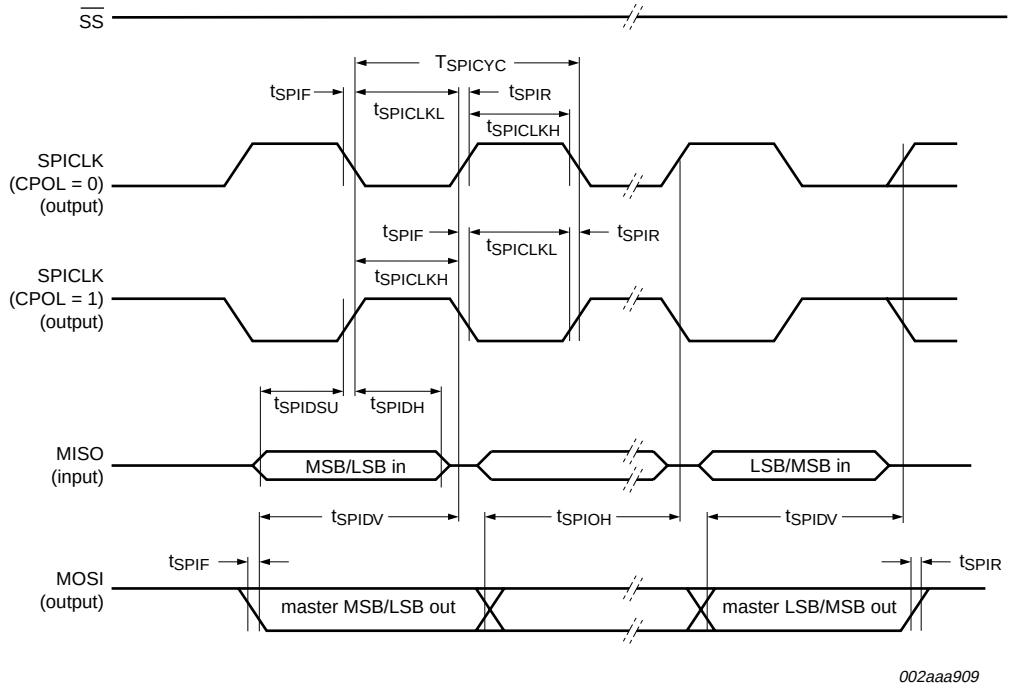


Fig 37. SPI master timing (CPHA = 1)

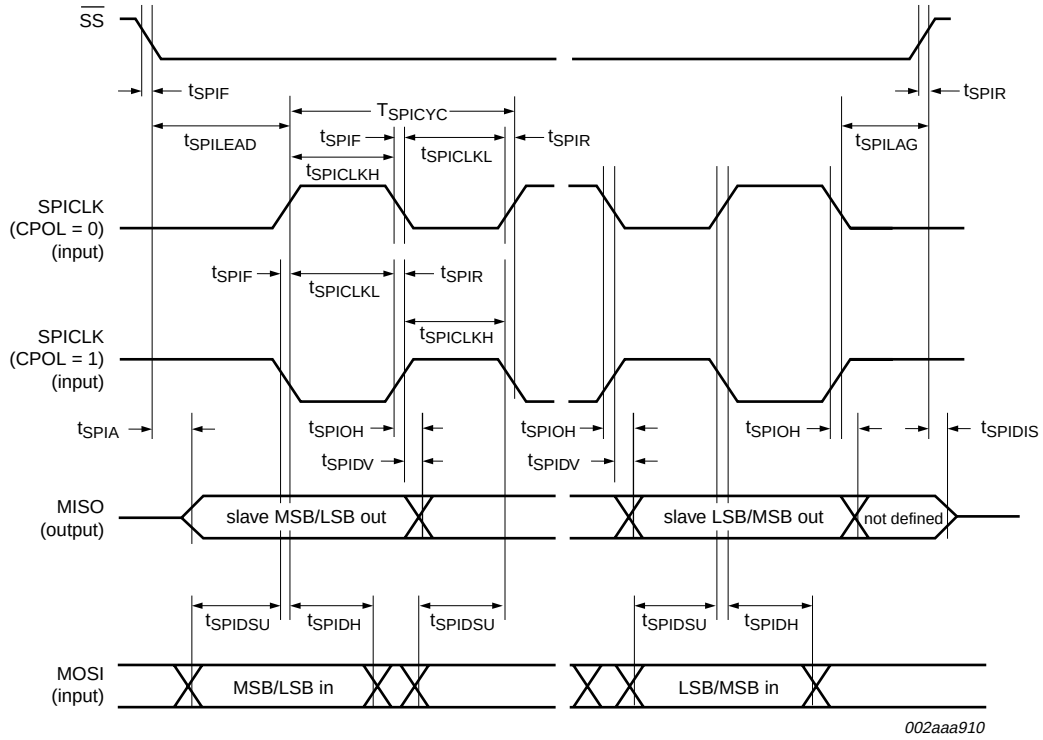


Fig 38. SPI slave timing (CPHA = 0)

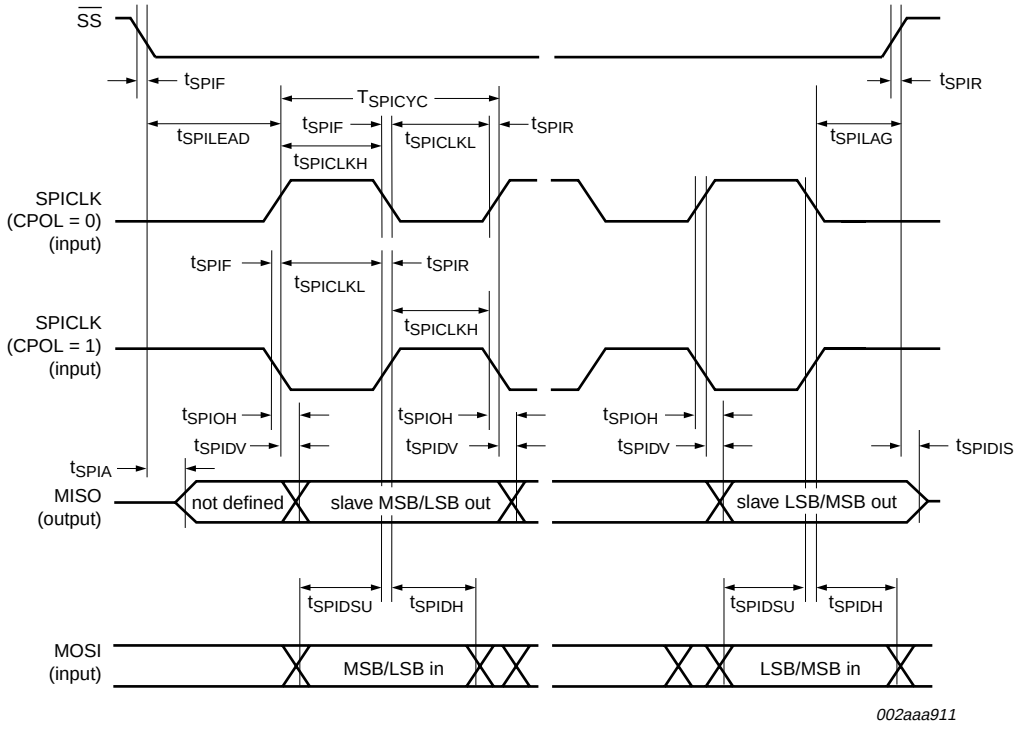
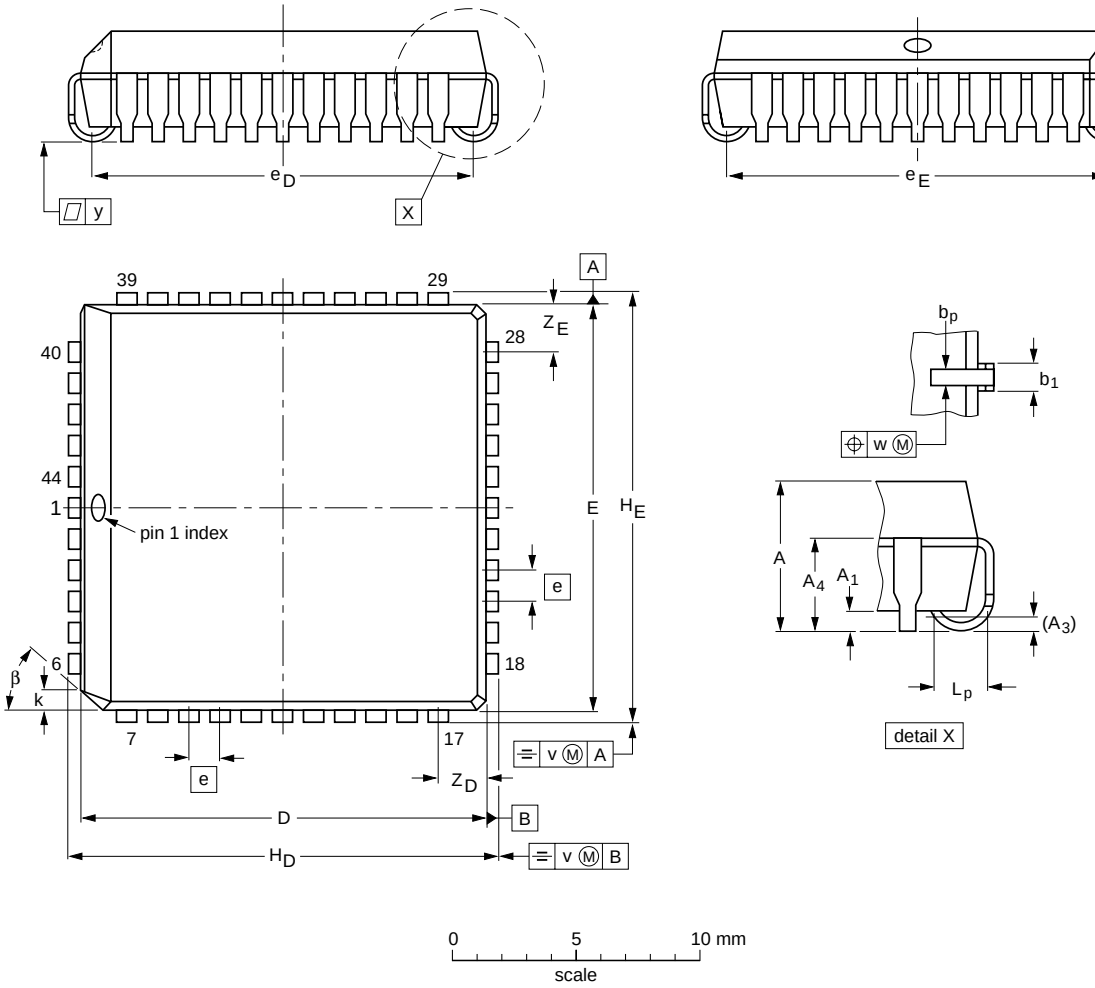


Fig 39. SPI slave timing (CPHA = 1)

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 46. SOT187-2 (PLCC44) package outline

12. Revision history

Table 68. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89V51RB2_RC2_RD2_5	20091112	Product data sheet	-	P89V51RB2_RC2_RD2_4
Modifications:	• Table 37: Changed 2nd row, f_{osc} / 6 to f_{osc} / 2. • Table 62: Changed 12 MHz max values for $I_{DD(oper)}$ and $I_{DD(idle)}$. • Table 3: Removed sentence “However, Security lock level 4 will disable $\overline{EA}$...” from $\overline{EA}$ pin description. • Changed SCK to SPICLK throughout data sheet. • Table 3: Changed SCK to SPICLK and updated pin description.			
P89V51RB2_RC2_RD2_4	20070501	Product data sheet	-	P89V51RB2_RC2_RD2-03
P89V51RB2_RC2_RD2-03	20041202	Product data	-	P89V51RB2_RC2_RD2-02
P89V51RD2-02	20041011	Product data	-	P89V51RD2-01
P89V51RD2-01	20040301	Product data	-	-