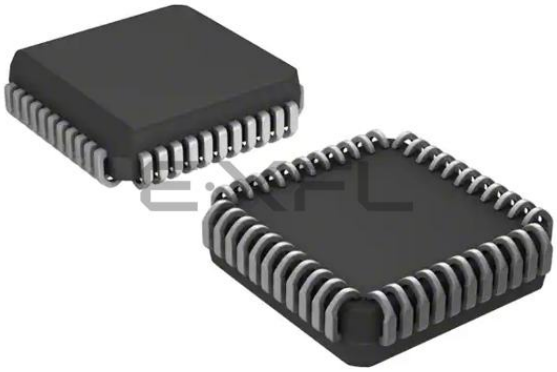

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	40MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89v51rd2fa-512

4. Block diagram

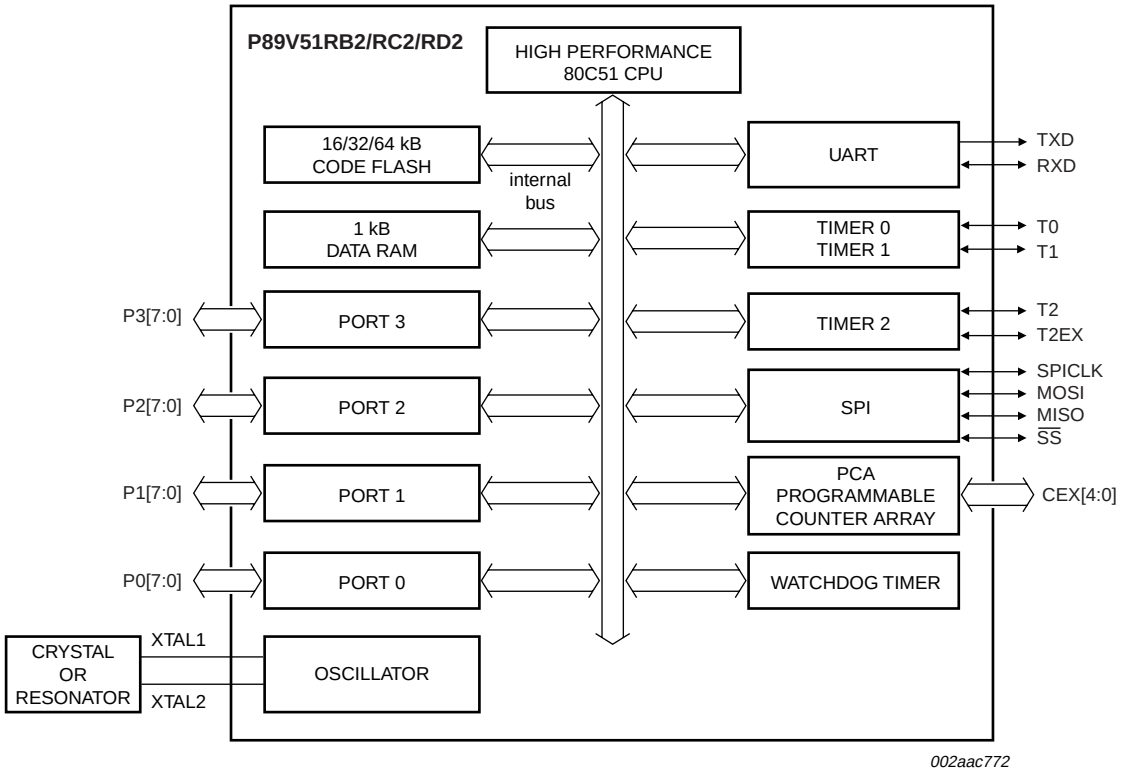


Fig 1. Block diagram

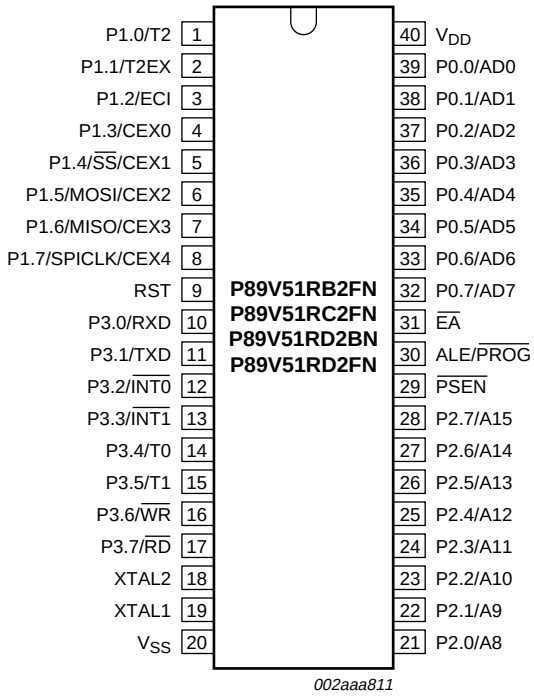


Fig 3. DIP40 pin configuration

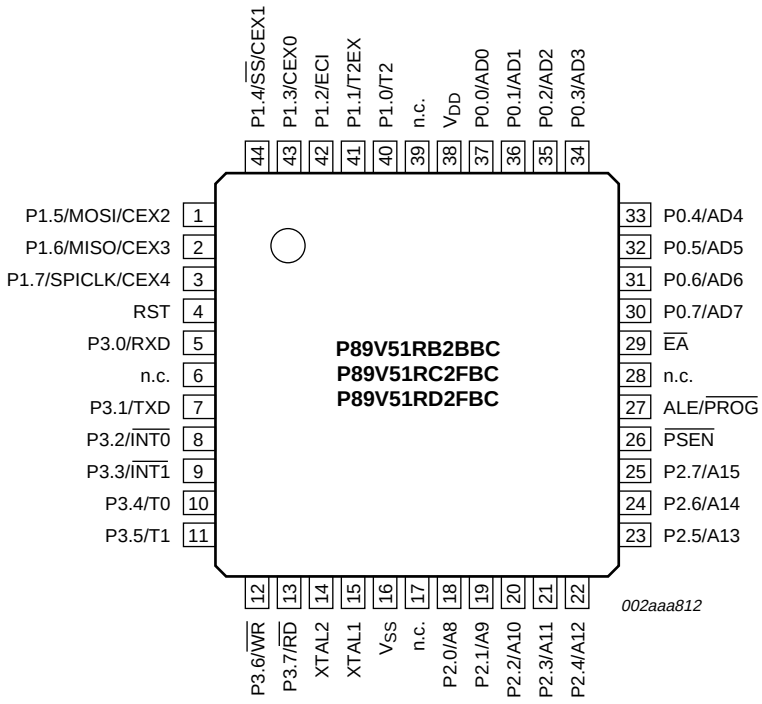


Fig 4. TQFP44 pin configuration

5.2 Pin description

Table 3. P89V51RB2/RC2/RD2 pin description

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
P0.0 to P0.7				I/O	**Port 0:** Port 0 is an 8-bit open drain bidirectional I/O port. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's. Port 0 also receives the code bytes during the external host mode programming, and outputs the code bytes during the external host mode verification. External pull-ups are required during program verification or as a general purpose I/O port.
P0.0/AD0	39	37	43	I/O	**P0.0 —** Port 0 bit 0.
				I/O	**AD0 —** Address/data bit 0.
P0.1/AD1	38	36	42	I/O	**P0.1 —** Port 0 bit 1.
				I/O	**AD1 —** Address/data bit 1.
P0.2/AD2	37	35	41	I/O	**P0.2 —** Port 0 bit 2.
				I/O	**AD2 —** Address/data bit 2.
P0.3/AD3	36	34	40	I/O	**P0.3 —** Port 0 bit 3.
				I/O	**AD3 —** Address/data bit 3.
P0.4/AD4	35	33	39	I/O	**P0.4 —** Port 0 bit 4.
				I/O	**AD4 —** Address/data bit 4.
P0.5/AD5	34	32	38	I/O	**P0.5 —** Port 0 bit 5.
				I/O	**AD5 —** Address/data bit 5.
P0.6/AD6	33	31	37	I/O	**P0.6 —** Port 0 bit 6.
				I/O	**AD6 —** Address/data bit 6.
P0.7/AD7	32	30	36	I/O	**P0.7 —** Port 0 bit 7.
				I/O	**AD7 —** Address/data bit 7.
P1.0 to P1.7				I/O with internal pull-up	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. P1.5, P1.6, P1.7 have high current drive of 16 mA. Port 1 also receives the low-order address bytes during the external host mode programming and verification.
P1.0/T2	1	40	2	I/O	**P1.0 —** Port 1 bit 0.
				I/O	**T2 —** External count input to Timer/counter 2 or Clock-out from Timer/counter 2.
P1.1/T2EX	2	41	3	I/O	**P1.1 —** Port 1 bit 1.
				I	**T2EX**: Timer/counter 2 capture/reload trigger and direction control.

Table 3. P89V51RB2/RC2/RD2 pin description *…continued*

Symbol	Pin			Type	Description
	DIP40	TQFP44	PLCC44		
P1.2/ECI	3	42	4	I/O	**P1.2 —** Port 1 bit 2.
				I	**ECI —** External clock input. This signal is the external clock input for the PCA.
P1.3/CEX0	4	43	5	I/O	**P1.3 —** Port 1 bit 3.
				I/O	**CEX0 —** Capture/compare external I/O for PCA Module 0. Each capture/compare module connects to a Port 1 pin for external I/O. When not used by the PCA, this pin can handle standard I/O.
P1.4/$\overline{SS}$/CEX1	5	44	6	I/O	**P1.4 —** Port 1 bit 4.
				I	**$\overline{SS}$ —** Slave port select input for SPI.
				I/O	**CEX1 —** Capture/compare external I/O for PCA Module 1.
P1.5/MOSI/ CEX2	6	1	7	I/O	**P1.5 —** Port 1 bit 5.
				I/O	**MOSI —** Master Output Slave Input for SPI.
				I/O	**CEX2 —** Capture/compare external I/O for PCA Module 2.
P1.6/MISO/ CEX3	7	2	8	I/O	**P1.6 —** Port 1 bit 6.
				I/O	**MISO —** Master Input Slave Output for SPI.
				I/O	**CEX3 —** Capture/compare external I/O for PCA Module 3.
P1.7/SPICLK/ CEX4	8	3	9	I/O	**P1.7 —** Port 1 bit 7.
				I/O	**SPICLK —** Serial clock input/output for SPI.
				I/O	**CEX4 —** Capture/compare external I/O for PCA Module 4.
P2.0 to P2.7				I/O with internal pull-up	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins are pulled HIGH by the internal pull-ups when ‘1’s are written to them and can be used as inputs in this state. As inputs, Port 2 pins that are externally pulled LOW will source current (I_{IL}) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application, it uses strong internal pull-ups when transitioning to ‘1’s. Port 2 also receives some control signals and a partial of high-order address bits during the external host mode programming and verification.
P2.0/A8	21	18	24	I/O	**P2.0 —** Port 2 bit 0.
				O	**A8 —** Address bit 8.
P2.1/A9	22	19	25	I/O	**P2.1 —** Port 2 bit 1.
				O	**A9 —** Address bit 9.
P2.2/A10	23	20	26	I/O	**P2.2 —** Port 2 bit 2.
				O	**A10 —** Address bit 10.
P2.3/A11	24	21	27	I/O	**P2.3 —** Port 2 bit 3.
				O	**A11 —** Address bit 11.
P2.4/A12	25	22	28	I/O	**P2.4 —** Port 2 bit 4.
				O	**A12 —** Address bit 12.

to work during initial power up, before the voltage reaches the brownout detection level. The POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain active until cleared by software.

Following a power-on or external reset the P89V51RB2/RC2/RD2 will force the SWR and BSEL bits (FCF[1:0]) = 00. This causes the boot block to be mapped into the lower 8 kB of code memory and the device will execute the ISP code in the boot block and attempt to autobaud to the host. If the autobaud is successful the device will remain in ISP mode. If, after approximately 400 ms, the autobaud is unsuccessful the boot block code will check to see if the SoftICE flag is set (from a previous programming operation). If the SoftICE flag is set the device will enter SoftICE mode. If the SoftICE flag is cleared, the boot code will execute a software reset causing the device to execute the user code from block 0 starting at address 0000H. Note that an external reset applied to the RST pin has the same effect as a power-on reset.

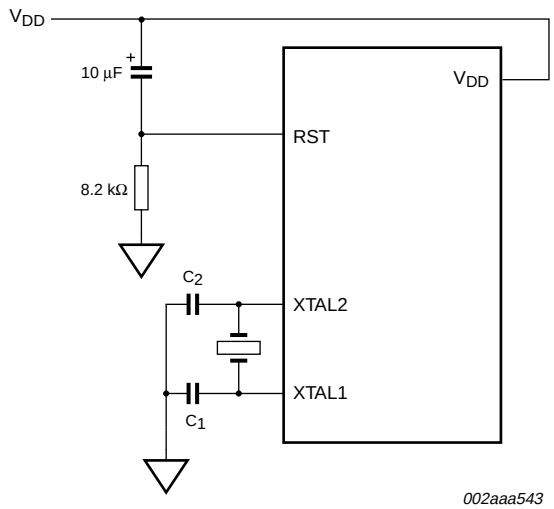


Fig 5. Power-on reset circuit

6.2.3 Software reset

A software reset is executed by changing the SWR bit (FCF.1) from '0' to '1'. A software reset will reset the program counter to address 0000H and force both the SWR and BSEL bits (FCF[1:0]) = 10. This will result in the lower 8 kB of the user code memory being mapped into the user code memory space. Thus the user's code will be executed starting at address 0000H. A software reset will not change WDTC.2 or RAM data. Other SFRs will be set to their reset values.

6.2.4 Brownout detect reset

The device includes a brownout detection circuit to protect the system from severe supply voltage fluctuations. The P89V51RB2/RC2/RD2's brownout detection threshold is 2.35 V. When V_{DD} drops below this voltage threshold, the brownout detect triggers the circuit to generate a brownout interrupt but the CPU still runs until the supplied voltage returns to the brownout detection voltage V_{BOD}. The default operation for a brownout detection is to cause a processor reset.

V_{DD} must stay below V_{BOD} at least four oscillator clock periods before the brownout detection circuit will respond.

Brownout interrupt can be enabled by setting the EBO bit (IEA.3). If EBO bit is set and a brownout condition occurs, a brownout interrupt will be generated to execute the program at location 004BH. It is required that the EBO bit be cleared by software after the brownout interrupt is serviced. Clearing EBO bit when the brownout condition is active will properly reset the device. If brownout interrupt is not enabled, a brownout condition will reset the program to resume execution at location 0000H. A brownout detect reset will clear the BSEL bit (FCF.0) but will not change the SWR bit (FCF.1) and therefore will not change the banking of the lower 8 kB of user code memory space.

6.2.5 Watchdog reset

Like a brownout detect reset, the watchdog timer reset will clear the BSEL bit (FCF.0) but will not change the SWR bit (FCF.1) and therefore will not change the banking of the lower 8 kB of user code memory space.

The state of the SWR and BSEL bits after different types of resets is shown in Table 6. This results in the code memory bank selections as shown.

Table 6. Effects of reset sources on bank selection

Reset source	SWR bit result (FCF.1)	BSEL bit result (FCF.0)	Addresses from 0000H to 1FFFH	Addresses above 1FFFH
External reset	0	0	Boot code (in block 1)	User code (in block 0)
Power-on reset				
Watchdog reset	x	0	Retains state of SWR bit. If SWR, BSEL = 00 then uses boot code. If SWR, BSEL = 10 then uses user code.	
Brownout detect reset				
Software reset	1	0	User code (in block 0)	

6.2.6 Data RAM memory

The data RAM has 1024 B of internal memory. The device can also address up to 64 kB for external data memory.

6.2.7 Expanded data RAM addressing

The P89V51RB2/RC2/RD2 has 1 kB of RAM. See Figure 6 “Internal and external data memory structure” on page 19.

The device has four sections of internal data memory:

1. The lower 128 B of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 B of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 768 B (00H to 2FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit (see ‘Auxiliary function Register’ (AUXR) in Table 4 “Special function registers” on page 11).

Since the upper 128 B occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.

Table 7. AUXR - Auxiliary register (address 8EH) bit allocation

Not bit addressable; Reset value 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	EXTRAM	AO

Table 8. AUXR - Auxiliary register (address 8EH) bit description

Bit	Symbol	Description
7 to 2	-	Reserved for future use. Should be set to '0' by user programs.
1	EXTRAM	Internal/External RAM access using MOVX @Ri/@DPTR. When '0', core attempts to access internal XRAM with address specified in MOVX instruction. If address supplied with this instruction exceeds on-chip available XRAM, off-chip XRAM is going to be selected and accessed. When '1', every MOVX @Ri/@DPTR instruction targets external data memory by default.
0	AO	ALE off: disables/enables ALE. AO = 0 results in ALE emitted at a constant rate of ½ the oscillator frequency. In case of AO = 1, ALE is active only during a MOVX or MOVC.

When instructions access addresses in the upper 128 B (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed. See the examples below.

Indirect Access:

MOV@R0, #data; R0 contains 90H

Register R0 points to 90H which is located in the upper address range. Data in '#data' is written to RAM location 90H rather than port 1.

Direct Access:

MOV90H, #data; write data to P1

Data in '#data' is written to port 1. Instructions that write directly to the address write to the SFRs.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 768 B of memory is physically located on the chip and logically occupies the first 768 B of external memory (addresses 000H to 2FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 ($\overline{WR}$), P3.7 ($\overline{RD}$), or P2. With EXTRAM = 0, the expanded RAM can be accessed as in the following example.

Expanded RAM Access (Indirect Addressing only):

MOVX@DPTR, A DPTR contains 0A0H

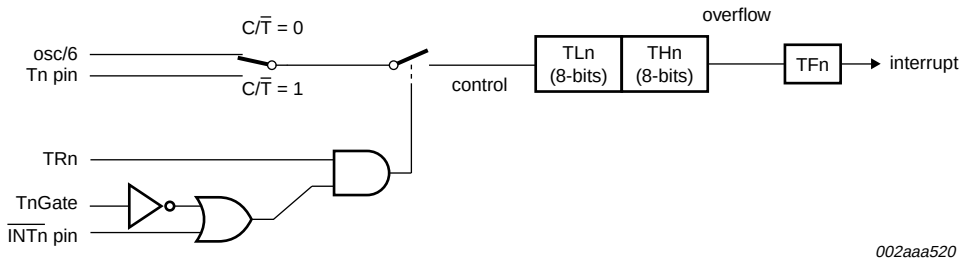


Fig 9. Timer/counter 0 or 1 in mode 1 (16-bit counter)

6.4.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TLn) with automatic reload, as shown in Figure 10. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

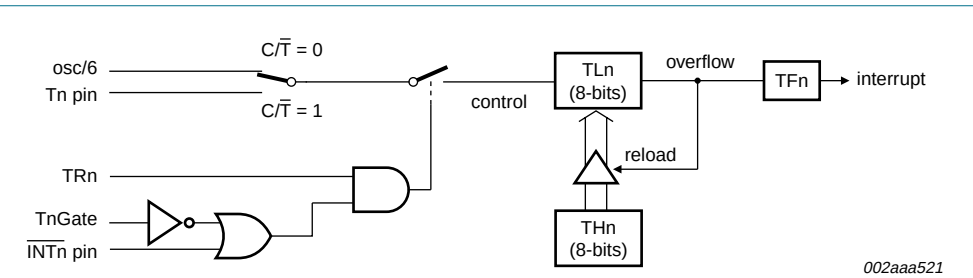


Fig 10. Timer/counter 0 or 1 in mode 2 (8-bit auto-reload)

6.4.4 Mode 3

When timer 1 is in mode 3 it is stopped (holds its count). The effect is the same as setting TR1 = 0.

Timer 0 in mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for mode 3 and Timer 0 is shown in Figure 11. TL0 uses the Timer 0 control bits: T0C/$\overline{T}$, T0GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the 'Timer 1' interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in mode 3, the P89V51RB2/RC2/RD2 can look like it has an additional Timer.

Note: When Timer 0 is in mode 3, Timer 1 can be turned on and off by switching it into and out of its own mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

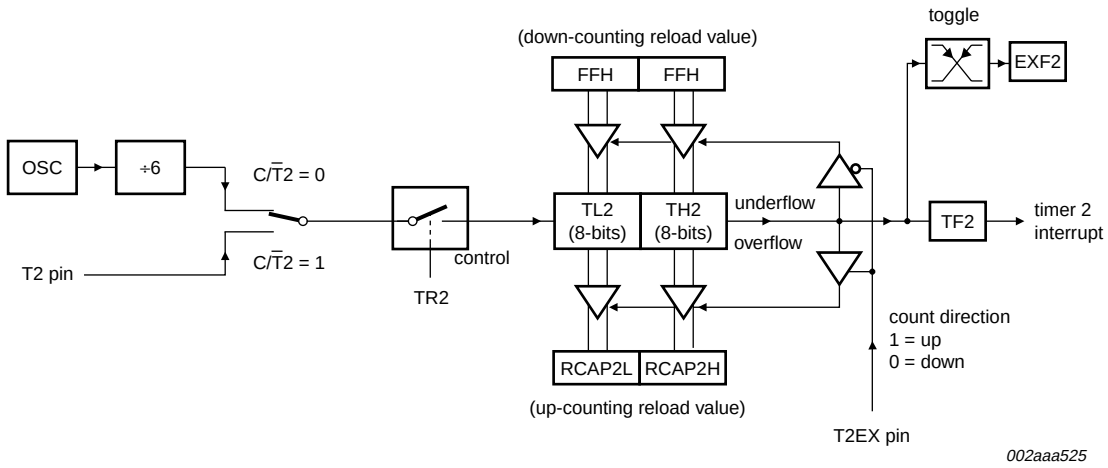


Fig 14. Timer 2 in Auto Reload mode (DCEN = 1)

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2. The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed.

6.5.3 Programmable clock-out

A 50 % duty cycle clock can be programmed to come out on pin T2 (P1.0). This pin, besides being a regular I/O pin, has two additional functions. It can be programmed:

1. To input the external clock for Timer/counter 2, or
2. To output a 50 % duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency.

To configure the Timer/counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in Equation 2:

$$\frac{OscillatorFrequency}{2\times(65536\angle(RCAP2H,RCAP2L))} \quad (2)$$

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator.

6.5.4 Baud rate generator mode

Bits TCLK and/or RCLK in T2CON allow the UART) transmit and receive baud rates to be derived from either Timer 1 or Timer 2 (See Section 6.6 “UARTs” on page 37 for details). When TCLK = 0, Timer 1 is used as the UART transmit baud rate generator. When

clock output and input for the master and slave modes, respectively. The SPI clock generator will start following a write to the master devices SPI data register. The written data is then shifted out of the MOSI pin on the master device into the MOSI pin of the slave device. Following a complete transmission of one byte of data, the SPI clock generator is stopped and the SPIF flag is set. An SPI interrupt request will be generated if the SPI Interrupt Enable bit (SPIE) and the Serial Port Interrupt Enable bit (ES) are both set.

An external master drives the Slave Select input pin, $\overline{SS}$/P1[4], low to select the SPI module as a slave. If $\overline{SS}$/P1[4] has not been driven low, then the slave SPI unit is not active and the MOSI/P1[5] port can also be used as an input port pin.

CPHA and CPOL control the phase and polarity of the SPI clock. Figure 18 and Figure 19 show the four possible combinations of these two bits.

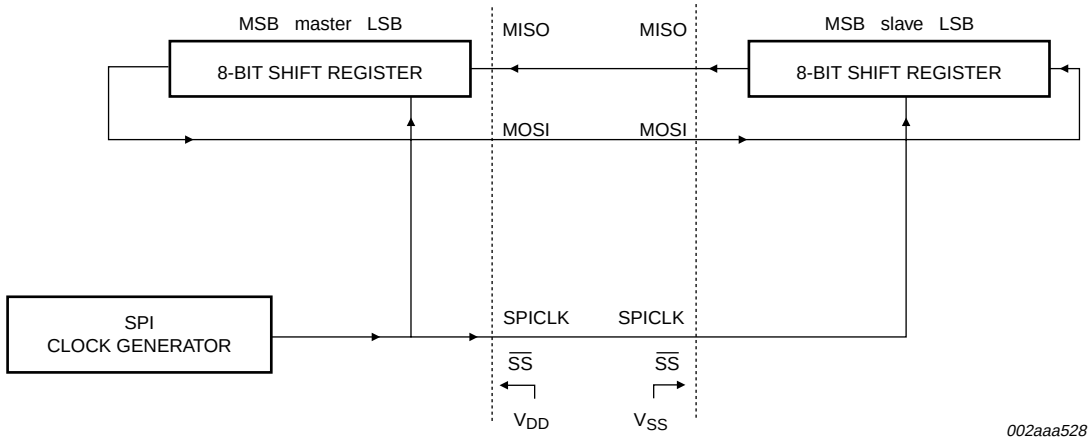


Fig 17. SPI master-slave interconnection

Table 28. SPCR - SPI control register (address D5H) bit allocation

Bit addressable; Reset source(s): any reset; Reset value: 0000 0000B

Bit	7	6	5	4	3	2	1	0
Symbol	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0

Table 29. SPCR - SPI control register (address D5H) bit description

Bit	Symbol	Description
7	SPIE	If both SPIE and ES are set to one, SPI interrupts are enabled.
6	SPE	SPI enable bit. When set enables SPI.
5	DORD	Data transmission order. 0 = MSB first; 1 = LSB first in data transmission.
4	MSTR	Master/slave select. 1 = master mode, 0 = slave mode.
3	CPOL	Clock polarity. 1 = SPICLK is high when idle (active LOW), 0 = SPICLK is low when idle (active HIGH).

Table 33. WDTC - Watchdog control register (address COH) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT

Table 34. WDTC - Watchdog control register (address COH) bit description

Bit	Symbol	Description
7 to 5	-	Reserved for future use. Should be set to '0' by user programs.
4	WDOUT	Watchdog output enable. When this bit and WDRE are both set, a Watchdog reset will drive the reset pin active for 32 clocks.
3	WDRE	Watchdog timer reset enable. When set enables a watchdog timer reset.
2	WDTS	Watchdog timer reset flag, when set indicates that a WDT reset occurred. Reset in software.
1	WDT	Watchdog timer refresh. Set by software to force a WDT reset.
0	SWDT	Start watchdog timer, when set starts the WDT. When cleared, stops the WDT.

6.9 PCA

The PCA includes a special 16-bit Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or PWM. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3 (CEX0), module 1 to P1.4 (CEX1), etc. Registers CH and CL contain current value of the free running up counting 16-bit PCA timer. The PCA timer is a common time base for all five modules and can be programmed to run at: $^1/_6$ the oscillator frequency, $^1/_2$ the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR (see Table 35 and Table 36).

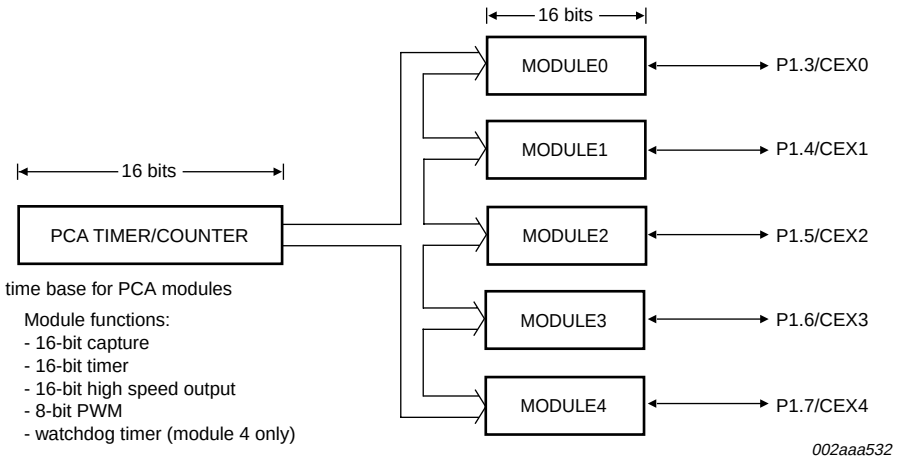


Fig 21. PCA

Table 37. CMOD - PCA counter mode register (address D9H) count pulse select

CPS1	CPS0	Select PCA input
0	0	0 Internal clock, f_{osc} / 6
0	1	1 Internal clock, f_{osc} / 2
1	0	2 Timer 0 overflow
1	1	3 External clock at ECI/P1.2 pin (max rate = f_{osc} / 4)

Table 38. CCON - PCA counter control register (address 0D8H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0

Table 39. CCON - PCA counter control register (address 0D8H) bit description

Bit	Symbol	Description
7	CF	PCA counter overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
6	CR	PCA counter run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
5	-	Reserved for future use. Should be set to ‘0’ by user programs.
4	CCF4	PCA Module 4 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
3	CCF3	PCA Module 3 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
2	CCF2	PCA Module 2 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
1	CCF1	PCA Module 1 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.
0	CCF0	PCA Module 0 Interrupt Flag. Set by hardware when a match or capture occurs. Must be cleared by software.

Table 40. CCAPMn - PCA modules compare/capture register (address CCAPM0 0DAH, CCAPM1 0DBH, CCAPM2 0DCH, CCAPM3 0DDH, CCAPM4 0DEH) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn

Table 41. CCAPMn - PCA modules compare/capture register (address CCAPM0 0DAH, CCAPM1 0DBH, CCAPM2 0DCH, CCAPM3 0DDH, CCAPM4 0DEH) bit description

Bit	Symbol	Description
7	-	Reserved for future use. Should be set to ‘0’ by user programs.
6	ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
5	CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
4	CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
3	MATn	Match. When MATn = 1 a match of the PCA counter with this module’s compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.

Table 41. CCAPMn - PCA modules compare/capture register (address CCAPM0 0DAH, CCAPM1 0DBH, CCAPM2 0DCH, CCAPM3 0DDH, CCAPM4 0DEH) bit description

Bit	Symbol	Description
2	TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
1	PWMn	Pulse Width Modulation mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
0	ECCFn	Enable CCF Interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

Table 42. PCA module modes (CCAPMn register)

ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	Module function
0	0	0	0	0	0	0	no operation
x	1	0	0	0	0	x	16-bit capture by a positive-edge trigger on CEXn
x	0	1	0	0	0	x	16-bit capture by a negative-edge trigger on CEXn
x	1	1	0	0	0	x	16-bit capture by any transition on CEXn
1	0	0	1	0	0	x	16-bit software timer
1	0	0	1	1	0	x	16-bit high-speed output
1	0	0	0	0	1	0	8-bit PWM
1	0	0	1	x	0	x	Watchdog timer

6.9.1 PCA capture mode

To use one of the PCA modules in the capture mode (Figure 23) either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH).

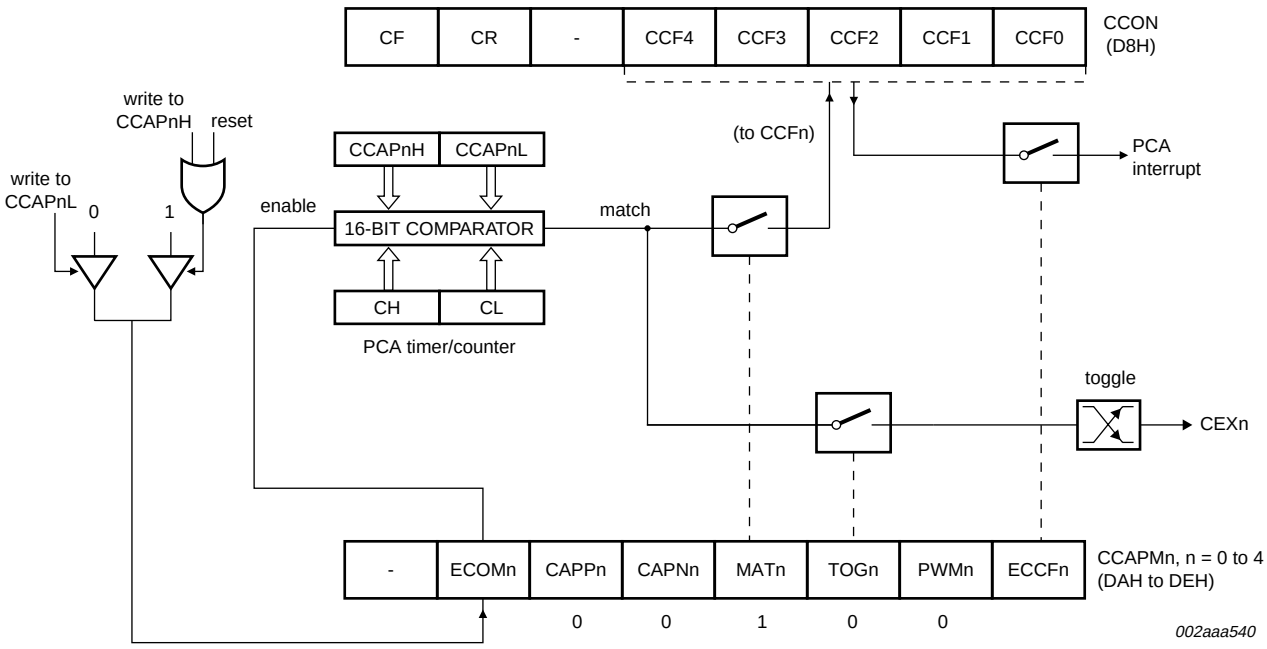


Fig 25. PCA high-speed output mode

6.9.4 PWM mode

All of the PCA modules can be used as PWM outputs (Figure 26). Output frequency depends on the source for the PCA timer.

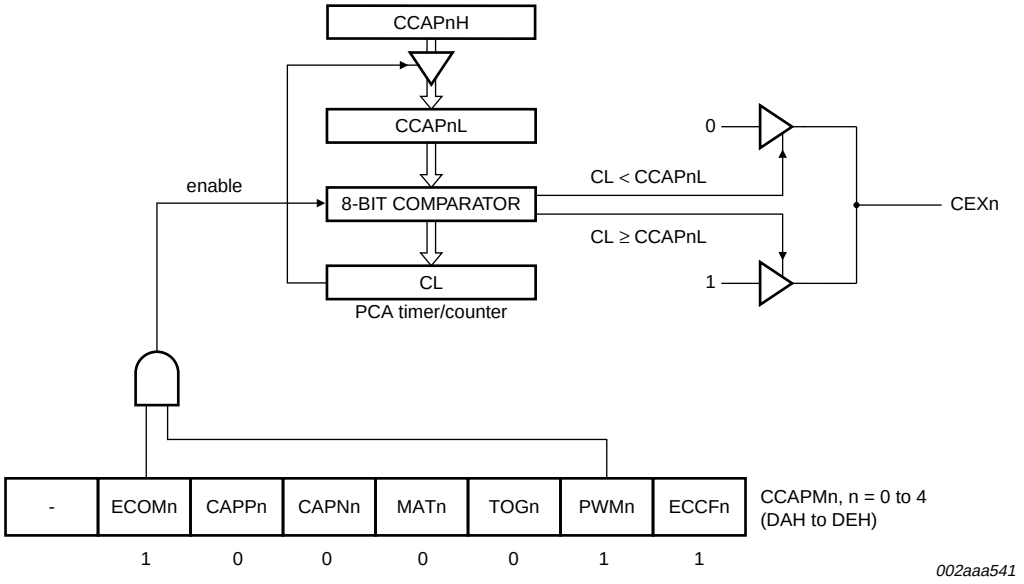


Fig 26. PCA PWM mode

All of the modules will have the same frequency of output because they all share one and only PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPnL. When the value of the PCA CL SFR is less than the

6.13 System clock and clock options

6.13.1 Clock input options and recommended capacitor values for oscillator

Shown in Figure 28 and Figure 29 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 57 shows the typical values for C1 and C2 vs. crystal type for various frequencies.

Table 57. Recommended values for C1 and C2 by crystal type

Crystal	C1 = C2
Quartz	20 pF to 30 pF
Ceramic	40 pF to 50 pF

More specific information about on-chip oscillator design can be found in the *FlashFlex51 Oscillator Circuit Design Considerations* application note.

6.13.2 Clock doubling option

By default, the device runs at 12 clocks per machine cycle (X1 mode). The device has a clock doubling option to speed up to 6 clocks per machine cycle (please see Table 58). Clock double mode can be enabled either by an external programmer or using IAP. When set, the EDC bit in FST register will indicate 6-clock mode.

The clock double mode is only for doubling the internal system clock and the internal flash memory, i.e. $\overline{EA}$ = 1. To access the external memory and the peripheral devices, careful consideration must be taken. Also note that the crystal output (XTAL2) will not be doubled.

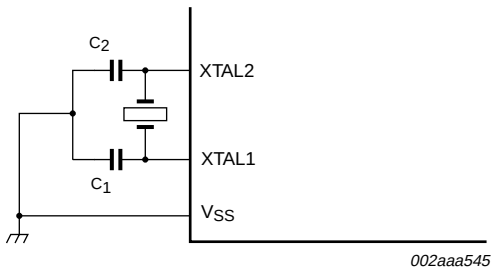


Fig 28. Oscillator characteristics (using the on-chip oscillator)

9. Dynamic characteristics

Table 63. Dynamic characteristics

Over operating conditions: load capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF

T_a = 0 °C to +70 °C or −40 °C to +85 °C; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	X1 mode	0	-	40	MHz
		X2 mode	0	-	20	MHz
		IAP	0.25	-	40	MHz
t_{LHLL}	ALE pulse width		$2T_{cy(clk)} - 15$	-	-	ns
t_{AVLL}	address valid to ALE LOW time		$T_{cy(clk)} - 15$	-	-	ns
t_{LLAX}	address hold after ALE LOW time		$T_{cy(clk)} - 15$	-	-	ns
t_{LLIV}	ALE LOW to valid instruction in time		-	-	$4T_{cy(clk)} - 45$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW time		$T_{cy(clk)} - 15$	-	-	ns
t_{PLPH}	$\overline{PSEN}$ pulse width		$3T_{cy(clk)} - 15$	-	-	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in time		-	-	$3T_{cy(clk)} - 50$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$ time		0	-	-	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$ time		-	-	$T_{cy(clk)} - 15$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid time		$T_{cy(clk)} - 8$	-	-	ns
t_{AVIV}	address to valid instruction in time		-	-	$5T_{cy(clk)} - 60$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float time		-	-	10	ns
t_{RLRH}	$\overline{RD}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	-	ns
t_{WLWH}	$\overline{WR}$ LOW pulse width		$6T_{cy(clk)} - 30$	-	-	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in time		-	-	$5T_{cy(clk)} - 50$	ns
t_{RHDX}	data hold after $\overline{RD}$ time		0	-	-	ns
t_{RHDZ}	data float after $\overline{RD}$ time		-	-	$2T_{cy(clk)} - 12$	ns
t_{LLDV}	ALE LOW to valid data in time		-	-	$8T_{cy(clk)} - 50$	ns
t_{AVDV}	address to valid data in time		-	-	$9T_{cy(clk)} - 75$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW time		$3T_{cy(clk)} - 15$	-	$3T_{cy(clk)} + 15$	ns
t_{AVWL}	address to $\overline{RD}$ or $\overline{WR}$ LOW time		$4T_{cy(clk)} - 30$	-	-	ns
t_{WHQX}	data hold after $\overline{WR}$ time		$T_{cy(clk)} - 20$	-	-	ns
t_{QVWH}	data output valid to $\overline{WR}$ HIGH time		$7T_{cy(clk)} - 50$	-	-	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float time		-	-	0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH time		$T_{cy(clk)} - 15$	-	$T_{cy(clk)} + 15$	ns

[1] $T_{cy(clk)} = 1 / f_{osc}$.

[2] Calculated values are for 6-clock mode only.

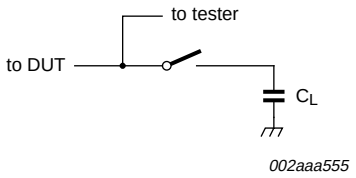
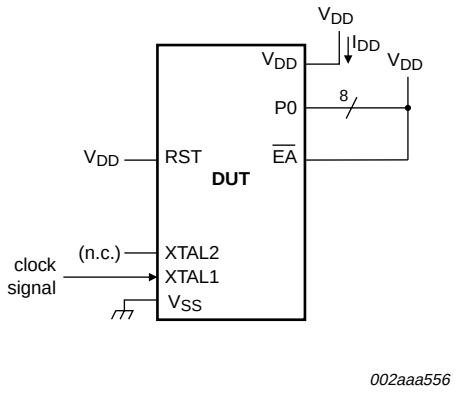
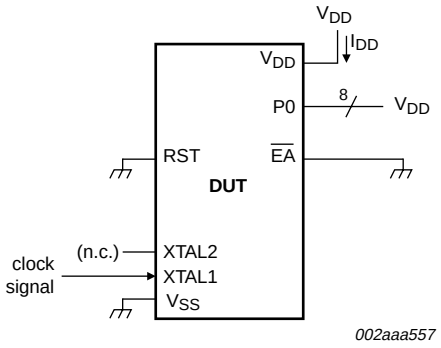


Fig 40. Test load example



All other pins disconnected

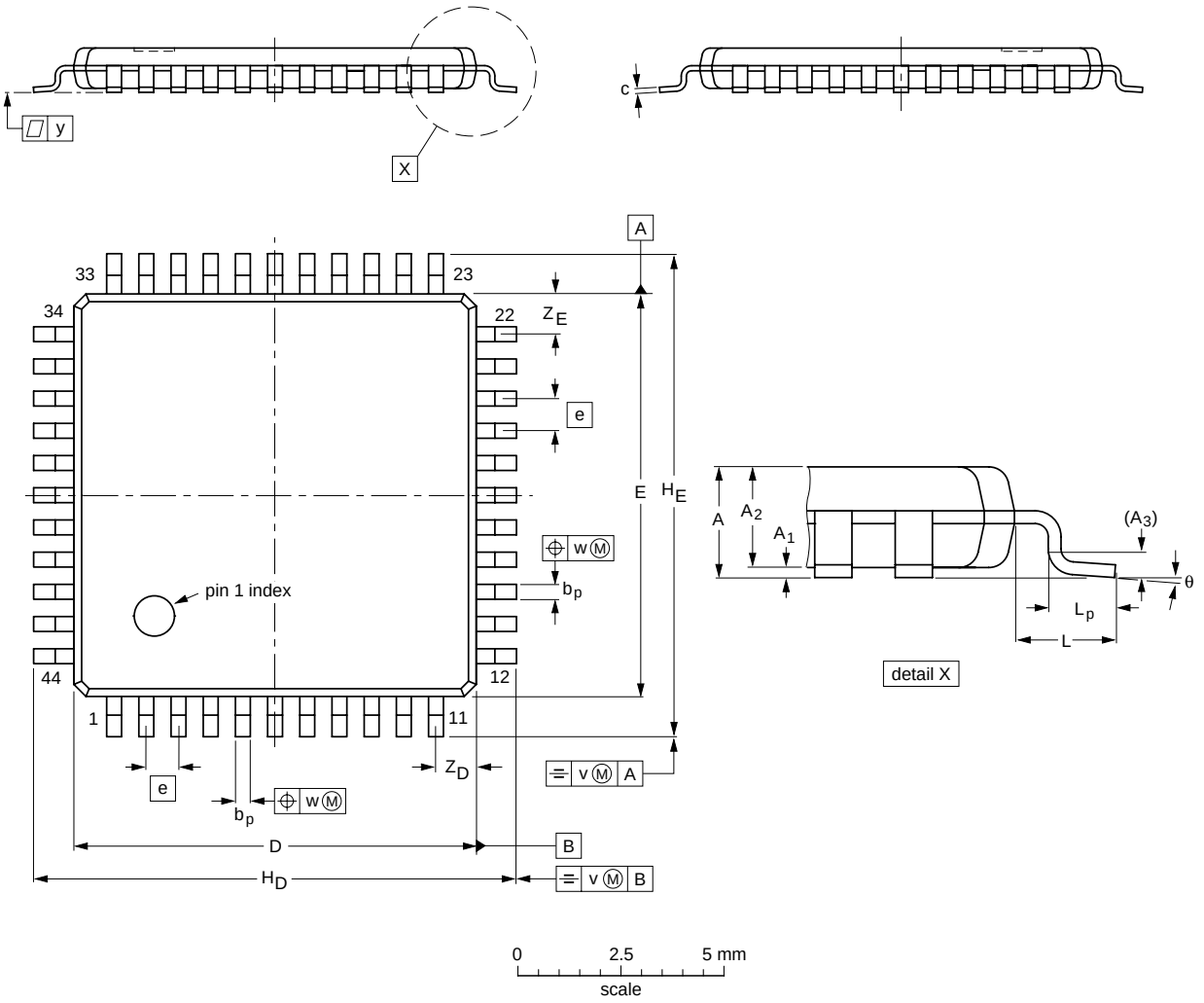
Fig 41. I_{DD} test condition, Active mode



All other pins disconnected

Fig 42. I_{DD} test condition, Idle mode

TQFP44: plastic thin quad flat package; 44 leads; body 10 x 10 x 1.0 mm **SOT376-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.45 0.30	0.18 0.12	10.1 9.9	10.1 9.9	0.8	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT376-1	137E08	MS-026				~~00-01-19~~ 02-03-14

Fig 45. SOT376-1 (TQFP44) package outline

12. Revision history

Table 68. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89V51RB2_RC2_RD2_5	20091112	Product data sheet	-	P89V51RB2_RC2_RD2_4
Modifications:	• Table 37: Changed 2nd row, f_{osc} / 6 to f_{osc} / 2. • Table 62: Changed 12 MHz max values for $I_{DD(oper)}$ and $I_{DD(idle)}$. • Table 3: Removed sentence “However, Security lock level 4 will disable $\overline{EA}$...” from $\overline{EA}$ pin description. • Changed SCK to SPICLK throughout data sheet. • Table 3: Changed SCK to SPICLK and updated pin description.			
P89V51RB2_RC2_RD2_4	20070501	Product data sheet	-	P89V51RB2_RC2_RD2-03
P89V51RB2_RC2_RD2-03	20041202	Product data	-	P89V51RB2_RC2_RD2-02
P89V51RD2-02	20041011	Product data	-	P89V51RD2-01
P89V51RD2-01	20040301	Product data	-	-

15. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 12 November 2009
Document identifier: P89V51RB2_RC2_RD2_5