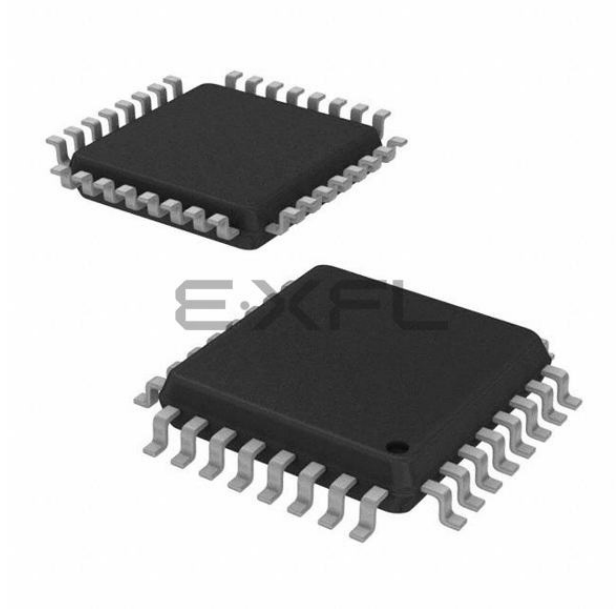

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbusSCI
Peripherals	LVD, Motor Control PWM, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fmc1k2t6

SYSTEM INTEGRITY MANAGEMENT (Cont'd)

SYSTEM INTEGRITY (SI) CONTROL/STATUS REGISTER (SICSR, page 1)

Reset Value: 00000000 (00h)

7							0
PAGE	0	VCOEN	LOCK	PLLEN	0	CKSEL	0

Bit 7 = **PAGE** *SICSR Register Page Selection*
This bit selects the SICSR register page. It is set and cleared by software
0: Access to SICSR register mapped in page 0.
1: Access to SICSR register mapped in page 1.

Bit 6 = Reserved, must be kept cleared.

Bit 5 = **VCOEN** *VCO Enable*
This bit is set and cleared by software.
0: VCO (Voltage Controlled Oscillator) connected to the output of the PLL charge pump (default mode), to obtain a 16-MHz output frequency (with an 8-MHz input frequency).
1: VCO tied to ground in order to obtain a 10-MHz frequency (f_{vco})

Notes:
1. During ICC session, this bit is set to 1 in order to have an internal frequency which does not depend on the input clock. Then, it can be reset in order to run faster with an external oscillator.

Bit 4 = **LOCK** *PLL Locked*
This bit is read only. It is set by hardware. It is set automatically when the PLL reaches its operating frequency.
0: PLL not locked
1: PLL locked

Bit 3 = **PLLEN** *PLL Enable*
This bit enables the PLL and the clock detector. It is set and cleared by software.
0: PLL and Clock Detector (CKD) disabled
1: PLL and Clock Detector (CKD) enabled

Notes:
1. During ICC session, this bit is set to 1.
2. PLL cannot be disabled if PLL clock source is selected (CKSEL= 1).

Bit 2 = Reserved, must be kept cleared.

Bit 1 = **CKSEL** *Clock Source Selection*
This bit selects the clock source: oscillator clock or clock from the PLL. It is set and cleared by software. It can also be set by option byte (PLL opt)
0: Oscillator clock selected
1: PLL clock selected

Notes:
1. During ICC session, this bit is set to 1. Then, CKSEL can be reset in order to run with f_{OSC}.
2. Clock from the PLL cannot be selected if the PLL is disabled (PLLEN =0)
3. If the clock source is selected by PLL option bit, CKSEL bit selection has no effect.

Bit 0 = Reserved, must be kept cleared.

I/O PORTS (Cont'd)

Table 13. I/O Port Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
Reset Value of all I/O port registers		0	0	0	0	0	0	0	0
0000h	**PADR**	MSB							LSB
0001h	**PADDR**								
0002h	**PAOR**								
0003h	**PBDR**	MSB							LSB
0004h	**PBDDR**								
0005h	**PBOR**								
0006h	**PCDR**	MSB							LSB
0007h	**PCDDR**								
0008h	**PCOR**								
0009h	**PDDR**	MSB							LSB
000Ah	**PDDDR**								
000Bh	**PDOR**								
000Ch	**PEDR**	MSB							LSB
000Dh	**PEDDR**								
000Eh	**PEOR**								
000Fh	**PFDR**	MSB							LSB
0010h	**PFDDR**								
0011h	**PFOR**								
0012h	**PGDR**	MSB							LSB
0013h	**PGDDR**								
0014h	**PGOR**								
0015h	**PHDR**	MSB							LSB
0016h	**PHDDR**								
0017h	**PHOR**								

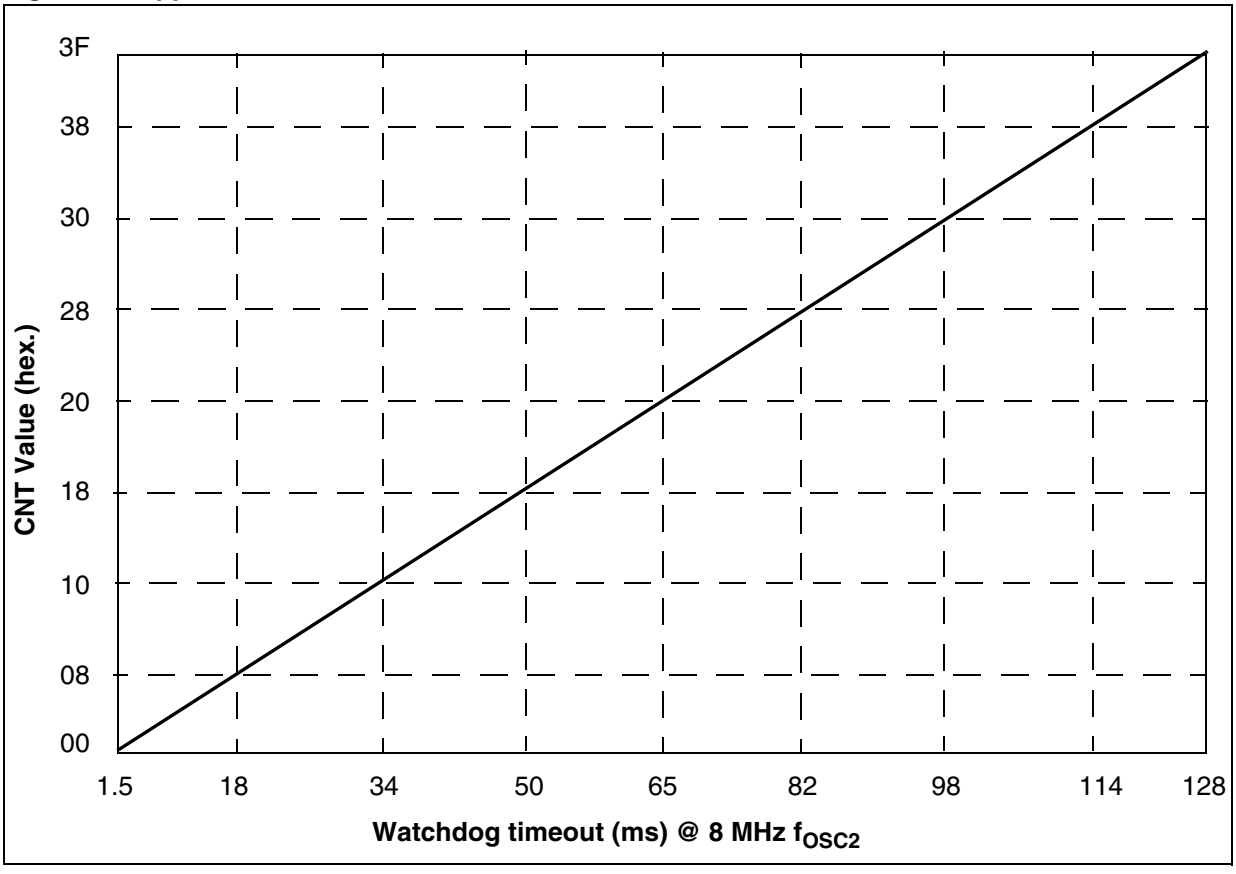
WINDOW WATCHDOG (Cont'd)

10.1.5 How to Program the Watchdog Timeout

Figure 35 shows the linear relationship between the 6-bit value to be loaded in the Watchdog Counter (CNT) and the resulting timeout duration in milliseconds. This can be used for a quick calculation without taking the timing variations into account. If more precision is needed, use the formulae in Figure 36.

Caution: When writing to the WDGCR register, always write 1 in the T6 bit to avoid generating an immediate reset.

Figure 35. Approximate Timeout Duration



ON-CHIP PERIPHERALS (Cont'd)

PWM CONTROL REGISTER (PWMCR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
OE3	OE2	OE1	OE0	OP3	OP2	OP1	OP0

Bit 7:4 = **OE[3:0]** *PWM Output Enable*
These bits are set and cleared by software. They enable or disable the PWM output channels independently acting on the corresponding I/O pin.
0: PWM output disabled.
1: PWM output enabled.

Bit 3:0 = **OP[3:0]** *PWM Output Polarity*
These bits are set and cleared by software. They independently select the polarity of the four PWM output signals.

PWMx output level		OPx
Counter <= OCRx	Counter > OCRx	
1	0	0
0	1	1

Note: When an OPx bit is modified, the PWMx output signal polarity is immediately reversed.

DUTY CYCLE REGISTERS (PWMDCRx)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0

Bit 7:0 = **DC[7:0]** *Duty Cycle Data*

These bits are set and cleared by software.

A PWMDCRx register is associated with the OCRx register of each PWM channel to determine the second edge location of the PWM signal (the first edge location is common to all channels and given by the ARTARR register). These PWMDCR registers allow the duty cycle to be set independently for each PWM channel.

SERIAL PERIPHERAL INTERFACE (cont'd)

10.4.5.4 Single Master and Multimaster Configurations

There are two types of SPI systems:

– Single Master System

– Multimaster System

Single Master System

A typical single master system may be configured using a device as the master and four devices as slaves (see Figure 61).

The master device selects the individual slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the slave devices.

The $\overline{SS}$ pins are pulled high during reset since the master device ports will be forced to be inputs at that time, thus disabling the slave devices.

Note: To prevent a bus conflict on the MISO line, the master allows only one active slave device during a transmission.

For more security, the slave device may respond to the master with the received data byte. Then the master will receive the previous byte back from the slave device if all MISO and MOSI pins are connected and the slave has not written to its SPIDR register.

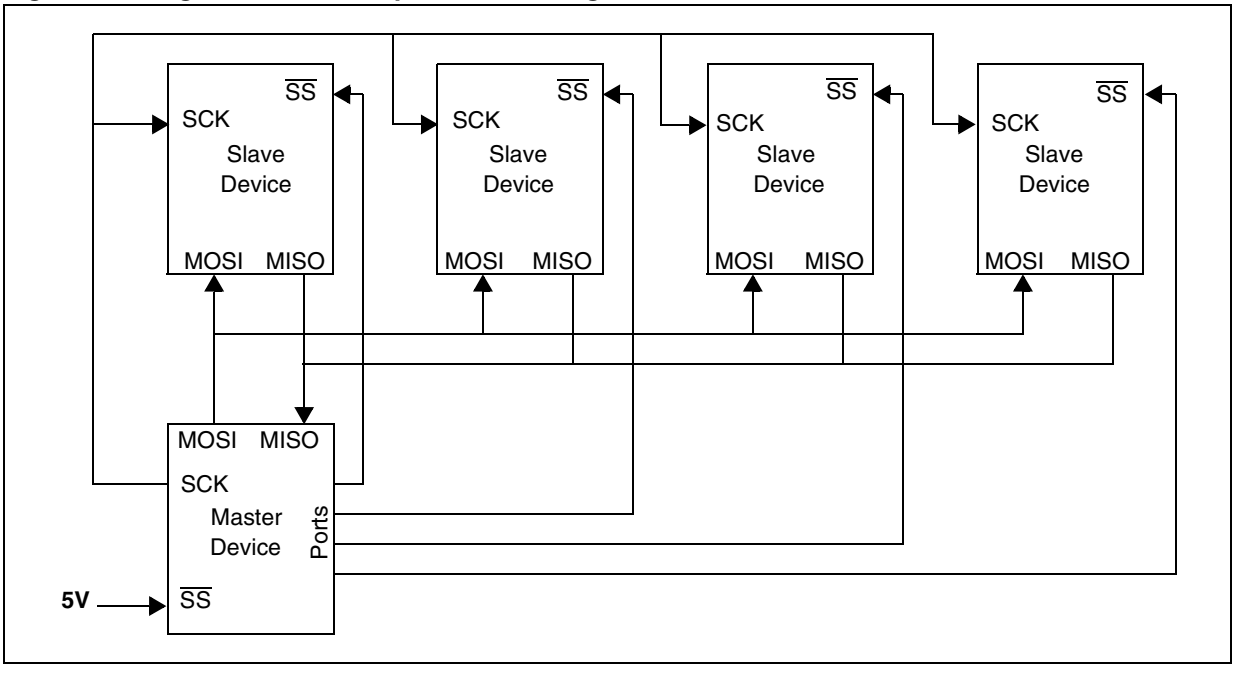
Other transmission security methods can use ports for handshake lines or data bytes with command fields.

Multimaster System

A multimaster system may also be configured by the user. Transfer of master control could be implemented using a handshake method through the I/O ports or by an exchange of code messages through the serial peripheral interface system.

The multimaster system is principally handled by the MSTR bit in the SPICR register and the MODF bit in the SPICSR register.

Figure 61. Single Master / Multiple Slave Configuration



LINSCI™ SERIAL COMMUNICATION INTERFACE (SCI Mode) (cont'd)

10.5.5.6 Receiver Muting and Wake-up Feature

In multiprocessor configurations it is often desirable that only the intended message recipient should actively receive the full message contents, thus reducing redundant SCI service overhead for all non-addressed receivers.

The non-addressed devices may be placed in sleep mode by means of the muting function.

Setting the RWU bit by software puts the SCI in sleep mode:

All the reception status bits can not be set.

All the receive interrupts are inhibited.

A muted receiver may be woken up in one of the following ways:

– by Idle Line detection if the WAKE bit is reset,

– by Address Mark detection if the WAKE bit is set.

Idle Line Detection

Receiver wakes up by Idle Line detection when the Receive line has recognized an Idle Line. Then the RWU bit is reset by hardware but the IDLE bit is not set.

This feature is useful in a multiprocessor system when the first characters of the message determine the address and when each message ends by an idle line: As soon as the line becomes idle, every receivers is waken up and analyse the first characters of the message which indicates the addressed receiver. The receivers which are not addressed set RWU bit to enter in mute mode. Consequently, they will not treat the next characters constituting the next part of the message. At the end of the message, an idle line is sent by the transmitter: this wakes up every receivers which are ready to analyse the addressing characters of the new message.

In such a system, the inter-characters space must be smaller than the idle time.

Address Mark Detection

Receiver wakes up by Address Mark detection when it received a "1" as the most significant bit of a word, thus indicating that the message is an address. The reception of this particular word wakes up the receiver, resets the RWU bit and sets the RDRF bit, which allows the receiver to receive this word normally and to use it as an address word.

This feature is useful in a multiprocessor system when the most significant bit of each character (except for the break character) is reserved for Address Detection. As soon as the receivers received an address character (most significant bit = '1'), the receivers are waken up. The receivers which are not addressed set RWU bit to enter in mute mode. Consequently, they will not treat the next characters constituting the next part of the message.

10.5.5.7 Parity Control

Hardware byte Parity control (generation of parity bit in transmission and parity checking in reception) can be enabled by setting the PCE bit in the SCICR1 register. Depending on the character format defined by the M bit, the possible SCI character formats are as listed in Table 20.

Note: In case of wake-up by an address mark, the MSB bit of the data is taken into account and not the parity bit

Table 20. Character Formats

M bit	PCE bit	Character format
0	0	ǀ SB ǀ 8 bit data ǀ STB ǀ
	1	ǀ SB ǀ 7-bit data ǀ PB ǀ STB ǀ
1	0	ǀ SB ǀ 9-bit data ǀ STB ǀ
	1	ǀ SB ǀ 8-bit data ǀ PB ǀ STB ǀ

Legend: SB = Start Bit, STB = Stop Bit, PB = Parity Bit

Even parity: The parity bit is calculated to obtain an even number of "1s" inside the character made of the 7 or 8 LSB bits (depending on whether M is equal to 0 or 1) and the parity bit.

Example: data = 00110101; 4 bits set => parity bit will be 0 if even parity is selected (PS bit = 0).

Odd parity: The parity bit is calculated to obtain an odd number of "1s" inside the character made of the 7 or 8 LSB bits (depending on whether M is equal to 0 or 1) and the parity bit.

Example: data = 00110101; 4 bits set => parity bit will be 1 if odd parity is selected (PS bit = 1).

Transmission mode: If the PCE bit is set then the MSB bit of the data written in the data register is not transmitted but is changed by the parity bit.

Reception mode: If the PCE bit is set then the interface checks if the received data byte has an even number of "1s" if even parity is selected (PS = 0) or an odd number of "1s" if odd parity is selected (PS = 1). If the parity check fails, the PE flag is set in the SCISR register and an interrupt is generated if PCIE is set in the SCICR1 register.

LINSCI™ SERIAL COMMUNICATION INTERFACE (SCI Mode) (cont'd)

10.5.6 Low Power Modes

Mode	Description
Wait	No effect on SCI. SCI interrupts cause the device to exit from Wait mode.
Halt	SCI registers are frozen. In Halt mode, the SCI stops transmitting/receiving until Halt mode is exited.

10.5.7 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Transmit Data Register Empty	TDRE	TIE	Yes	No
Transmission Complete	TC	TCIE		
Received Data Ready to be Read	RDRF	RIE		
Overrun Error or LIN Synch Error Detected	OR/ LHE			
Idle Line Detected	IDLE	ILIE		
Parity Error	PE	PIE		
LIN Header Detection	LHDF	LHIE		

The SCI interrupt events are connected to the same interrupt vector (see Interrupts chapter).

These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

LINSCI™ SERIAL COMMUNICATION INTERFACE (LIN Mode) (cont'd)

LIN PRESCALER FRACTION REGISTER (LPFR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	LPFR 3	LPFR 2	LPFR 1	LPFR 0

Bits 7:4 = Reserved.

Bits 3:0 = **LPFR[3:0]** *Fraction of LDIV*

These 4 bits define the fraction of the LIN Divider (LDIV):

LPFR[3:0]	Fraction (LDIV)
0h	0
1h	1/16
...	...
Eh	14/16
Fh	15/16

1. When initializing LDIV, the LPFR register must be written first. Then, the write to the LPR register will effectively update LDIV and so the clock generation.

2. In LIN Slave mode, if the LPR[7:0] register is equal to 00h, the transceiver and receiver input clocks are switched off.

Examples of LDIV coding:

Example 1: LPR = 27d and LPFR = 12d

This leads to:

Mantissa (LDIV) = 27d

Fraction (LDIV) = 12/16 = 0.75d

Therefore LDIV = 27.75d

Example 2: LDIV = 25.62d

This leads to:

LPFR = rounded(16*0.62d)

= rounded(9.92d) = 10d = Ah

LPR = mantissa (25.620d) = 25d = 1Bh

Example 3: LDIV = 25.99d

This leads to:

LPFR = rounded(16*0.99d)

= rounded(15.84d) = 16d

MOTOR CONTROLLER (Cont'd)

10.6.5 Functional Description

The MTC can be split into five main parts as shown in the simplified block diagram in Figure 77. Each of these parts may be configured for different purposes:

- INPUT DETECTION BLOCK with a comparator, an input multiplexer and an incremental encoder interface, which may work as:
  - A BEMF zero-crossing detector
  - A Speed Sensor Interface
- The DELAY MANAGER with an 8/16-bit timer and an 8x8 bit multiplier, which may work as a:
  - 8-bit delay manager
  - Speed Measurement unit
- The PWM MANAGER, including a measurement window generator, a mode selector and a current comparator.
- The CHANNEL MANAGER with the PWM multiplexer, polarity programming, deadtime insertion and high frequency chopping capability and emergency HiZ configuration input.
- The THREE-PHASE PWM GENERATOR with 12-bit free-running counter and repetition counter.

10.6.6 Input Detection Block

This block can operate in Position sensor mode, in sensorless mode or in Speed Sensor mode. The mode is selected via the SR bit in the MCRA register and the TES[1:0] bits in MPAR register (refer to Table 35 for set-up information). The block diagram is shown in Figure 78 for the Position Sensor/Sensorless modes (TES[1:0] = 00) and in Figure 88 for the Speed Sensor mode (TES[1:0] = 01, 10, 11).

10.6.6.1 Input Pins

The MCIA, MCIB and MCIC input pins can be used as analog or as digital pins.

- In sensorless mode, the analog inputs are used to measure the BEMF zero crossing and to detect the end of demagnetization if required.
- In sensor mode, the analog inputs are used to get the Hall sensor information.
- In speed sensor mode (e.g. tachogenerator), the inputs are used as digital pins. When using an AC tachogenerator, a small external circuit may be needed to convert the incoming signal into a square wave signal which can be treated by the MTC.

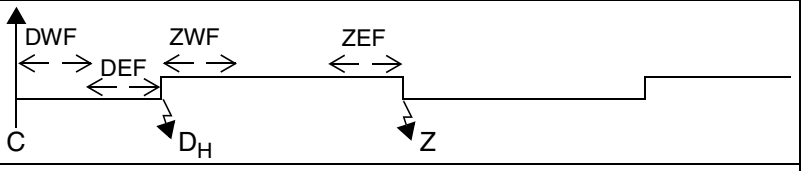
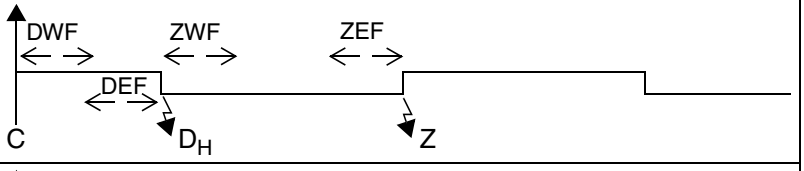
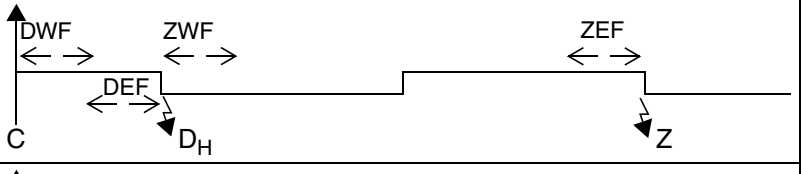
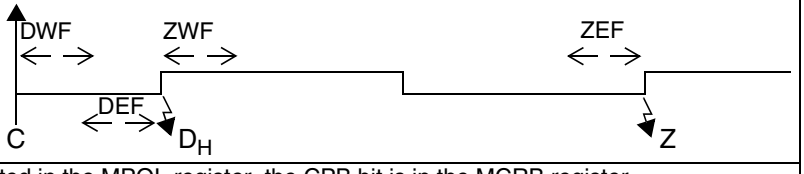
Due to the presence of diodes, these pins can permanently support an input current of 5mA. In sensorless mode, this feature enables the inputs to be connected to each motor phase through a single resistor.

A multiplexer, programmed by the IS[1:0] bits in the MPHST register selects the input pins and connects them to the control logic in either sensorless or tachogenerator mode. In encoder mode, it is mandatory to connect sensor digital outputs to the MCIA and MCIB pins.

MOTOR CONTROLLER (Cont'd)

Table 30 shows the event control selected by the ZVD and CPB bits. In most cases, the D and Z events have opposite edge polarity, so the ZVD bit is usually 0.

Table 30. ZVD and CPB Edge Selection Bits

ZVD bit	CPB bit	Event generation vs input data sampled
0	0	
0	1	
1	0	
1	1	
Note: The ZVD bit is located in the MPOL register, the CPB bit is in the MCRB register.		

Legend:

DWF= D window filter

DEF= D event filter

ZWF = Z window filter

ZEF = Z event filter

Refer also to Table 34 on page 162.

MOTOR CONTROLLER (Cont'd)

10.6.6.9 Sampling block

For a full digital solution, the phase comparator output sampling frequency is the frequency of the PWM signal applied to the switches and the sampling for the Z event detection in sensorless mode is done at the end of the off time of this PWM signal to avoid to have to re-create a virtual ground because when the PWM signal is off, the star point is at ground due to the free-wheeling diode. That's why, the sampling for Z event detection is done by default during the OFF-state of the PWM signal and therefore at the PWM frequency.

In current mode, this PWM signal is generated by a combination of the output of the measurement window generator (SA[3:0] bits), the output of the current comparator and a minimum OFF time set by the OT[3:0] bits for system stabilisation.

In voltage mode, this PWM signal is generated by the 12-bit PWM generator signal in the compare U register with still a minimum OFF time required if the sampling is done at the end of the OFF time of the PWM signal for system stabilisation. The PWM signal is put OFF as soon as the current feedback reaches the current input limitation. This can add an OFF time to the one programmed with the 12-bit Timer.

For D event detection in sensorless mode, no specific PWM configuration is needed and the sampling frequency ($f_{SCF,}$ see Table 82) is completely independent from the PWM signal.

In sensor mode, the D event detection is not needed as the MCIA, MCIB and MCIC pins are the digital signals coming from the hall sensors so no specific PWM configuration is needed and the sampling for the Z detection event is done at f_{SCF}, completely independent from the PWM signal.

In sensorless mode, if a virtual ground is created by the addition of an external circuit, sampling for the Z event detection can be completely independent from the PWM signal applied to the switches. Setting the SPLG bit in the MCRC register allows a sampling frequency of f_{SCF} for Z event detection independent from the PWM signal after getting the D (end of demagnetisation) event. This means that the sampling order is given whatever the PWM signal (during the ON time or the OFF time). As soon as the SPLG bit is set in the MCRC register, the minimum OFF time needed for the PWM signal in current mode is set to 0µs and a true 100% duty cycle can be set in the 12-bit PWM generator compare register in voltage mode.

Specific applications can require sampling for the Z event detection only during the ON time of the PWM signal. This can happen when the PWM signal is applied only on the low side switches for Z event detection. In this case, during the OFF time of the PWM signal, the phase voltage is tied to the application voltage V and no back-EMF signal can be seen. During the ON time of the PWM signal, the phase voltage can be compared to the neutral point voltage and the Z event can be detected. Therefore, it is possible to add a programmable delay before sampling (which is normally done when the PWM signal is switched ON) to perform the sampling during the ON time of the PWM signal. This delay is set with the DS [3:0] bits in the MCONF register.

Table 33. Delay length before sampling

DS3	DS2	DS1	DS0	Delay added to sample at Ton
0	0	0	0	No delay added. Sample during Toff
0	0	0	1	2.5 µs
0	0	1	0	5 µs
0	0	1	1	7.5 µs
0	1	0	0	10 µs
0	1	0	1	12.5 µs
0	1	1	0	15 µs
0	1	1	1	17.5 µs
1	0	0	0	20 µs
1	0	0	1	22.5 µs
1	0	1	0	25 µs
1	0	1	1	27.5 µs
1	1	0	0	30 µs
1	1	0	1	32.5 µs
1	1	1	0	35 µs
1	1	1	1	37.5 µs

Note: Times are indicated for 4 MHz f_{PERIPH}

As soon as a delay is set in the DS[3:0] bits, the minimum OFF time for the PWM signal is no longer required and it is automatically set to 0µs in current mode in the internal sampling clock and a true 100% duty cycle can be set in the 12-bit PWM generator compare U register if needed.

MOTOR CONTROLLER (Cont'd)

10.6.7.5 Speed Measurement Mode

Motor speed can be measured using two methods depending on sensor type: period measurement or pulse counting. Typical sensor handling is described here.

Incremental encoders allows accurate speed measurement by providing a large number of pulses per revolution (ppr) with ppr rates up to several thousands; the higher the ppr rate, the higher the resolution. The proposed method consists of counting the number of clock cycles issued by the Incremental Encoder Interface (Encoder Clock) during a fixed time window (refer to Figure 100).

The tachogenerator has a much lower ppr rate than the encoder (typically factor 10). In this context, it is more meaningful to measure the period between Tacho Captures (i.e. relevant transitions of the incoming signals). Accuracy is imposed by the reference clock, i.e. the CPU clock (refer to Figure 99).

Figure 99. Tachogenerator period acquisition using MTIM timer

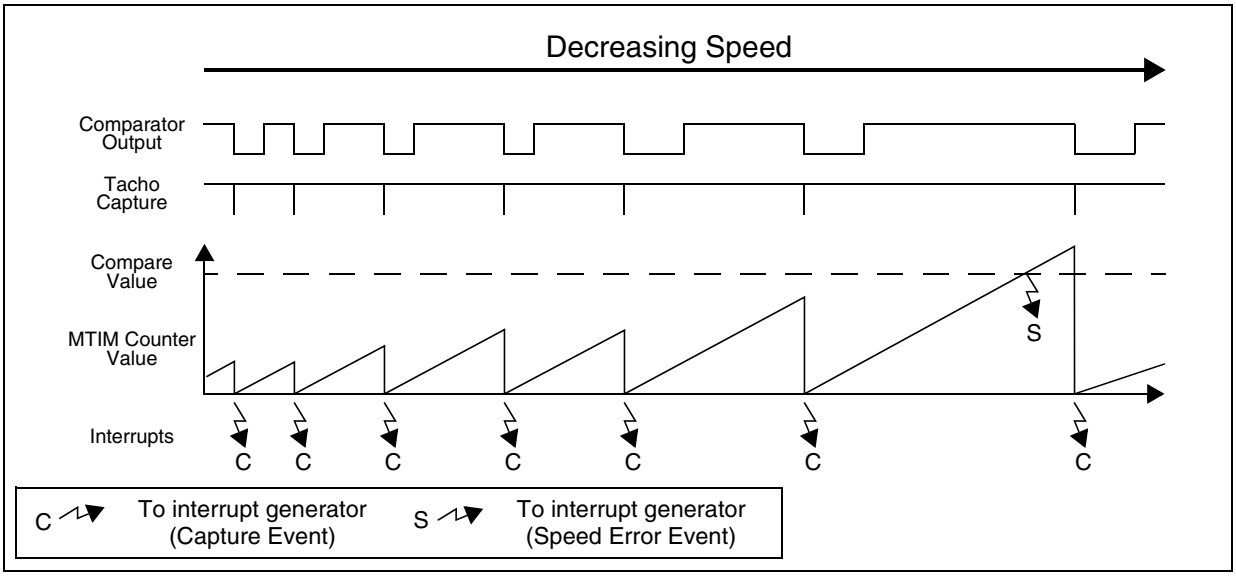
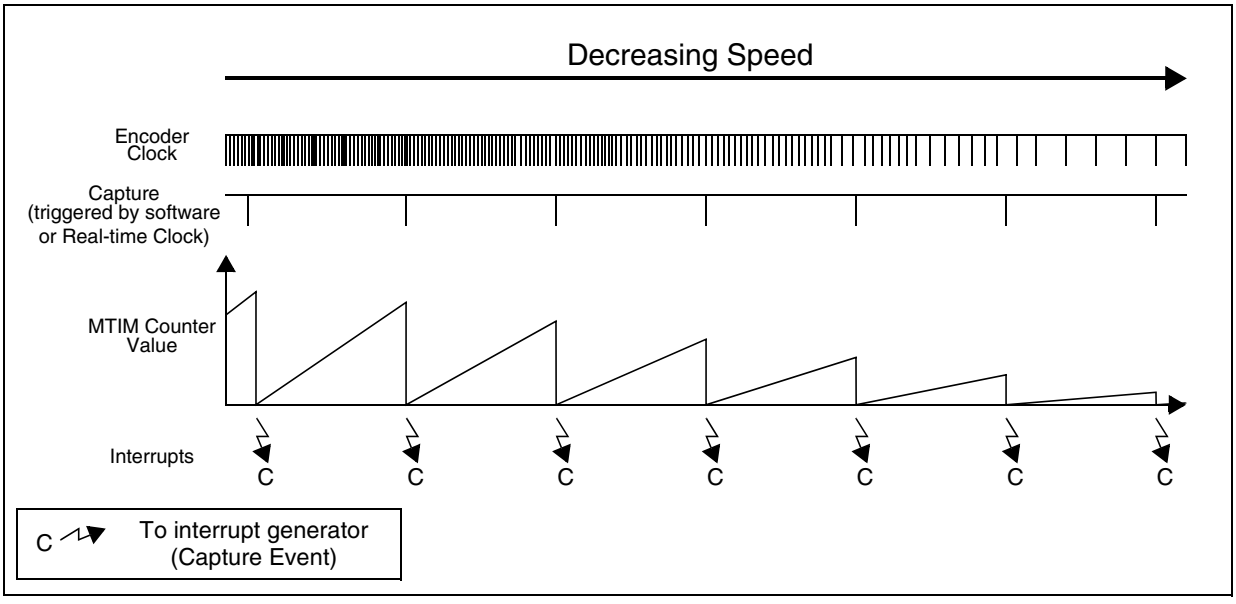


Figure 100. Encoder Clock frequency measure using MTIM timer



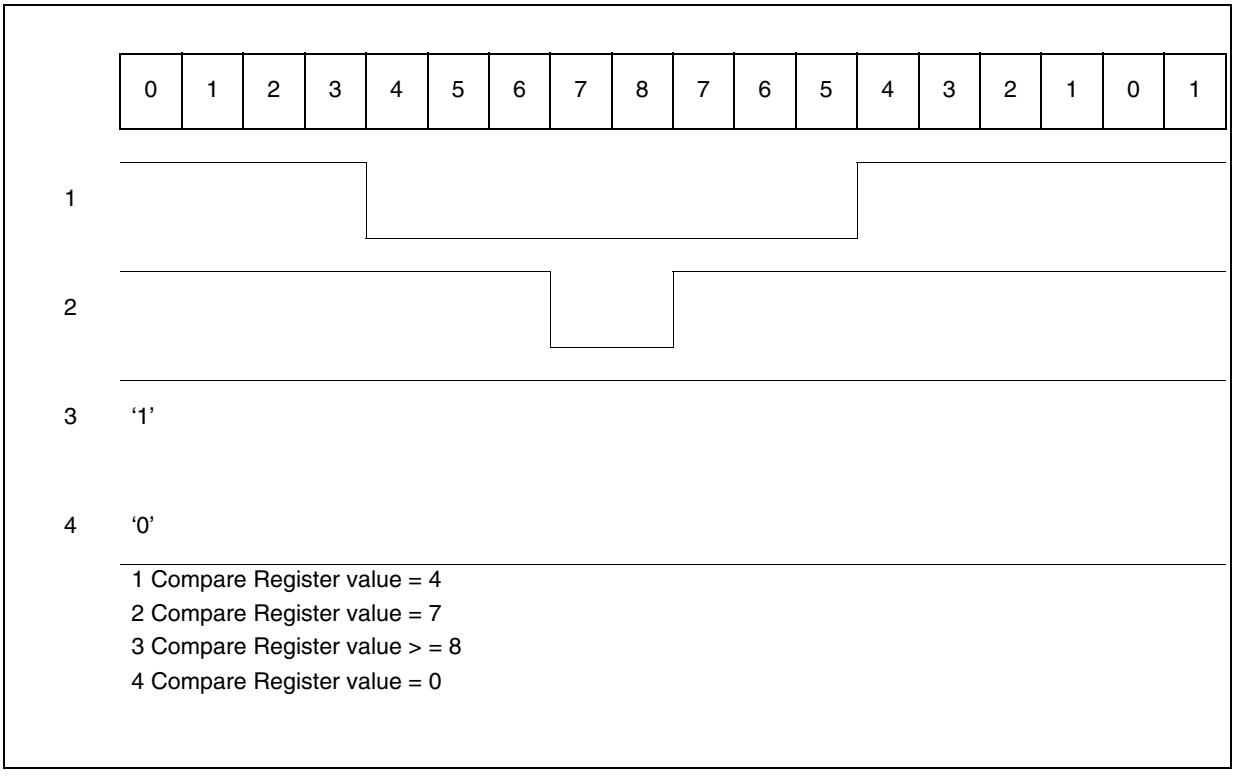
MOTOR CONTROLLER (Cont'd)

If the 13-bit Compare register value is greater than the extended Compare 0 Register (the 13th bit is set to '0'), the corresponding PWM output signal is held at '1'.

If the 13-bit Compare register value is 0, the corresponding PWM output signal is held at '0'.

Figure 119 shows some center-aligned PWM waveforms in an example where the Compare 0 register value = 8.

Figure 119. Center-aligned PWM Waveforms (Compare 0 Register = 8)



MOTOR CONTROLLER (Cont'd)

- Edge-aligned Mode (CMS bit = 0)

In this operating mode, the PWM Counter counts up to the value loaded in the 12-bit Compare Register. Then the PWM Counter is cleared and it restarts counting up.

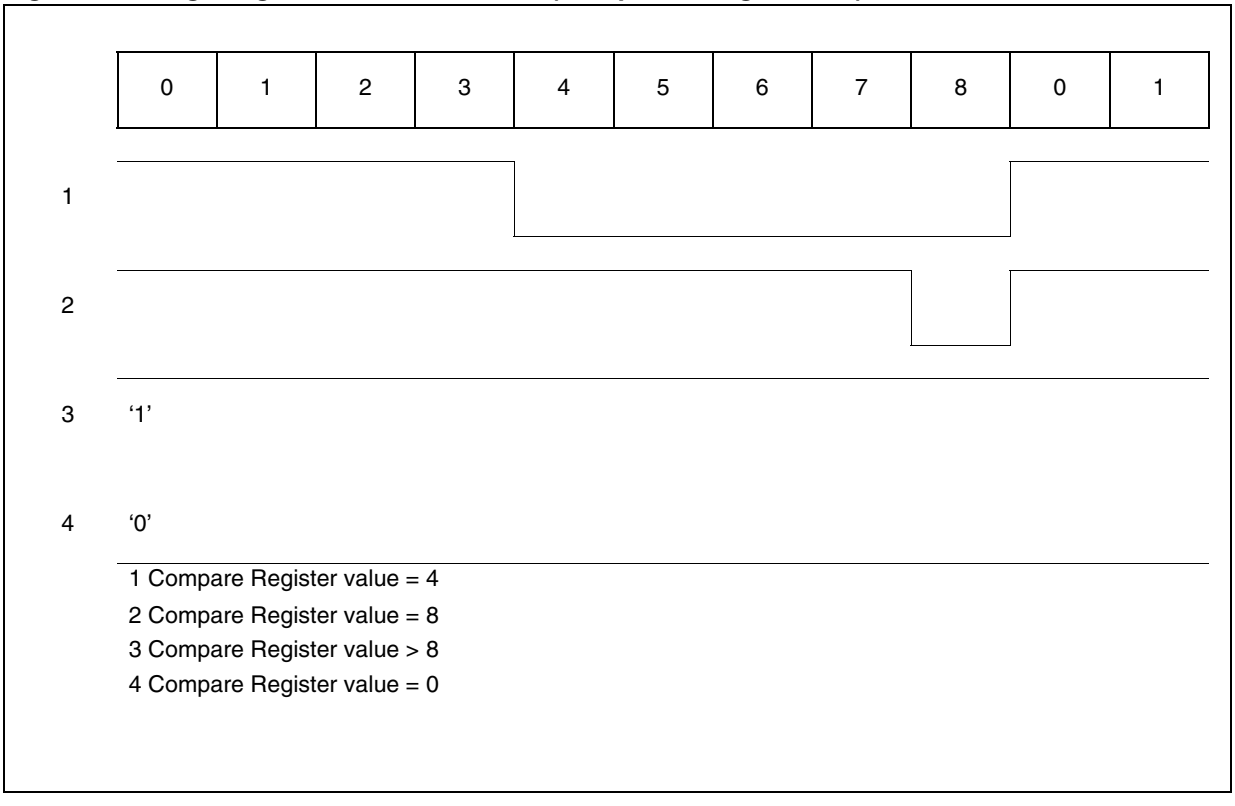
The PWM signals are set to '0' when the PWM Counter reaches, in up-counting, the corresponding 13-bit Compare register value and they are set to '1' when the PWM Counter is cleared.

If the 13-bit Compare register value is greater than the extended Compare 0 register (the 13th bit is set to '0'), the corresponding PWM output signal is held at '1'.

If the 13-bit Compare register value = 0, the corresponding PWM output signal is held at '0'.

Figure 120 shows some edge-aligned PWM waveforms in an example where the Compare 0 register value = 8.

Figure 120. Edge-aligned PWM Waveforms (Compare 0 Register = 8)



MOTOR CONTROLLER (Cont'd)

CONTROL REGISTER B (MCRB)
Read/Write
Reset Value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
0	CPB*	HDM*	SDM*	OCV	OS2*	OS1	OS0

Bit 7= Reserved, must be kept at reset value.

Bit 6= **CPB***: *Compare Bit for Zero-crossing detection.*
0: Zero crossing detection on falling edge
1: Zero crossing detection on rising edge

Bit 5= **HDM***: *Hardware Demagnetization event Mask bit*
0: Hardware Demagnetization disabled
1: Hardware Demagnetization enabled

Bit 4= **SDM***: *Simulated Demagnetization event Mask bit*
0: Simulated Demagnetization disabled
1: Simulated Demagnetization enabled

Bit 3 = **OCV**: Over Current Handling in Voltage mode
0: Over Current protection is OFF
1:Over current protection is ON

This bit acts as follows

Table 60. Over current handling

CLIM bit	CLI bit	OCV bit	Output effect	Interrupt
0	0	x	Normal running mode	No
0	1	x	PWM is put off as Current loop effect	No
1	0	x	Normal running mode	No
1	1	0	PWM is put off as Current loop effect	Yes
1	1	1	All MCOx outputs are put in reset state (MOE reset) [1)]	Yes

Note 1: This feature is also available when using the three PWM outputs (PCN bit=1 in the MDTG register), providing that the VOC1bit = 0 (MCRA register). See section 10.6.8.2 on page 186

Bits 2:0 = **OS2*, OS[1:0]**: *Operating output mode Selection bits*

Refer to the Step behaviour diagrams (Figure 109, Figure 110) and Table 61, "Step Behaviour/ sensorless mode," on page 212.

These bits are used to define the various PWM output configurations.

Note: OS2 is the only preload bit.

Table 61. Step Behaviour/ sensorless mode

OS2 bit	PWM after C and before D	OS1 bit	PWM after D and before Z	OS0	PWM after Z and before next C
0	On High Channels	0	On High Channels	0	On high channels
				1	On low channels
		1	On Low Channels	0	On high channels
				1	On low channels
1	On Low Channels	0	On High Channels	0	On high channels
				1	On low channels
		1	On Low Channels	0	On high channels
				1	On low channels

Note: For more details, see Step behaviour diagrams (Figure 109 and Figure 110).

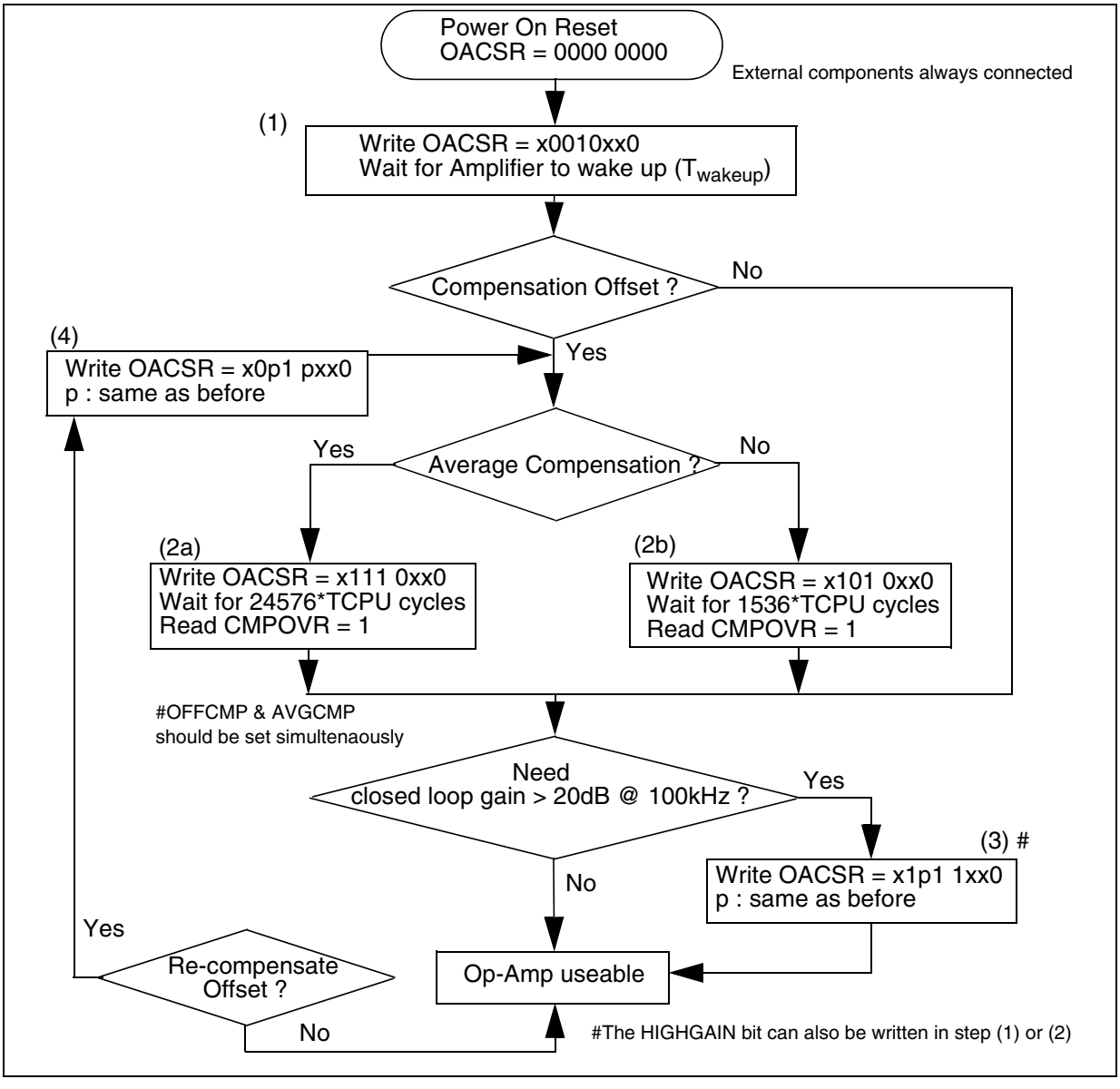
* Preload bits, new value taken into account at the next C event. A C event is generated at each write to MPHST in Direct Access mode.

OP-AMP MODULE (Cont'd)

10.7.5 Op-Amp Programming

The flowchart for Op-Amp operation is shown in Figure 126

Figure 126. Normal Op-Amp Operation



12.5 CLOCK AND TIMING CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

12.5.1 General Timings

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$t_{c(INST)}$	Instruction cycle time		2	3	12	t_{CPU}
		f_{CPU}=8MHz	250	375	1500	ns
$t_{v(IT)}$	Interrupt reaction time [2] $t_{v(IT)} = \Delta t_{c(INST)} + 10$		10		22	t_{CPU}
		f_{CPU}=8MHz	1.25		2.75	µs

Notes:

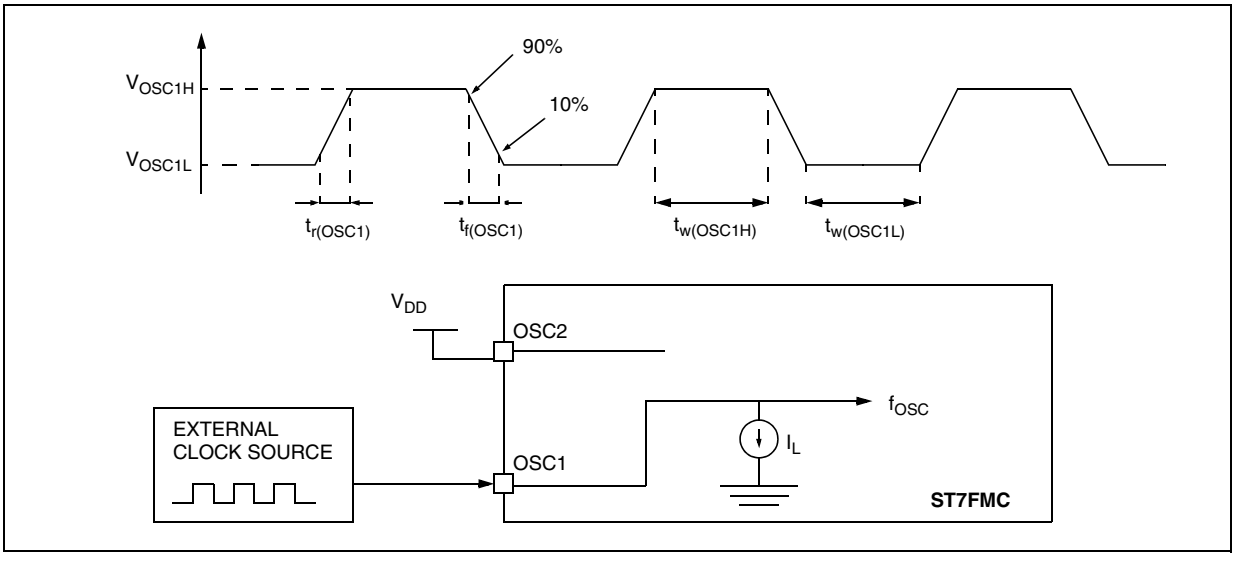
1. Data based on typical application software.

2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

12.5.2 External Clock Source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OSC1H}	OSC1 input pin high level voltage	see Figure 135	0.7xV_{DD}		V_{DD}	V
V_{OSC1L}	OSC1 input pin low level voltage		V_{SS}		0.3xV_{DD}	
$t_{w(OSC1H)}$ $t_{w(OSC1L)}$	OSC1 high or low time [1]		25			ns
$t_{r(OSC1)}$ $t_{f(OSC1)}$	OSC1 rise or fall time [1]				5	
I_L	OSCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			± 1	µA

Figure 135. Typical Application with an External Clock Source



Notes:

1. Data based on design simulation and/or technology characteristics, not tested in production.

12.14 10-BIT ADC CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AREF}	Analog Reference Voltage		3		V_{DD}	V
f_{ADC}	ADC clock frequency				4	MHz
V_{AIN}	Conversion voltage range [1]		V_{SSA}		V_{AREF}	V
I_{lkg}	Positive input leakage current for analog input				±1	µA
	Negative input leakage current on analog pins	$V_{IN}<V_{SS,}$ | I_{IN} |< 400µA on adjacent analog pin		5	6	µA
R_{AIN}	External input impedance				see Figure 157 and Figure 158 [2)3)4)]	kΩ
C_{AIN}	External capacitor on analog input					pF
f_{AIN}	Variation freq. of analog input signal					Hz
C_{ADC}	Internal sample and hold capacitor			6		pF
t_{ADC}	Conversion time (Sample+Hold)	f_{CPU}=8MHz, f_{ADC}=4MHz, ADSTS bit in MCCBCR register = 0	3.5			µs
	- Sample capacitor loading time - Hold conversion time		4 10			$1/f_{ADC}$
	Conversion time (Sample+Hold)	f_{CPU}=8MHz, f_{ADC}=4MHz, ADSTS bit in MCCBCR register = 1	6.5			µs
	- Sample capacitor loading time - Hold conversion time		16 10			$1/f_{ADC}$
R_{AREF}	Analog Reference Input Resistor			11		kΩ

Figure 157. R_{AIN} max. vs f_{ADC} with C_{AIN}=0pF[3)]

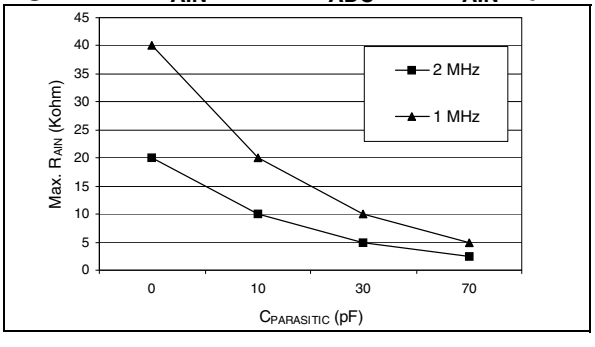
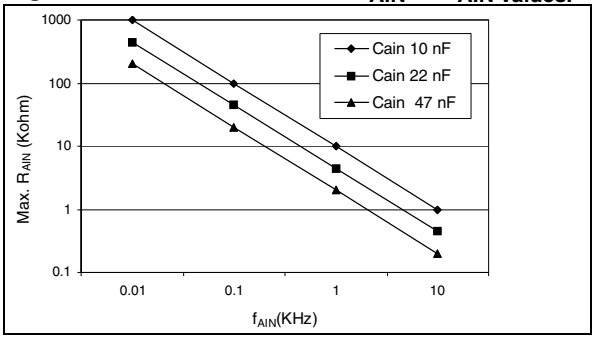


Figure 158. Recommended C_{AIN} & R_{AIN} values.[4)]



ST7MC DEVICE CONFIGURATION AND ORDERING INFORMATION (Cont'd)

OPTION BYTE 1

OPT7:5= **PKG[2:0]** *package selection*
These option bits are used to select the device package.

Selected Package	PKG2	PKG1	PKG0
LQFP32 / SDIP32	0	0	0
LQFP44	0	0	1
SDIP 56	0	1	0
LQFP64	0	1	1
LQFP80	1	x	x

OPT4:2= Reserved

OPT1:0 = **MCO** *Motor Control Output Options*
MCO port under reset.

Motor Control Output	bit 1	bit 0
HiZ	0	0
Low	0	1
High	1	0
HiZ	1	1

IMPORTANT NOTES (Cont'd)

Impact on application

Software may execute the interrupt routine twice after header reception.

Moreover, in reception mode, as the receiver is no longer in mute mode, an interrupt will be generated on each data byte reception.

Workaround

The problem can be detected in the LINSCI interrupt routine. In case of timeout error (LHE is set and LHLR is loaded with 00h), the software can check the RWU bit in the SCICR2 register. If RWU is cleared, it can be set by software. Refer to Figure 169. Workaround is shown in bold characters.

Figure 169. LINSCI Interrupt routine

```
@interrupt void LINSCI_IT ( void ) /* LINSCI interrupt routine */
{
      /* clear flags */
      SCISR_buffer = SCISR;
      SCIDR_buffer = SCIDR;

      if ( SCISR_buffer & LHE )/* header error ? */
      {
            if (!LHLR)/* header time-out? */
            {
                  if ( !(SCICR2 & RWU) )/* active mode ? */
                  {
                        _asm("sim");/* disable interrupts */
                        SCISR;
                        SCIDR;/* Clear RDRF flag */
                        SCICR2 |= RWU;/* set mute mode */
                        SCISR;
                        SCIDR;/* Clear RDRF flag */
                        SCICR2 |= RWU;/* set mute mode */
                        _asm("rim");/* enable interrupts */
                  }
            }
      }
}
```

Example using Cosmic compiler syntax

15.5 MISSING DETECTION OF BLDC "Z EVENT"

For a BLDC drive, the Dead Time generator is enabled through the MDTG register (PCN=0 and DTE=1). If the duty cycle of the PWM signal generated to drive the motor is lower than the programmed deadtime, the Z event sampling will be missing.

Workaround

The complementary PWM must be disabled by resetting the DTE bit in the MDTG register (see page 221).

As the current in the motor is very low in this case, the MOSFET body diode can be used.

15.6 INJECTED CURRENT ON PD7

On rev.B silicon, the parameter Iinj(pin), injected current on I/O pins (see section 12.8.1 on page 264), is limited at 0 (instead of -2mA) for the pin PD7. This limitation is no longer present on rev.C and A silicon and all I/O pins have the max values +5/-2 mA.

15.7 RESET VALUE OF UNAVAILABLE PINS

On A silicon versions, some ports (Ports A, C and E) have less than 8 pins. The bits associated to the unavailable pins must always be kept at reset state.