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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbusSCI, SPI
Peripherals	LVD, Motor Control PWM, POR, PWM, WDT
Number of I/O	44
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fmc2r6t6

FLASH PROGRAM MEMORY (Cont'd)

4.5 ICP (IN-CIRCUIT PROGRAMMING)

To perform ICP the microcontroller must be switched to ICC (In-Circuit Communication) mode by an external controller or programming tool.

Depending on the ICP code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection serial communication interface for downloading).

When using an STMicroelectronics or third-party programming tool that supports ICP and the specific microcontroller device, the user needs only to implement the ICP hardware interface on the application board (see Figure 10). For more details on the pin locations, refer to the device pinout description.

4.6 IAP (IN-APPLICATION PROGRAMMING)

This mode uses a BootLoader program previously stored in Sector 0 by the user (in ICP mode or by plugging the device in a programming tool).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored, etc.). For example, it is possible to download code from the SPI, SCI or other type of serial interface and program it in the Flash. IAP mode can be used to program any of the Flash sectors except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

4.7 RELATED DOCUMENTATION

For details on Flash programming and ICC protocol, refer to the *ST7 Flash Programming Reference Manual* and to the *ST7 ICC Protocol Reference Manual*.

4.8 REGISTER DESCRIPTION

FLASH CONTROL/STATUS REGISTER (FCSR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	0	0

This register is reserved for use by Programming Tool software. It controls the Flash programming and erasing operations.

10 ON-CHIP PERIPHERALS

10.1 WINDOW WATCHDOG (WWDG)

10.1.1 Introduction

The Window Watchdog is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The Watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the contents of the downcounter before the T6 bit becomes cleared. An MCU reset is also generated if the 7-bit downcounter value (in the control register) is refreshed before the downcounter has reached the window register value. This implies that the counter must be refreshed in a limited window.

10.1.2 Main Features

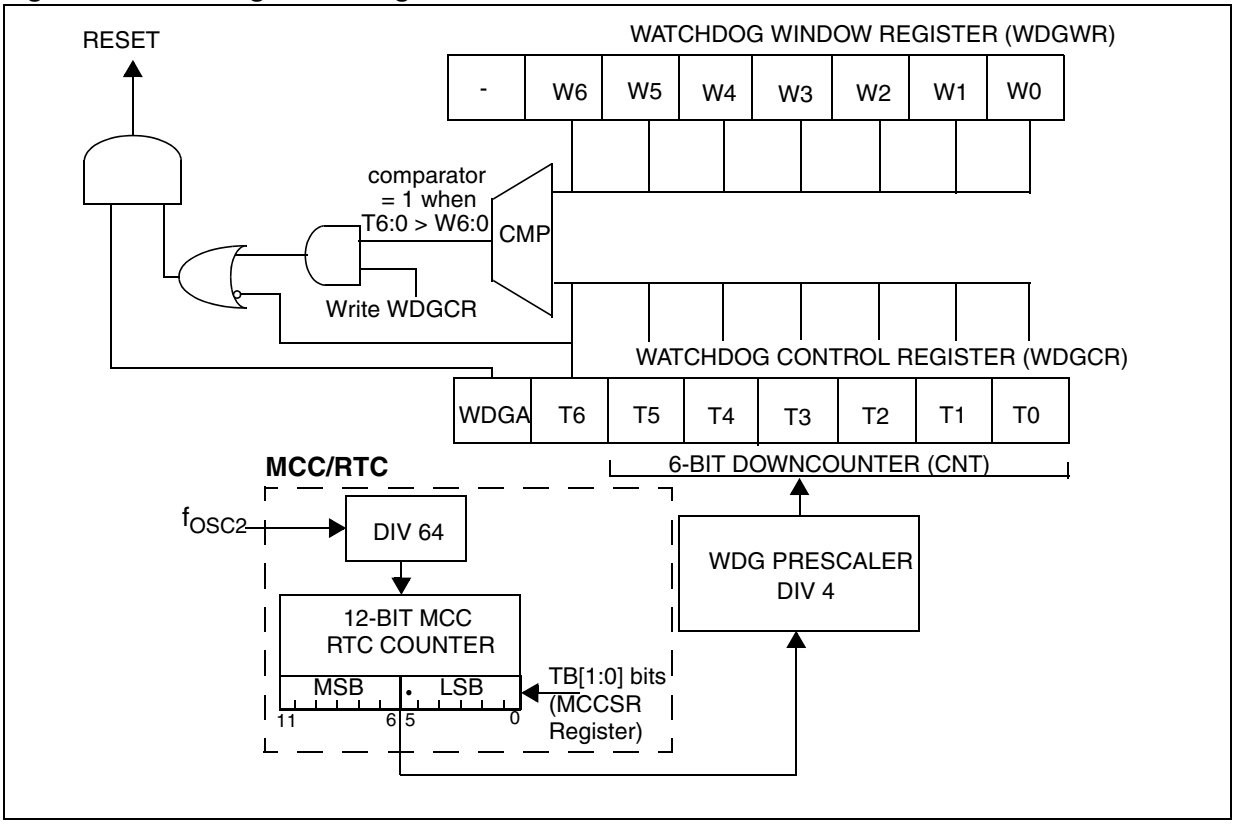
- Programmable free-running downcounter
- Conditional reset
  - Reset (if watchdog activated) when the downcounter value becomes less than 40h
  - Reset (if watchdog activated) if the downcounter is reloaded outside the window (see Figure 37)
- Hardware/Software Watchdog activation (selectable by option byte)
- Optional reset on HALT instruction (configurable by option byte)

10.1.3 Functional Description

The counter value stored in the WDGCR register (bits T[6:0]), is decremented every 16384 f_{OSC2} cycles (approx.), and the length of the timeout period can be programmed by the user in 64 increments.

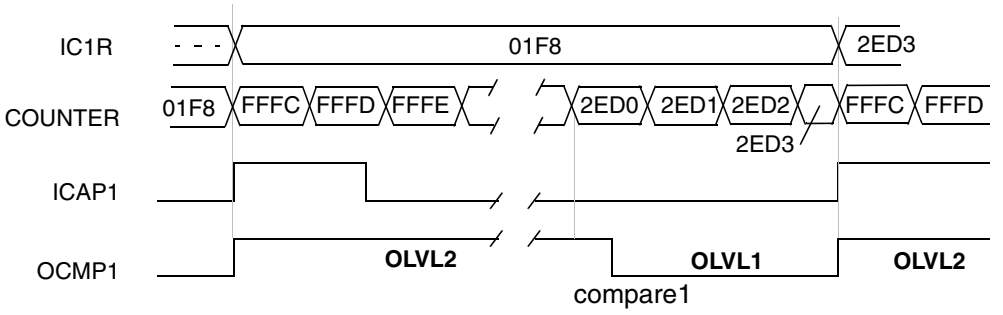
If the watchdog is activated (the WDGA bit is set) and when the 7-bit downcounter (T[6:0] bits) rolls over from 40h to 3Fh (T6 becomes cleared), it initiates a reset cycle pulling low the reset pin for typically 30µs. If the software reloads the counter while the counter is greater than the value stored in the window register, then a reset is generated.

Figure 34. Watchdog Block Diagram



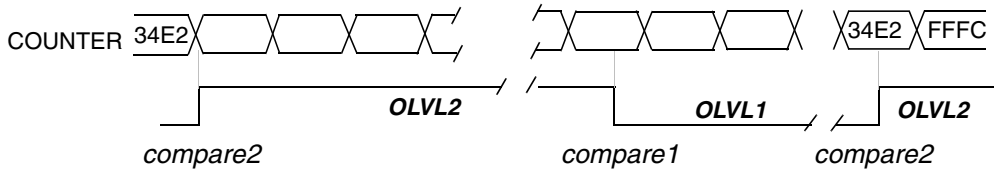
16-BIT TIMER (Cont'd)

Figure 53. One Pulse Mode Timing Example



Note: IEDG1=1, OC1R=2ED0h, OLVL1=0, OLVL2=1

Figure 54. Pulse Width Modulation Mode Timing Example



Note:

(cont'd)

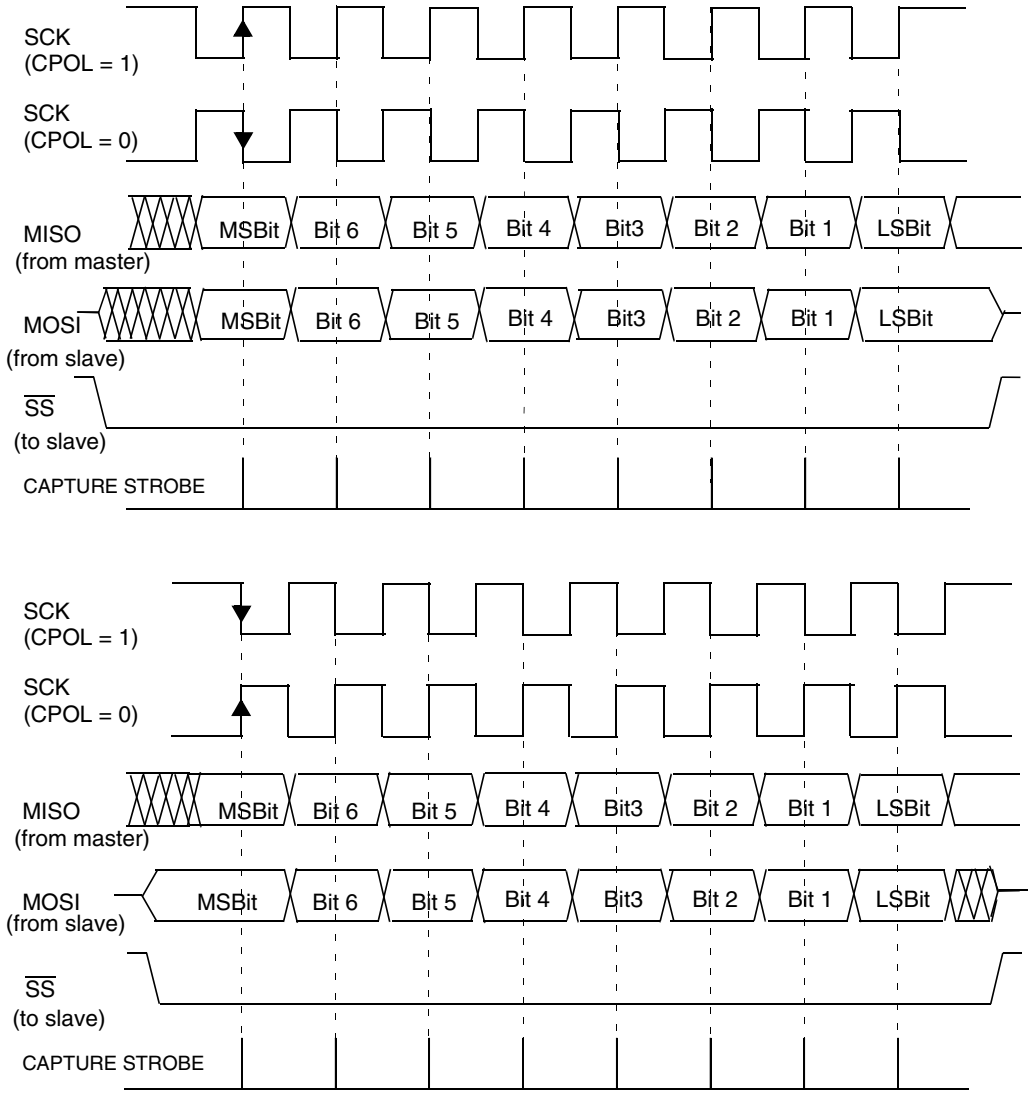
Four possible timing relationships may be chosen by software, using the CPOL and CPHA bits (See Figure 59).

The idle state of SCK must correspond to the polarity selected in the SPICSR register (by pulling up SCK if CPOL = 1 or pulling down SCK if CPOL = 0).

The combination of the CPOL clock polarity and CPHA (clock phase) bits selects the data capture clock edge.

Figure 59 shows an SPI transfer with the four combinations of the CPHA and CPOL bits. The diagram may be interpreted as a master or slave timing diagram where the SCK pin, the MISO pin and the MOSI pin are directly connected between the master and the slave device.

: If CPOL is changed at the communication byte boundaries, the SPI must be disabled by resetting the SPE bit.



Note: This figure should not be used as a replacement for parametric information. Refer to the Electrical Characteristics chapter.

LINSCI™ SERIAL COMMUNICATION INTERFACE (SCI Mode) (cont'd)

10.5.5.4 Conventional Baud Rate Generation

The baud rates for the receiver and transmitter (Rx and Tx) are set independently and calculated as follows:

$$Tx = \frac{f_{CPU}}{(16*PR)*TR} \qquad Rx = \frac{f_{CPU}}{(16*PR)*RR}$$

with:

PR = 1, 3, 4 or 13 (see SCP[1:0] bits)

TR = 1, 2, 4, 8, 16, 32, 64,128

(see SCT[2:0] bits)

RR = 1, 2, 4, 8, 16, 32, 64,128

(see SCR[2:0] bits)

All these bits are in the SCIBRR register.

Example: If f_{CPU} is 8 MHz (normal mode) and if PR = 13 and TR = RR = 1, the transmit and receive baud rates are 38400 baud.

Note: The baud rate registers MUST NOT be changed while the transmitter or the receiver is enabled.

10.5.5.5 Extended Baud Rate Generation

The extended prescaler option gives a very fine tuning on the baud rate, using a 255 value prescaler, whereas the conventional Baud Rate Generator retains industry standard software compatibility.

The extended baud rate generator block diagram is described in Figure 64.

The output clock rate sent to the transmitter or to the receiver will be the output from the 16 divider divided by a factor ranging from 1 to 255 set in the SCIERPR or the SCIETPR register.

Note: The extended prescaler is activated by setting the SCIETPR or SCIERPR register to a value other than zero. The baud rates are calculated as follows:

$$Tx = \frac{f_{CPU}}{16*ETPR*(PR*TR)} \qquad Rx = \frac{f_{CPU}}{16*ERPR*(PR*RR)}$$

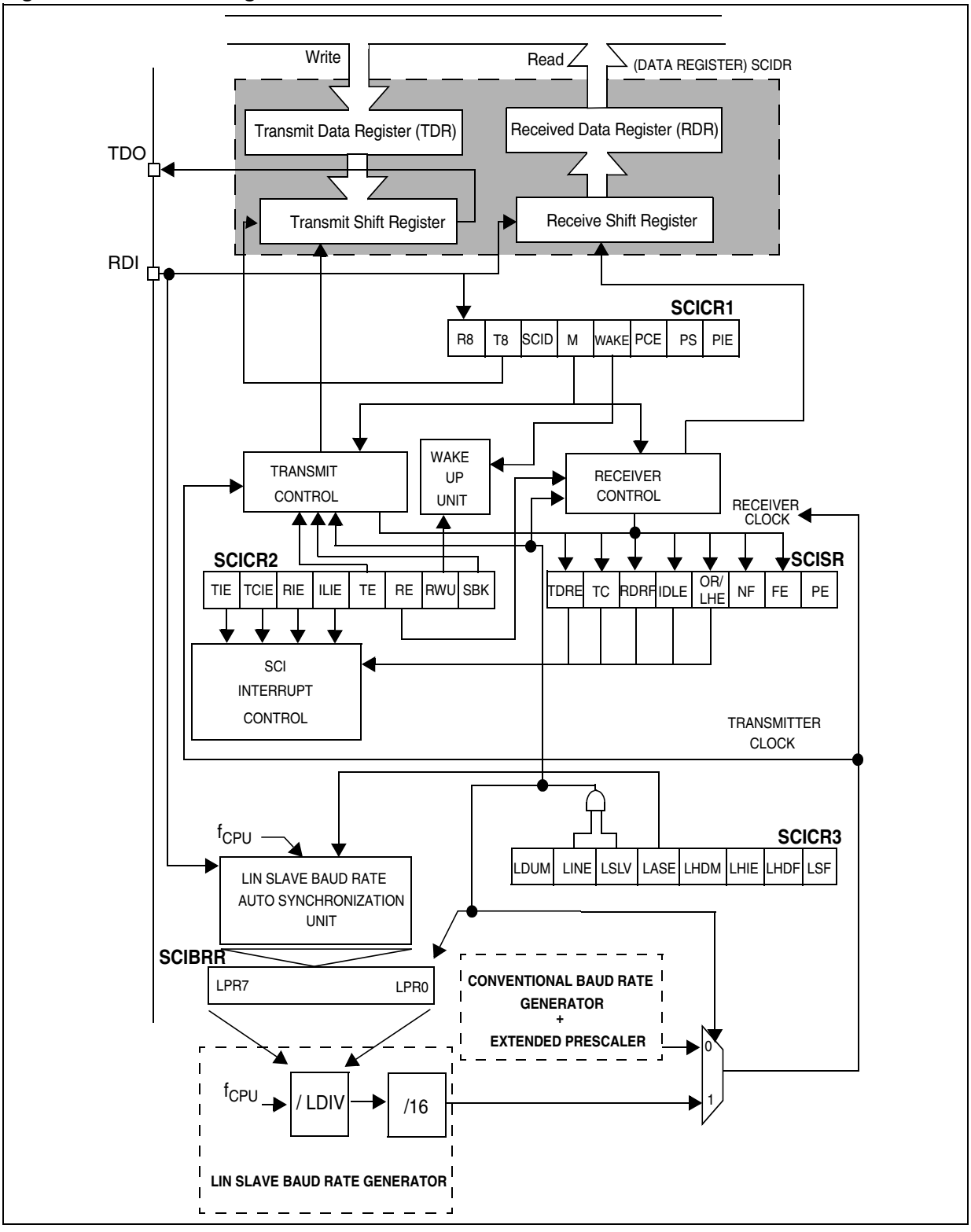
with:

ETPR = 1, ..., 255 (see SCIETPR register)

ERPR = 1, ..., 255 (see SCIERPR register)

LINSCI™ SERIAL COMMUNICATION INTERFACE (LIN Mode) (cont'd)

Figure 66. SCI Block Diagram in LIN Slave Mode



LINSCI™ SERIAL COMMUNICATION INTERFACE (LIN Mode) (cont'd)

10.5.10 LIN Mode Register Description

STATUS REGISTER (SCISR)
Read Only
Reset Value: 1100 0000 (C0h)

7							0
TDRE	TC	RDRF	IDLE	LHE	NF	FE	PE

Bits 7:4 = Same function as in SCI mode, please refer to Section 10.5.8 SCI Mode Register Description.

Bit 3 = **LHE** *LIN Header Error*.
During LIN Header this bit signals three error types:

– The LIN Synch Field is corrupted and the SCI is blocked in LIN Synch State (LSF bit = 1).

– A timeout occurred during LIN Header reception

– An overrun error was detected on one of the header field (see OR bit description in Section 10.5.8 SCI Mode Register Description)).

An interrupt is generated if RIE = 1 in the SCICR2 register. If blocked in the LIN Synch State, the LSF bit must first be reset (to exit LIN Synch Field state and then to be able to clear LHE flag). Then it is cleared by the following software sequence: An access to the SCISR register followed by a read to the SCIDR register.
0: No LIN Header error
1: LIN Header error detected

Note:

Apart from the LIN Header this bit signals an Overrun Error as in SCI mode, (see description in Section 10.5.8 SCI Mode Register Description)

Bit 2 = **NF** *Noise flag*

In LIN Master mode (LINE bit = 1 and LSLV bit = 0) this bit has the same function as in SCI mode, please refer to Section 10.5.8 SCI Mode Register Description

In LIN Slave mode (LINE bit = 1 and LSLV bit = 1) this bit has no meaning.

Bit 1 = **FE** *Framing error.*
In LIN slave mode, this bit is set only when a real framing error is detected (if the stop bit is dominant (0) and at least one of the other bits is recessive (1). It is not set when a break occurs, the LHDF bit is used instead as a break flag (if the LHDM bit = 0). It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).
0: No Framing error
1: Framing error detected

Bit 0 = **PE** *Parity error.*
This bit is set by hardware when a LIN parity error occurs (if the PCE bit is set) in receiver mode. It is cleared by a software sequence (a read to the status register followed by an access to the SCIDR data register). An interrupt is generated if PIE = 1 in the SCICR1 register.
0: No LIN parity error
1: LIN Parity error detected

CONTROL REGISTER 1 (SCICR1)
Read/Write
Reset Value: x000 0000 (x0h)

7							0
R8	T8	SCID	M	WAKE	PCE	PS	PIE

Bits 7:3 = Same function as in SCI mode, please refer to Section 10.5.8 SCI Mode Register Description.

Bit 2 = **PCE** *Parity control enable.*
This bit is set and cleared by software. It selects the hardware parity control for LIN identifier parity check.
0: Parity control disabled
1: Parity control enabled

When a parity error occurs, the PE bit in the SCISR register is set.

Bit 1 = Reserved

Bit 0 = Same function as in SCI mode, please refer to Section 10.5.8 SCI Mode Register Description.

MOTOR CONTROLLER (Cont'd)

10.6.6.3 D Event detection

In sensorless mode, the D Window Filter becomes active after each C event. It blanks out the D event during the time window defined by the DWF[3:0] bits in the MDFR register (see Table 26). The reset value is 200µs.

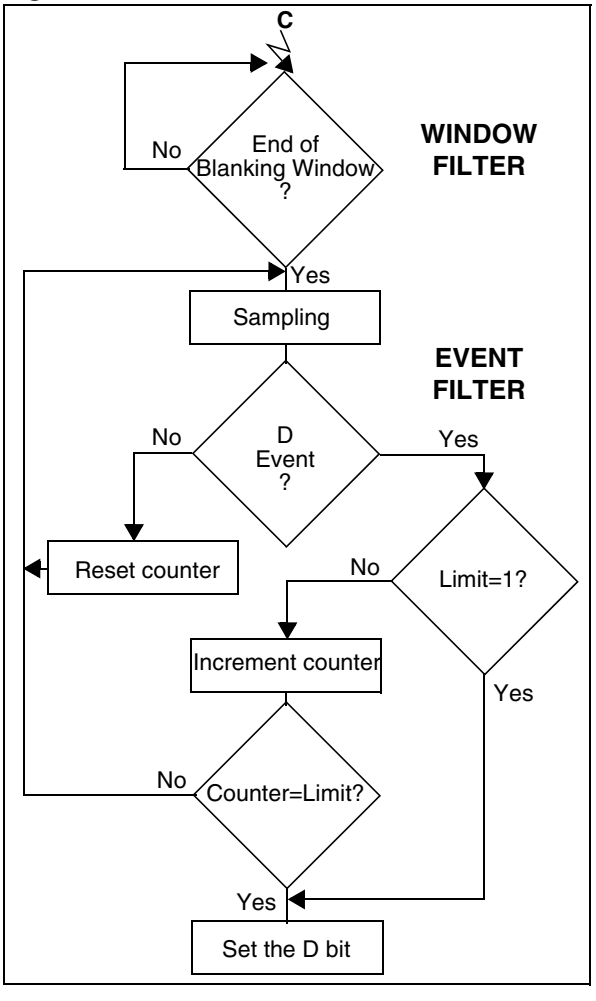
This Window Filter becomes active after both hardware and software C events.

The D Event Filter becomes active after the D Window Filter. It counts the number of consecutive D events up to a limit defined by the DEF[3:0] bits in the MDFR register. The reset value is 1. The D bit is set when the counter limit is reached.

Sampling is done at a selectable frequency (f_{SCF}), see Table 82.

The D event filter is active only for a hardware D event (D_H). For a simulated (D_S) event, it is forced to 1.

Figure 79. D Window and Event Filter Flowchart



DWF3	DWF2	DWF1	DWF0	C to D window filter in Sensorless Mode (SR=0)	SR=1
0	0	0	0	5 µs	No Window Filter after C event
0	0	0	1	10 µs	
0	0	1	0	15 µs	
0	0	1	1	20 µs	
0	1	0	0	25 µs	
0	1	0	1	30 µs	
0	1	1	0	35 µs	
0	1	1	1	40 µs	
1	0	0	0	60 µs	
1	0	0	1	80 µs	
1	0	1	0	100 µs	
1	0	1	1	120 µs	
1	1	0	0	140 µs	
1	1	0	1	160 µs	
1	1	1	0	180 µs	
1	1	1	1	200 µs	

Note: Times are indicated for 4 MHz f_{PERIPH}

Table 27. D Event filter Setting

DEF3	DEF2	DEF1	DEF0	D event Limit	SR=1
0	0	0	0	1	No D Event Filter
0	0	0	1	2	
0	0	1	0	3	
0	0	1	1	4	
0	1	0	0	5	
0	1	0	1	6	
0	1	1	0	7	
0	1	1	1	8	
1	0	0	0	9	
1	0	0	1	10	
1	0	1	0	11	
1	0	1	1	12	
1	1	0	0	13	
1	1	0	1	14	
1	1	1	0	15	
1	1	1	1	16	

MOTOR CONTROLLER (Cont'd)

10.6.6.5 Demagnetization (D) Event

At the end of the demagnetization phase, current no longer goes through the free-wheeling diodes. The voltage on the non-excited winding terminal goes from one of the power rail voltages to the common star connection voltage plus the BEMF voltage. In some cases (if the BEMF voltage is positive and the free-wheeling diodes are at ground for example) this end of demagnetization can be seen as a voltage edge on the selected MCIx input and it is called a hardware demagnetization event D_H. See Table 30.

The D event filter can be used to select the number of consecutive D events needed to generate the D_H event.

If enabled by the HDM bit in the MCRB register, the current value of the MTIM timer is captured in register MDREG when this event occurs in order to be able to simulate the demagnetization phase for the next steps.

When enabled by the SDM bit in the MCRB register, demagnetization can also be simulated by comparing the MTIM timer with the MDREG register. This kind of demagnetization is called simulated demagnetization D_S.

If the HDM and SDM bits are both set, the first event that occurs, triggers a demagnetization event. For this to work correctly, a D_S event must not precede a D_H event because the latter could be detected as a Z event.

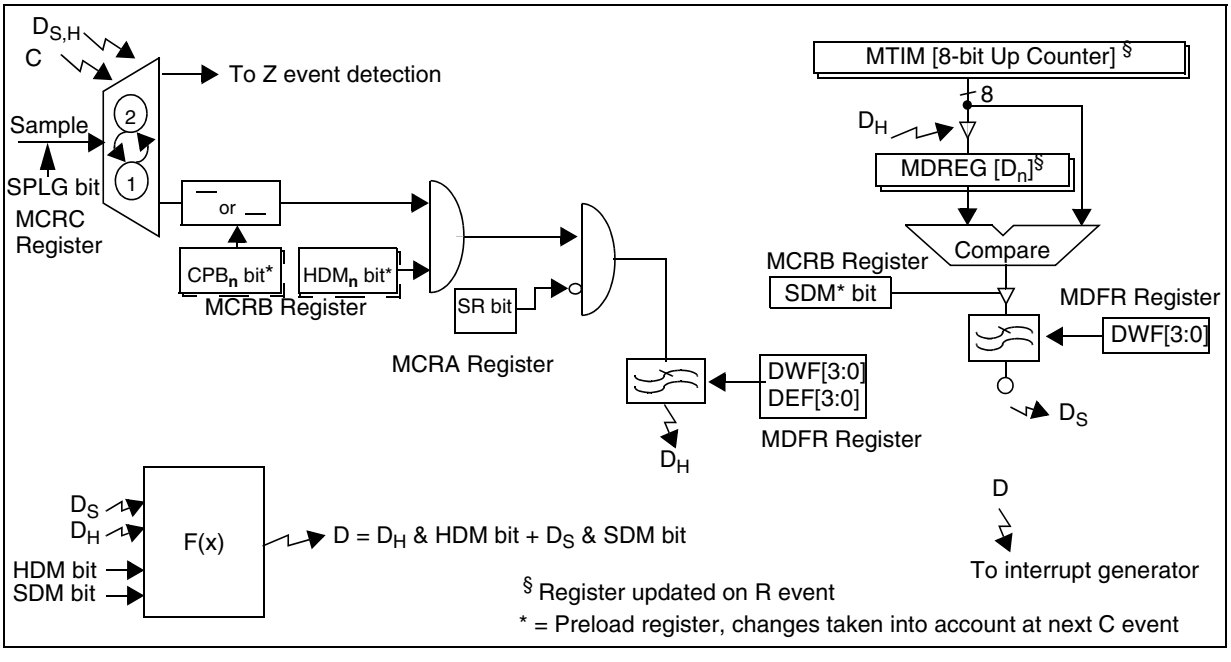
Simulated demagnetization can also be always used if the HDM bit is reset and the SDM bit is set. This mode works as a programmable masking time between the C_H and Z events. To drive the motor securely, the masking time must be always greater than the real demagnetization time in order to avoid a spurious Z event.

When an event occurs, (either D_H or D_S) the DI bit in the MISR register is set and an interrupt request is generated if the DIM bit of register MIMR is set.

Caution 1: Due to the alternate automatic capture and compare of the MTIM timer with MDREG register by D_H and D_S events, the MDREG register should be manipulated with special care.

Caution 2: Due to the event generation protection in the MZREG, MCOMP and MDREG registers for Soft Event generation (See "Built-in Checks and Controls for simulated events" on page 175.), the value written in the MDREG register in soft demagnetisation mode (SDM=1) is checked by hardware after the C event. If this value is less than or equal to the MTIM counter value at this moment, the Software demagnetisation event is generated immediately and the MTIM current value overwrites the value in the MDREG register to be able to reuse the right demagnetisation time for another simulated event generation.

Figure 81. D Event Generation Mechanism



MOTOR CONTROLLER (Cont'd)

10.6.6.13 Encoder Mode (IS[1:0] = 11)

Figure 90 shows the signals delivered by a standard digital incremental encoder and associated information:

- Two 90° phased square signals with variable frequency proportional to the speed; they must be connected to MCIA and MCIB input pins,
- Clock derived from incoming signal edges,
- Direction information determined by the relative phase shift of input signals (+ or -90°).

The Incremental Encoder Interface block aims at extracting these signals. As input logic is both rising and falling edge sensitive (independently from TES[1:0] bits setting), resulting clock frequency is four times the one of the input signals, thus increasing resolution for measurements.

It may be noticed that Direction bit (EDIR bit in MCRC register) is read only and that it does'nt affect counting direction of clocked timer (cf Section). As a result, one cannot extract position information from encoder inputs during speed reversal.

Figure 89. Tacho Capture events configured by the TES[1:0] bits

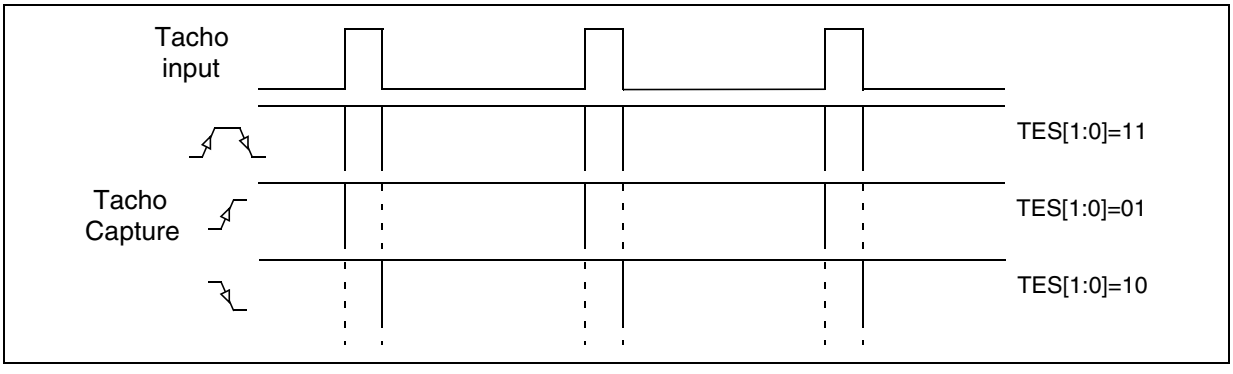
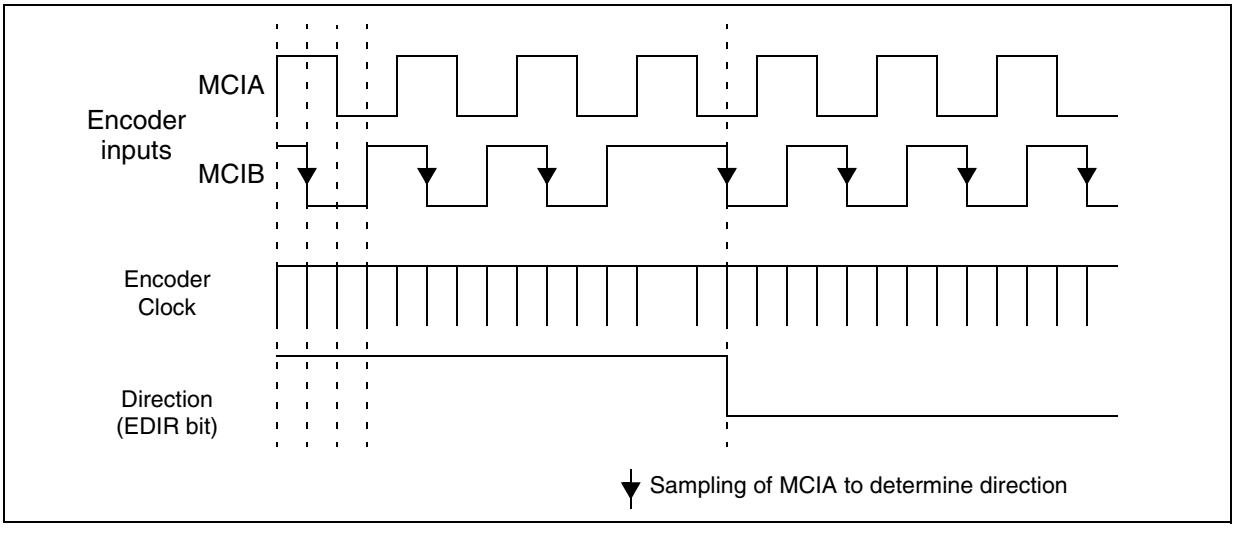
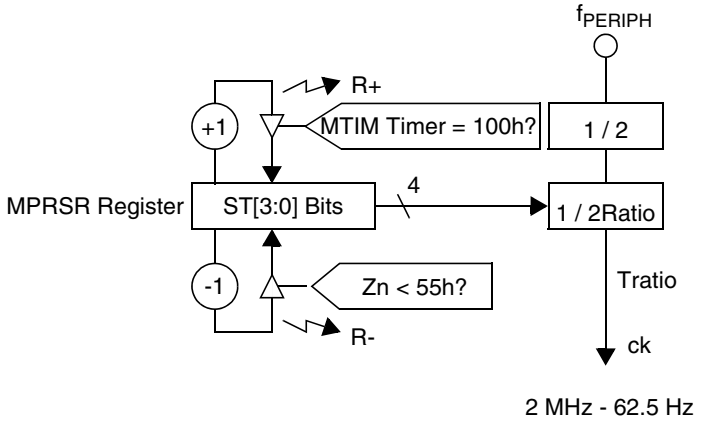


Figure 90. Incremental Encoder output signals and derived information

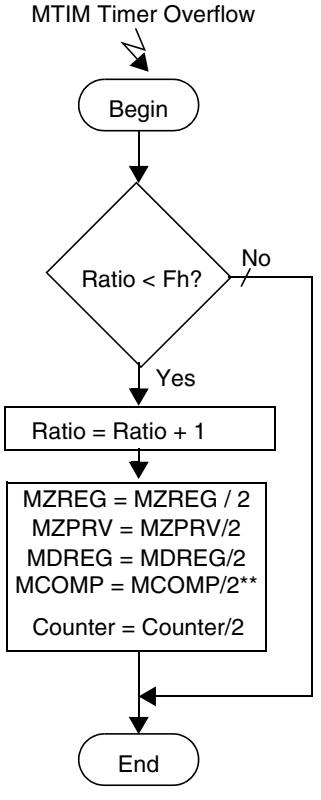


MOTOR CONTROLLER (Cont'd)

Figure 92. Step Ratio Functional Diagram

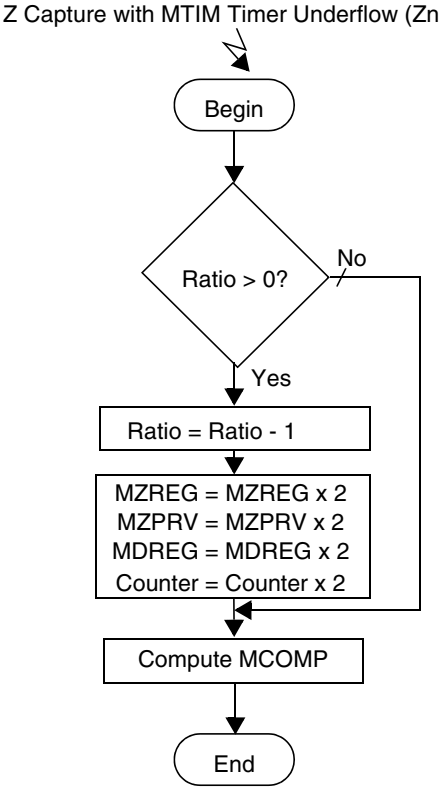


MTIM Timer control over T_{ratio} and register operation



Slow-down control

** Only in Auto-switched mode (SWA=1 in MCRA register)



Speed-up control

MOTOR CONTROLLER (Cont'd)

10.6.7.2 Autoswitched Mode

In this mode, using the hardware commutation event C_H (SC bit reset in MCRC register), the MCOMP register content is automatically computed in real-time as described below and in Figure 93.

The C (either C_S or C_H) event has no effect on the contents of the MTIM timer.

When a Z_H event occurs the MTIM timer value is captured in the MZREG register, the previous captured value is shifted into the MZPRV register and the MTIM timer is reset. See Figure 73.

When a Z_S event occurs, the value written in the MZREG register is shifted into the MZPRV register and the MTIM timer is reset.

One of these two registers, (when the SC bit = 0 in the MCRC register and depending on the DCB bit in the MCRA register), is multiplied with the contents of the MWGHT register and divided by 256. The result is loaded in the MCOMP compare register, which automatically triggers the next hardware commutation (C_H event).

Note: The result of the 8*8 bit multiplication, once written in the MCOMP register is compared with the current MTIM value to check that the MCOMP value is not already less than the MTIM value due to the multiplication time. If MCOMP<=MTIM, a C_H event is generated immediately and the MCOMP value is overwritten by the MTIM value.

Table 39. Multiplier Result

DCB bit	Commutation Delay
0	MCOMP = MWGHT x MZPRV / 256
1	MCOMP = MWGHT x MZREG / 256

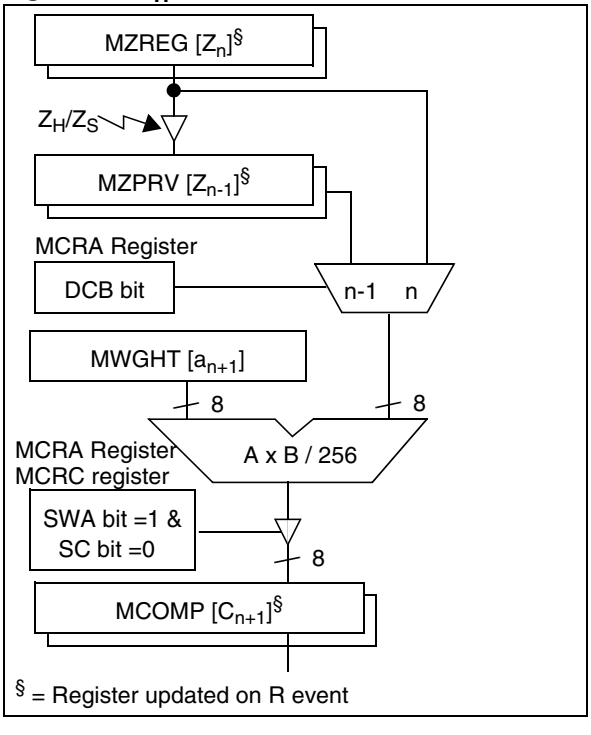
After each shift operation the multiply is recomputed for greater precision.

Using either the MZREG or MZPRV register depends on the motor symmetry and type.

The MWGHT register gives directly the phase shift between the motor driven voltage and the BEMF. This parameter generally depends on the motor and on the speed.

Setting the SC bit in the MCRC register enables the simulated commutation event (C_S) generation. This means that a write access is possible to the MCOMP register and the MTIM value will be compared directly with the value written by software in the MCOMP register to generate the C_S event. The comparison is enabled as soon as a write access is done to the MCOMP register. This means that if the SC bit is set and no write access is done to the MCOMP register, the C event will never occur because no comparison will be done between MCOMP and MTIM. Therefore, it is recommended in autoswitched mode, when using software commutation feature (SC bit is set) and for a normal event sequence, the corresponding value to be put in MCOMP has to be written during the Z interrupt routine (because MTIM has just been reset), so that there is no spurious comparison. If the SC bit is set during a Z event interrupt, then , the result of the 8*8 bits hardware multiplication can be overwritten by software in the MCOMP register. When simulated commutation mode is enabled, the event sequence is no longer respected, meaning that the peripheral will accept consecutive commutation events and not necessarily wait for a D event after a C_s event. In this case the MCOMP register can be written immediately after the previous C event, in the C interrupt service routine for example.

Figure 93. C_H Processor Block



Note 1: An overflow of the MTIM timer generates an RPI interrupt if the RIM bit is set.

Note 2: When simulated commutation mode is enabled, the D and Z event are not ignored by the peripheral, this means that if a Z event happens, the MTIM 8 bit internal counter will be reset.

Note 3: To generate consecutive simulated commutations (C_S), the successive value has to be written in the MCOMP register only after a C event

MOTOR CONTROLLER (Cont'd)

10.6.8.5 Current feedback amplifier

In both current and voltage mode, the current feedback from the motor can be amplified before entering the comparator. This is done by an integrated Op-amp that can be used when the OAON bit is set in the OACSR register and the CFAV bit in the MREF register is reset. This allows the three points of the Op-amp to be accessed for a programmable gain. The CFAV bit in the MREF register selects the MCCFI0 or OAZ(MCCFI1) pin as the comparator input as shown in the following table.

Table 46. Comparator input selection

CFAV bit	Meaning
0	Select OAZ(MCCFI1) as the current comparator input
1	Select MCCFI0 as the current comparator input

If the amplifier is not used for current feedback, it can be used for other purposes. In this case, the OAON bit in the OACSR register and the CFAV bit in the MREF register both have to be set. This means that the current feedback has to be on the MCCFI0 pin to be directly connected to the comparator and the OAP, OAN and OAZ (MCCFI1) pins can be used to amplify another signal. Both the OAZ(MCCFI1) and MCCFI0 pins can be connected to an ADC entry. See (Figure 106).

Note: The MCCFI0 pin is not available in LQFP32; SDIP32 and LQFP44 devices. In this case, the CFAV bit must be reset. The choice to use the Op-amp or not is made with the OAON bit.

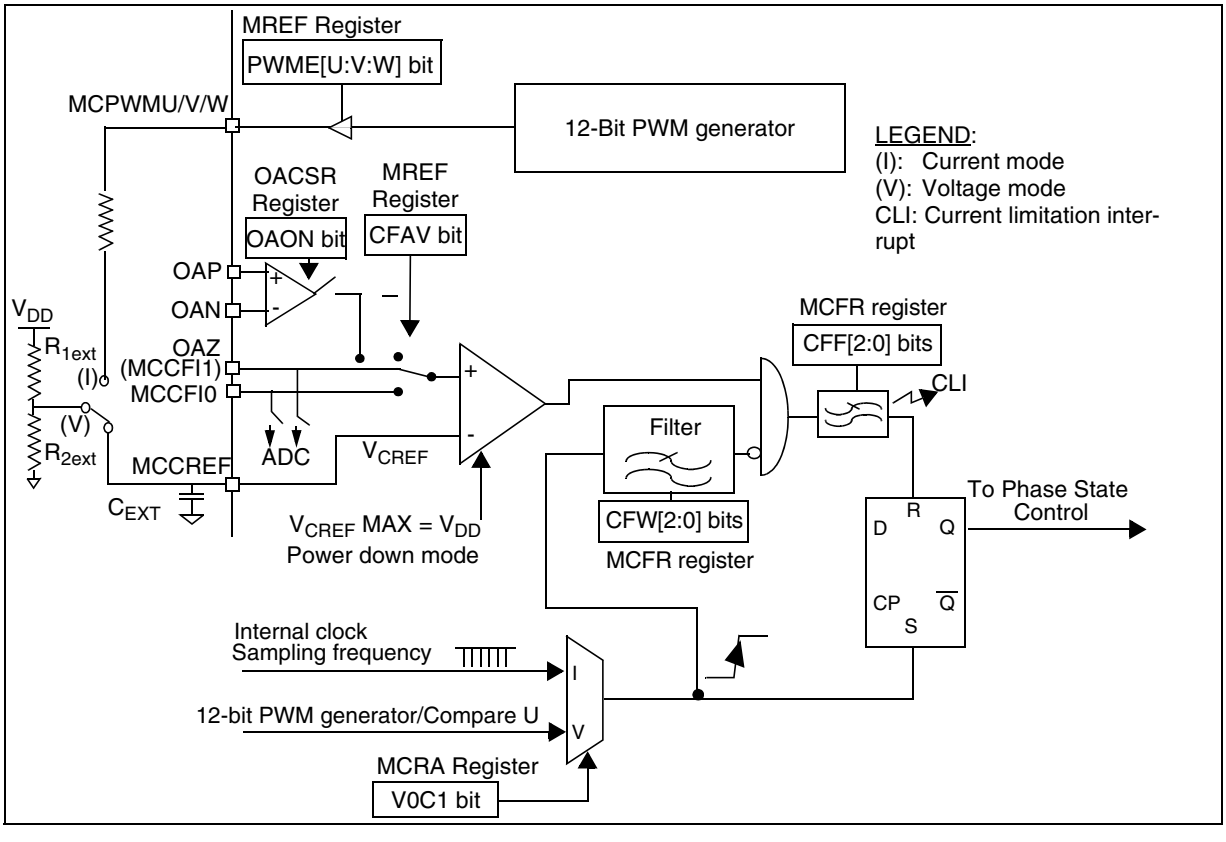
10.6.8.6 Measurement Window

In current mode, the measurement window frequency can be programmed between 390Hz and 50KHz by the means of the SA[3:0] bits in the MPRSR register.

Note: These frequencies are given for a 4 MHz peripheral input frequency for a BLDC drive (XT16, XT8 bits in MCONF register).

In sensorless mode this measurement window can be used to detect BEMF zero crossing events. Its width can be defined between 2.5µs and 40µs as a minimum in sensorless mode by the OT[3:0] bits in the MPWME register.

Figure 106. Current Feedback



MOTOR CONTROLLER (Cont'd)

MOTOR Z EVENT FILTER REGISTER (MZFR)
Read/Write
Reset Value: 0000 1111 (0Fh)

7	6	5	4	3	2	1	0
ZEF3	ZEF2	ZEF1	ZEF0	ZWF3	ZWF2	ZWF1	ZWF0

Bits 7:4 = **ZEF[3:0]**: *Z Event Filter bits*
These bits select the number of valid consecutive Z events (when the Z event is detected) needed to generate the active event. Sampling is done at the selected f_{SCF} frequency (see Table 82.) or at PWM frequency.

Table 80. Z Event filter Setting

ZEF3	ZEF2	ZEF1	ZEF0	Z event Samples
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

Bits 3:0 = **ZWF[3:0]**: *Z Window Filter bits*
These bits select the length of the blanking window activated at each D event. The filter blanks the Z event detection until the end of the time window.

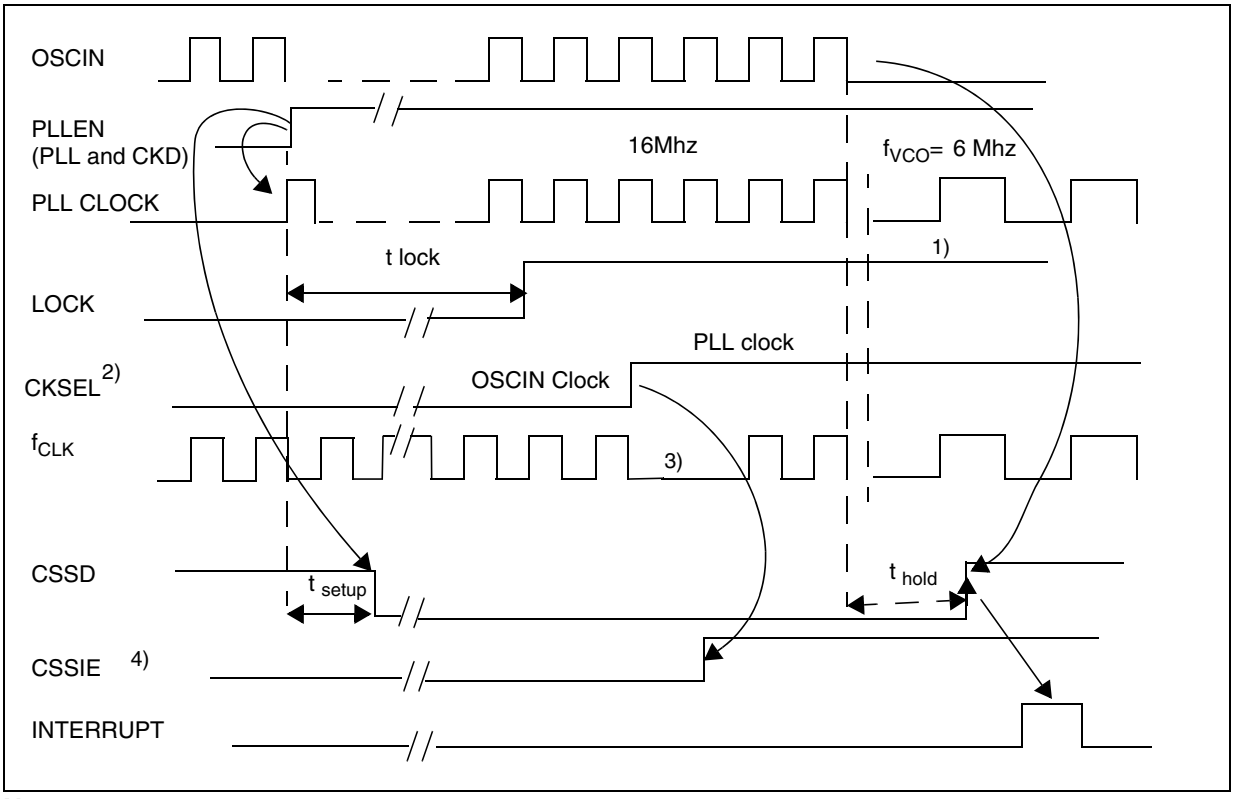
Table 81. Z Window filter Setting

ZWF3	ZWF2	ZWF1	ZWF0	D to Z window filter in Sensorless Mode (SR=0)	SR=1
0	0	0	0	5 µs	No Window Filter after D event
0	0	0	1	10 µs	
0	0	1	0	15 µs	
0	0	1	1	20 µs	
0	1	0	0	25 µs	
0	1	0	1	30 µs	
0	1	1	0	35 µs	
0	1	1	1	40 µs	
1	0	0	0	60 µs	
1	0	0	1	80 µs	
1	0	1	0	100 µs	
1	0	1	1	120 µs	
1	1	0	0	140 µs	
1	1	0	1	160 µs	
1	1	1	0	180 µs	
1	1	1	1	200 µs	

Note: Times are indicated for 4 MHz f_{PERIPH}

CLOCK AND TIMING CHARACTERISTICS (Cont'd)

Figure 137. PLL And Clock Detector Signal Start Up Sequence



Notes:

1. Lock does not go low without resetting the PLLEN bit.

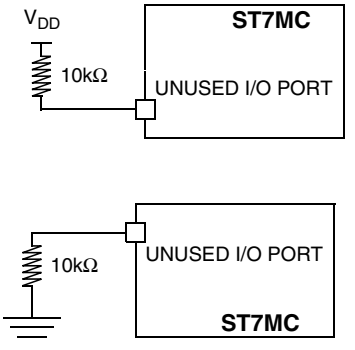
2. Before setting the CKSEL bit by software in order to switch to the PLL clock, a period of t_{lock} must have elapsed.

3. 2 clock cycles are missing after CKSEL = 1

4. CKSEL bit must be set before enabling the CSS interrupt (CSSIE=1).

I/O PORT PIN CHARACTERISTICS (Cont'd)

Figure 138. Two typical Applications with unused I/O Pin



Note: I/O can be left unconnected if it is configured as output (0 or 1) by the software. This has the advantage of greater EMC robustness and lower cost.

Figure 139. Typical I_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

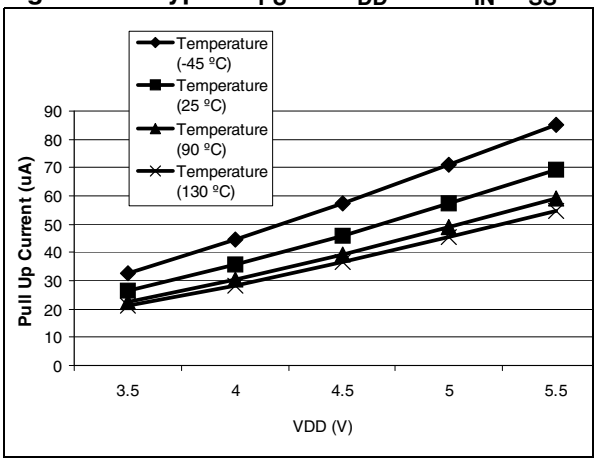
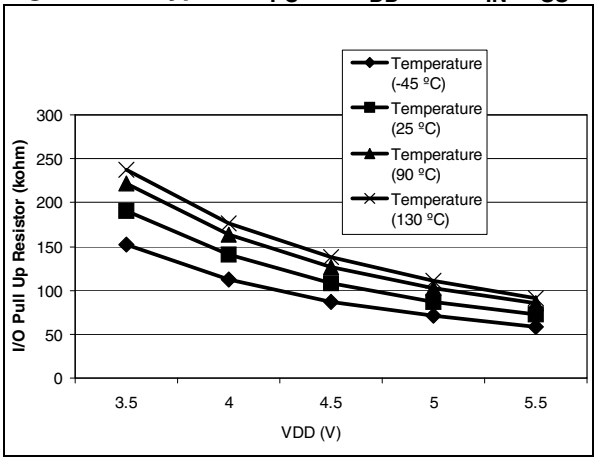


Figure 140. Typical R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$



12.9 CONTROL PIN CHARACTERISTICS

12.9.1 Asynchronous $\overline{\text{RESET}}$ Pin

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage					$0.3xV_{DD}$	V
V_{IH}	Input high level voltage			$0.7xV_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis [2]				1		V
V_{OL}	Output low level voltage [3]	V_{DD}=5V	I_{IO}=+5mA		0.5	1.2	V
			I_{IO}=+2mA		0.2	0.5	
I_{IO}	Driving current on $\overline{\text{RESET}}$ pin				2		mA
R_{ON}	Weak pull-up equivalent resistor	V_{IN}=V_{SS}, V_{DD}=5V		50	80	150	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration	Internal reset sources			30		µs
$t_{h(RSTL)in}$	External reset pulse hold time [4]			2.5			µs
$t_{g(RSTL)in}$	Filtered glitch duration [5]				450		ns

Notes:

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 12.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
4. To guarantee the reset of the device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.
5. The reset network protects the device against parasitic resets.

MOTOR CONTROL CHARACTERISTICS (Cont'd)

Figure 150. Example 1: Waveforms for Zero-crossing Detection with Sampling at the end of PWM off-time

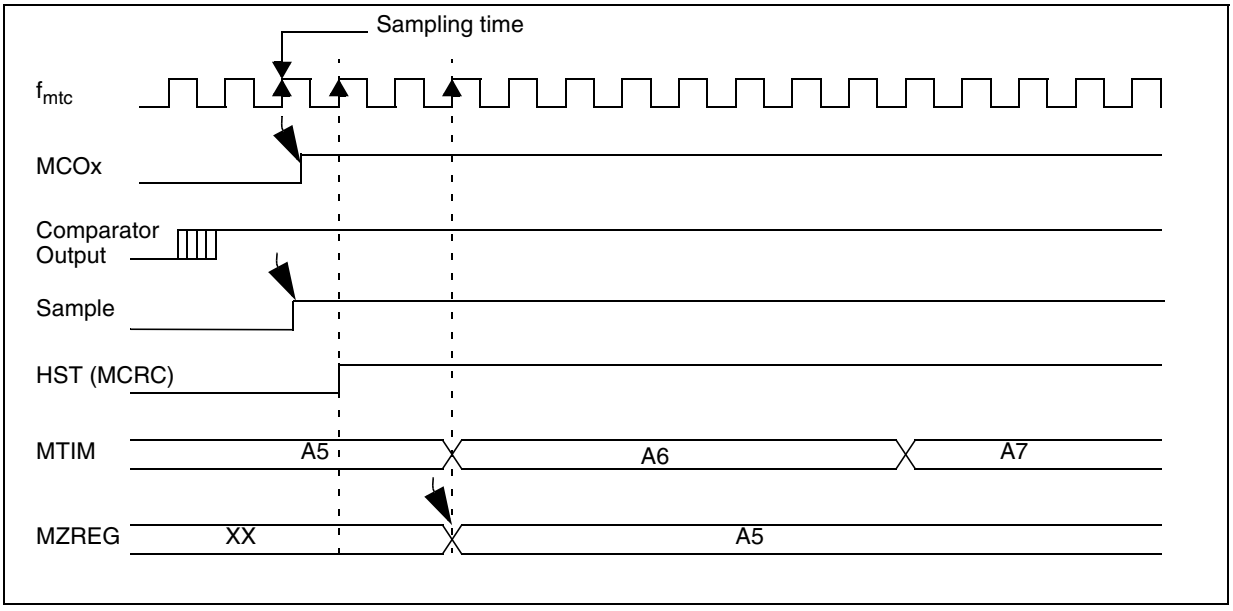
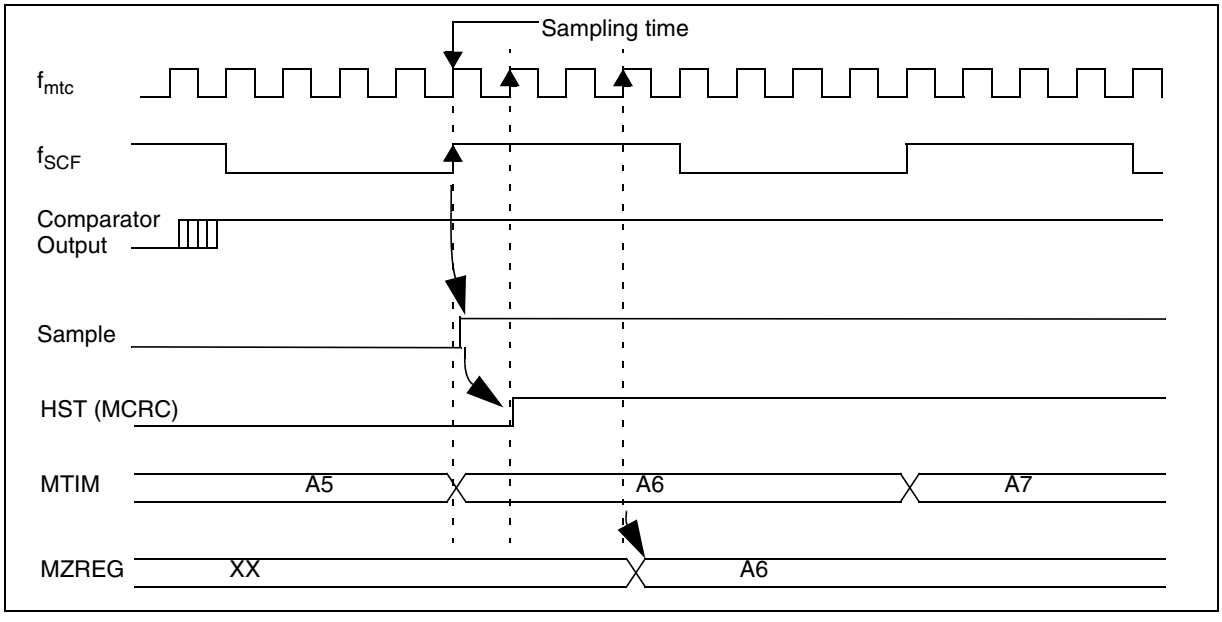


Figure 151. Example 2: Waveforms for Zero-crossing Detection with Sampling at f_{SCF}



PACKAGE CHARACTERISTICS (Cont'd)

13.2 THERMAL CHARACTERISTICS

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient) LQFP80 14x14 LQFP64 14x14 LQFP44 10x10 LQFP32 7x7 SDIP32 400mil SDIP56 600mil	 55 55 68 80 63 45	°C/W
T_{Jmax}	Maximum junction temperature[1)]	150	°C
P_{Dmax}	Power dissipation [2)]	500	mW

Notes:

1. The maximum chip-junction temperature is based on technology characteristics.

2. The maximum power dissipation is obtained from the formula $P_D = (T_J - T_A) / R_{thJA}$.

The power dissipation of an application can be defined by the user with the formula: $P_D=P_{INT}+P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD} \times V_{DD}$) and P_{PORT} is the port power dissipation depending on the ports used in the application.

Table 95. Revision History

Date	Revision	Description of Changes
Mar-06	9	Added two sales types: ST7FMC2S4T3 and ST7FMC2S6T3 Changed QFP package name: TQFP replaced by LQFP Changed "Master Mode Operation" on page 98: added important note Changed "Interrupt Mapping" on page 43: modified interrupt n°13 Added note to V_{DD} in Figure 13. on page 27 Modified Figure 24. on page 45. Changed section 7.7 on page 46 (IPB, IS3[1:0] and IPA descriptions) Changed Table 36 on page 166 and added notes Changed SWA bit description after Table 58 on page 210 Added note to section 12.3.3 on page 250 Changed R_{ON} max values in section 12.9.1 on page 266 Added Figure 154. on page 276 Changed notes to "THERMAL CHARACTERISTICS" on page 288 Added text on ECOPACK packages in Section 13 PACKAGE CHARACTERISTICS and changed Section 13.3 SOLDERING INFORMATION Added "EXTERNAL INTERRUPT MISSED" on page 303 Added Section 15.7 MAXIMUM VALUES OF AVD THRESHOLDS
19-June-06	10	Modified MCES description in Section 7.2 on page 41 Modified name of bit 5 in the SPICSR register in Table 19 on page 106 Modifed section 10.4.3.3 on page 99 (added title "how to operate the SPI in Master mode) Modified table in section 12.7.1 on page 261 Modified section 12.11.1 on page 271 ($t_{su(\overline{SS})}$, $t_{v(MO)}$ and $t_{h(MO)}$) and added note1 to $t_{su(\overline{SS})}$ and $t_{h(\overline{SS})}$ Removed EMC protection circuitry in Figure 145 on page 268 (device works correctly without these components) Modified description of DIV2 bit in section 14.1 on page 290 Changed Table 91 on page 293: removed ST7MC1K2B6 and ST7PMC1K2B6 (SDIP32 package) Modified "ST7MC MICROCONTROLLER OPTION LIST" on page 293 Added revision history for revisions 6 and 7
08-Dec-06	11	Added caution to section 6.2.1 on page 30 Modified Figure 149 on page 272 ($t_{v(MO)}$, $t_{h(MO)}$) Replaced CPHA=0 with CPHA=1 in Figure 148. on page 272 Modified section 14.3 on page 294 Added one sales type (ST7FMC2S7T6) and modified Table 91 on page 293
25-Sep-08	12	Title of the document changed. Modified Table 1, "Device summary," on page 1 Removed SDIP32 package and part numbers for automotive products Removed reference to ST7MC1K6 Added footnote to Table 1, "ST7MC Device Pin Description," on page 12 indicating that it is mandatory to connect all available V_{DD} and V_{DDA} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground. Values in inches rounded to 4 decimal digits (instead of 3 decimal digits) in Section 13.1 PACKAGE MECHANICAL DATA. "Output Compare" on page 82: Changed text of note 3 and removed compare register i latch signal from Figure 52. "Output Compare Timing Diagram, fTIMER =fCPU/4" page 84. Modified t_{RET} values in Section 12.6.2 FLASH Memory Modified Section 12.7.3 Absolute Maximum Ratings (Electrical Sensitivity). Added "TIMD SET SIMULTANEOUSLY WITH OC INTERRUPT" on page 300. Modified section 14.2 on page 292. (Figure 167 on page 292 and "ST7MC MICROCONTROLLER OPTION LIST" on page 293)
02-Apr-09	13	$V_{ESD(MM)}$ removed in section 12.2.1 on page 248 and section 12.7.3 on page 263 Modified GPB values (and conditions) in section 12.13 on page 280 Modified ECOPACK text in section 13 on page 285