WINDOW WATCHDOG (Cont'd)

Figure 36. Exact Timeout Duration (t_{min} and t_{max})

WHERE:

$t_{min0} = (LSB + 128) \times 64 \times t_{OSC2}$

$t_{max0} = 16384 \times t_{OSC2}$

$t_{OSC2} = 125ns$ if $f_{OSC2} = 8$ MHz

CNT = Value of T[5:0] bits in the WDGCR register (6 bits)

MSB and LSB are values from the table below depending on the timebase selected by the TB[1:0] bits in the MCCSR register

TB1 Bit (MCCSR Reg.)	TB0 Bit (MCCSR Reg.)	Selected MCCSR Timebase	MSB	LSB
0	0	2ms	4	59
0	1	4ms	8	53
1	0	10ms	20	35
1	1	25ms	49	54

To calculate the minimum Watchdog Timeout (t_{min}):

$$\text{IF } CNT < \left[\frac{MSB}{4}\right] \quad \text{THEN } t_{min} = t_{min0} + 16384 \times CNT \times t_{osc2}$$

$$\text{ELSE } t_{min} = t_{min0} + \left[16384 \times CNT - \left[\frac{4CNT}{MSB}\right] + (192 + LSB) \times 64 \times \left[\frac{4CNT}{MSB}\right]\right] \times t_{osc2}$$

To calculate the maximum Watchdog Timeout (t_{max}):

$$\text{IF } CNT \left[\frac{MSB}{4}\right] \quad \text{THEN } t_{max} = t_{max0} + 16384 \times CNT \times t_{osc2}$$

$$\text{ELSE } t_{max} = t_{max0} + \left[16384 \times CNT - \left[\frac{4CNT}{MSB}\right] + (192 + LSB) \times 64 \times \left[\frac{4CNT}{MSB}\right]\right] \times t_{osc2}$$

Note: In the above formulae, division results must be rounded down to the next integer value.

Example:

With 2ms timeout selected in MCCSR register

Value of T[5:0] Bits in WDGCR Register (Hex.)	Min. Watchdog Timeout (ms) t_{min}	Max. Watchdog Timeout (ms) t_{max}
00	1.496	2.048
3F	128	128.552

16-BIT TIMER (Cont'd)

Figure 45. Counter Timing Diagram, internal clock divided by 2

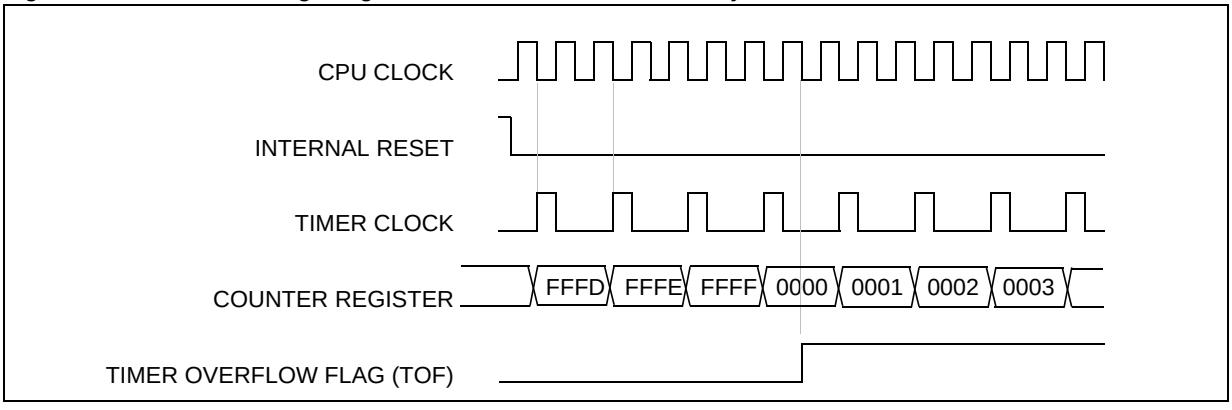


Figure 46. Counter Timing Diagram, internal clock divided by 4

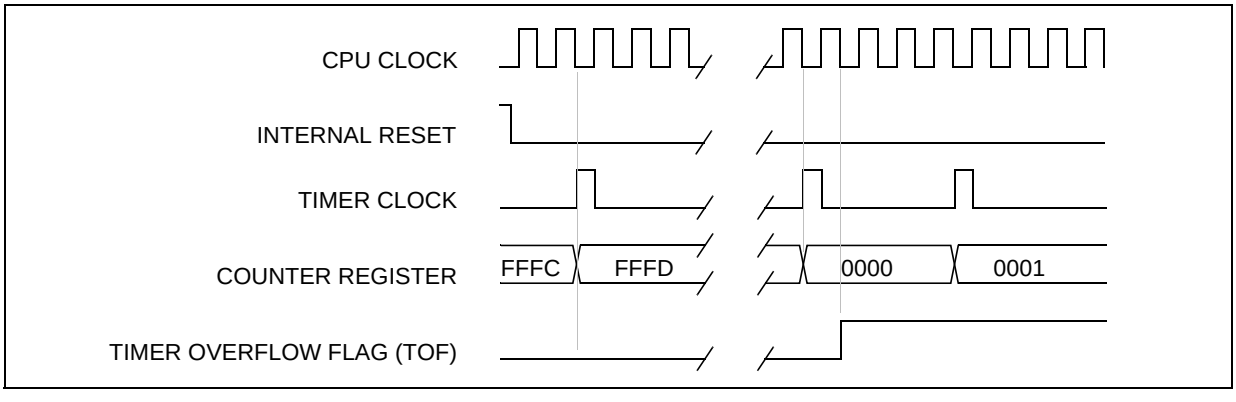
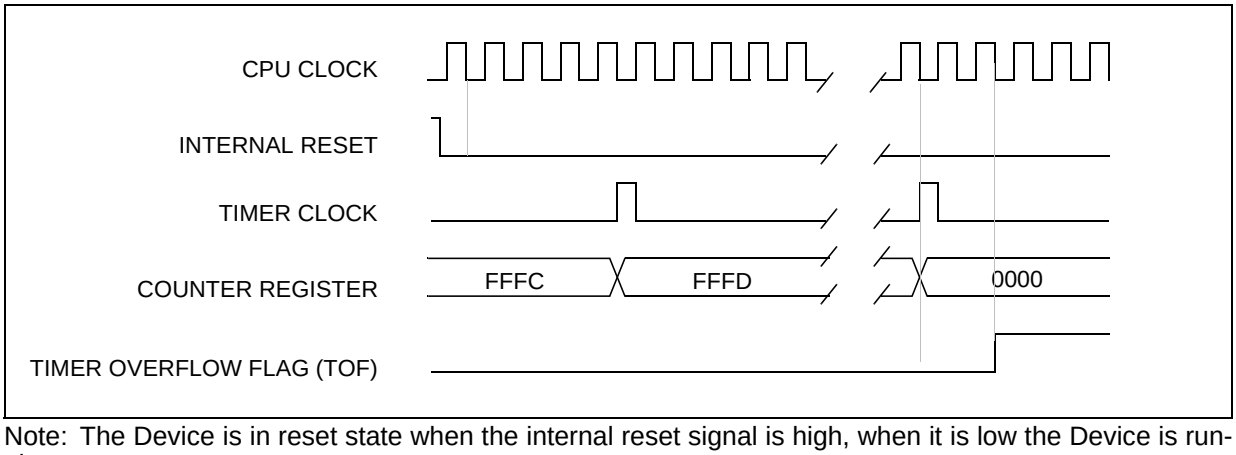
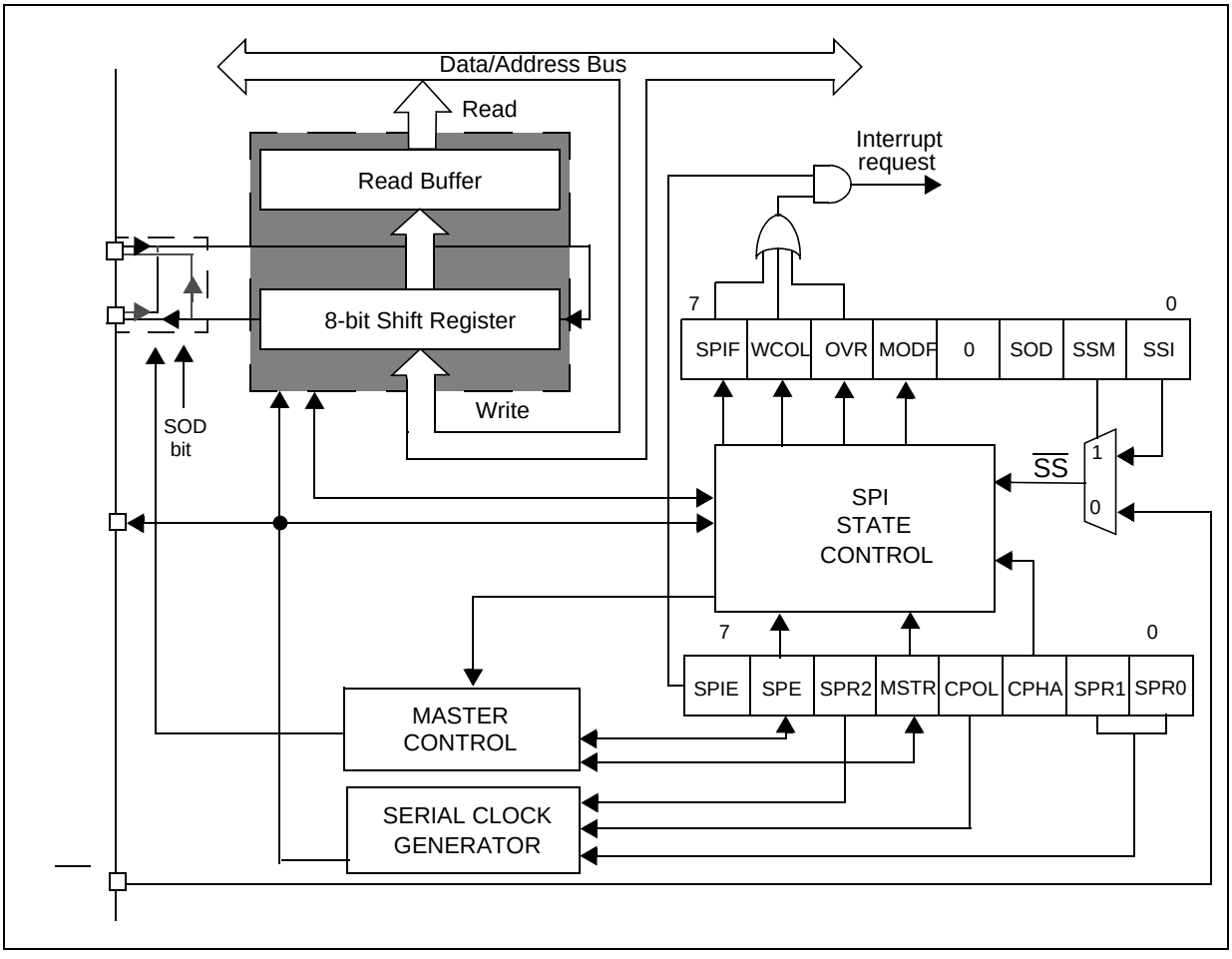


Figure 47. Counter Timing Diagram, internal clock divided by 8



Note: The Device is in reset state when the internal reset signal is high, when it is low the Device is running.

(cont'd)


Data/Address Bus
Read
Read Buffer
8-bit Shift Register
Write
SOD
bit
Interrupt
request
7
0
SPIF
WCOL
OVR
MODF
0
SOD
SSM
SSI
SS
1
0
SPI
STATE
CONTROL
7
0
SPIE
SPE
SPR2
MSTR
CPOL
CPHA
SPR1
SPR0
MASTER
CONTROL
SERIAL CLOCK
GENERATOR

(cont'd)

A basic example of interconnections between a single master and a single slave is illustrated in Figure 56.

The MOSI pins are connected together and the MISO pins are connected together. In this way data is transferred serially between master and slave (most significant bit first).

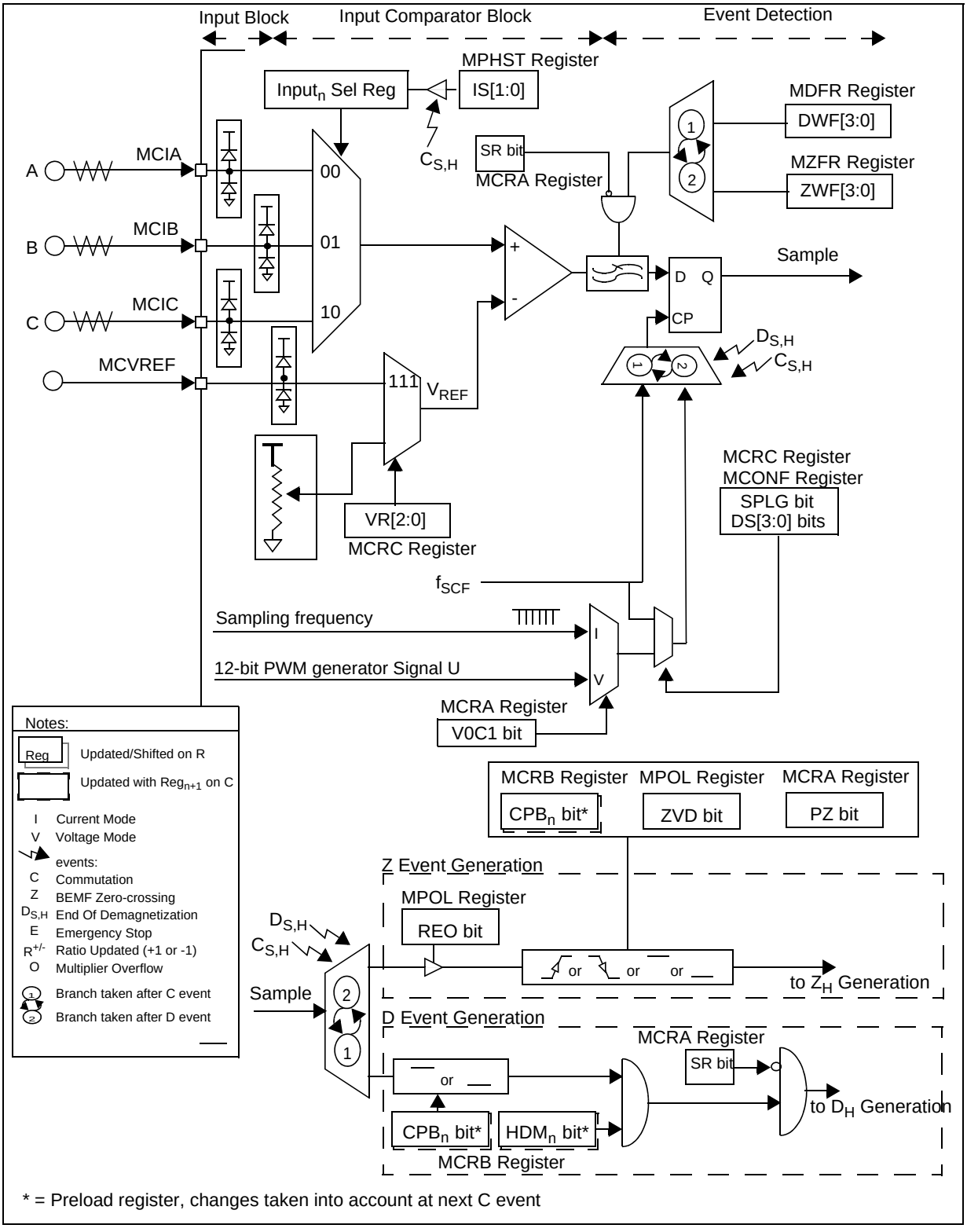
The communication is always initiated by the master. When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex communication with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

To use a single data line, the MISO and MOSI pins must be connected at each node (in this case only simplex communication is possible).

Four possible data/clock timing relationships may be chosen (see Figure 59 on page 100) but master and slave must be programmed with the same timing mode.

MOTOR CONTROLLER (Cont'd)

Figure 78. Input Stage in Sensorless or Sensor Mode (bits TES[1:0] = 00)



MOTOR CONTROLLER (Cont'd)

10.6.6.4 Z Event Detection

In sensorless mode, the Z window filter becomes active after each D event. It blanks out the Z event during the time window defined by the ZWF[3:0] bits in the MZFR register (see Table 28). The reset value is 200µs. This Window Filter becomes active after both hardware and software D events.

The Z Event Filter becomes active after the Z Window Filter. It counts the number of consecutive Z events up to a limit defined by the ZEF[3:0] bits in the MZFR register. The reset value is 1. The Z bit is set when the counter limit is reached.

Sampling is done at a selectable frequency (f_{SCF}), see Table 82.

The Z event filter is active only for a hardware Z event (Z_H). For a simulated (Z_S) event, it is forced to 1. Z event filter is also active in sensor mode.

Figure 80. Z Window and Ev ent Filter Flowchart

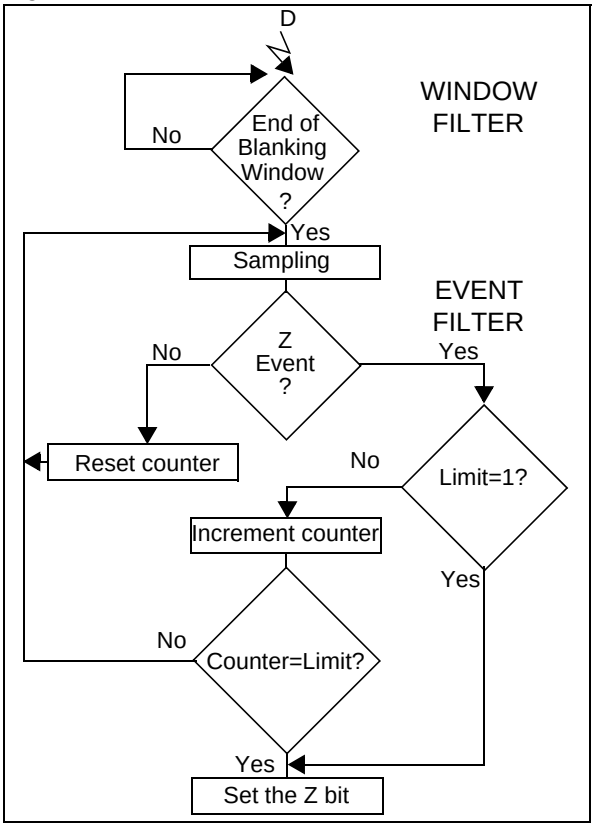


Table 28. Z Window filter Setting

ZWF3	ZWF2	ZWF1	ZWF0	D to Z window filter in Sensorless Mode (SR=0)	SR=1
0	0	0	0	5 µs	No Window Filter after D event
0	0	0	1	10 µs	
0	0	1	0	15 µs	
0	0	1	1	20 µs	
0	1	0	0	25 µs	
0	1	0	1	30 µs	
0	1	1	0	35 µs	
0	1	1	1	40 µs	
1	0	0	0	60 µs	
1	0	0	1	80 µs	
1	0	1	0	100 µs	
1	0	1	1	120 µs	
1	1	0	0	140 µs	
1	1	0	1	160 µs	
1	1	1	0	180 µs	
1	1	1	1	200 µs	

Note: Times are indicated for 4 MHz f_{PERIPH}

Table 29. Z Event filter Setting

ZEF3	ZEF2	ZEF1	ZEF0	Z event Limit
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

INSTRUCTION SET OVERVIEW (Cont'd)

11.1.1 Inherent

All Inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Inherent Instruction	Function
NOP	No operation
TRAP	S/W Interrupt
WFI	Wait For Interrupt (Low Power Mode)
HALT	Halt Oscillator (Lowest Power Mode)
RET	Sub-routine Return
IRET	Interrupt Sub-routine Return
SIM	Set Interrupt Mask (level 3)
RIM	Reset Interrupt Mask (level 0)
SCF	Set Carry Flag
RCF	Reset Carry Flag
RSP	Reset Stack Pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
MUL	Byte Multiplication
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles

11.1.2 Immediate

Immediate instructions have two bytes, the first byte contains the opcode, the second byte contains the operand value.

Immediate Instruction	Function
LD	Load
CP	Compare
BCP	Bit Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Operations

11.1.3 Direct

In Direct instructions, the operands are referenced by their memory address.

The direct addressing mode consists of two submodes:

Direct (short)

The address is a byte, thus requires only one byte after the opcode, but only allows 00 - FF addressing space.

Direct (long)

The address is a word, thus allowing 64 Kbyte addressing space, but requires 2 bytes after the opcode.

11.1.4 Indexed (No Offset, Short, Long)

In this mode, the operand is referenced by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset.

The indirect addressing mode consists of three sub-modes:

Indexed (No Offset)

There is no offset, (no extra byte after the opcode), and allows 00 - FF addressing space.

Indexed (Short)

The offset is a byte, thus requires only one byte after the opcode and allows 00 - 1FE addressing space.

Indexed (long)

The offset is a word, thus allowing 64 Kbyte addressing space and requires 2 bytes after the opcode.

11.1.5 Indirect (Short, Long)

The required data byte to do the operation is found by its memory address, located in memory (pointer).

The pointer address follows the opcode. The indirect addressing mode consists of two sub-modes:

Indirect (short)

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - FF addressing space, and requires 1 byte after the opcode.

Indirect (long)

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

ABSOLUTE MAXIMUM RATINGS (Cont'd)

12.2.3 Thermal Characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see Section 13.2 THERMAL CHARACTERISTICS)		

SUPPLY CURRENT CHARACTERISTICS (Cont'd)

12.4.3 Halt and Active-halt modes

Symbol	Parameter	Conditions		Typ	Max	Unit
I_{DD}	Supply current in Halt mode [1]	V_{DD}=5.5V	-40°C T_A +85°C	1	10	µA
			-40°C T_A +125°C		50	
	Supply current in Active-halt mode [2]	16Mhz external clock		1	1.5	mA

1. All I/O pins in push-pull output mode (when applicable) with a static value at V_{DD} or V_{SS} (no load), PLL and LVD disabled. Data based on characterization results, tested in production at V_{DD} max. and f_{CPU} max.

2. All I/O pins in input mode with a static value at V_{DD} or V_{SS}. Tested in production at V_{DD} max and f_{cpu} max with clock input OSC1 driven by an external square wave; V_{DD} applied on OSC2 to reduce oscillator consumption. Consumption may be slightly different with a quartz or resonator.

12.4.4 Supply and Clock Managers

The previous current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added (except for Halt mode).

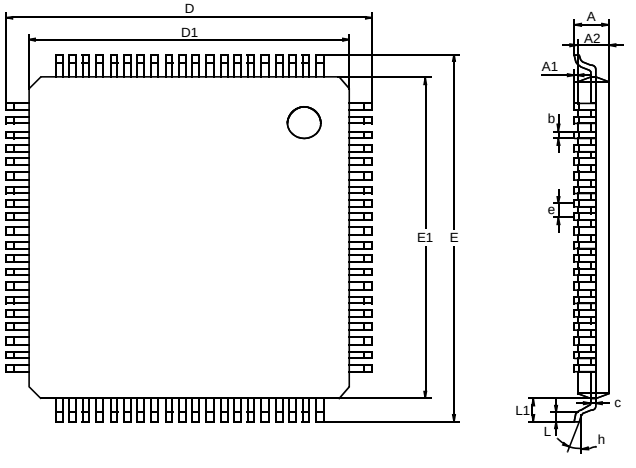
Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(LVD)}$	LVD supply current	Halt mode	180	280	µA
$I_{DD(PLL)}$	PLL supply current	V_{DD} = 5V	700		

13 PACKAGE CHARACTERISTICS

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

13.1 PACKAGE MECHANICAL DATA

Figure 162. 80-Pin Low Profile Quad Flat Package



Dim.	mm			inches [1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.22	0.32	0.38	0.0087	0.0126	0.0150
C	0.09		0.20	0.0035		0.0079
D		16.00			0.6299	
D1		14.00			0.5512	
E		16.00			0.6299	
E1		14.00			0.5512	
e		0.65			0.0256	
	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
	Number of Pins					
N	80					

ST7MC DEVICE CONFIGURATION AND ORDERING INFORMATION (Cont'd)

14.3 DEVELOPMENT TOOLS

Development tools for the ST7 microcontrollers include a complete range of hardware systems and software tools from STMicroelectronics and third-party tool suppliers. The range of tools includes solutions to help you evaluate microcontroller peripherals, develop and debug your application, and program your microcontrollers.

14.3.1 Starter kits

ST offers complete, affordable starter kits and full-featured that allow you to evaluate microcontroller features and quickly start developing ST7 applications. Starter kits are complete hardware/software tool packages that include features and samples to to help you quickly start developing your application.

14.3.2 Development and debugging tools

Application development for ST7 is supported by fully optimizing C Compilers and the ST7 Assembler-Linker toolchain, which are all seamlessly integrated in the ST7 integrated development environments in order to facilitate the debugging and fine-tuning of your application. The Cosmic C Compiler is available in a free version that outputs up to 16K of code.

The range of hardware tools includes full-featured ST7-EMU2B series emulators and the low-cost RLink in-circuit debugger/programmer. These tools are supported by the ST7 Toolset from STMicroelectronics, which includes the STVD7 integrated development environment (IDE) with high-level language debugger, editor, project manager and integrated programming interface.

14.3.3 Programming tools

During the development cycle, the ST7-EMU3 series emulators and the RLink provide in-circuit programming capability for programming the Flash microcontroller on your application board.

ST also provides a low-cost dedicated in-circuit programmer, the ST7-STICK, as well as ST7 Socket Boards which provide all the sockets required for programming any of the devices in a specific ST7 sub-family on a platform that can be used with any tool with in-circuit programming capability for ST7.

For production programming of ST7 devices, ST's third-party tool partners also provide a complete range of gang and automated programming solutions, which are ready to integrate into your production environment.

14.3.4 Order codes for ST7MC development tools

Table 91. Development tool order codes for the ST7MC family

MCU	Starter kit	Emulator	Programming tool
ST7MC1 ST7MC2	ST7MC-KIT/BLDC	ST7MDT50-EMU3	ST7-STICK[1)2)] STX-RLINK[3)]

1. Add suffix /EU, /UK or /US for the power supply for your region
2. Parallel port connection to PC
3. RLink with ST7 tool set

For additional ordering codes for spare parts and accessories, refer to the online product selector at www.st.com/mcu.