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### Understanding [Embedded - Microcontroller, Microprocessor, FPGA Modules](#)

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

### Applications of [Embedded - Microcontroller,](#)

#### Details

Product Status	Obsolete
Module/Board Type	FPGA Core
Core Processor	Artix-7 A35T
Co-Processor	-
Speed	-
Flash Size	16MB
RAM Size	-
Connector Type	Samtec LSHM
Size / Dimension	1.57" x 1.18" (40mm x 30mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	<a href="https://www.e-xfl.com/product-detail/trenz-electronic/te0714-02-35-2i">https://www.e-xfl.com/product-detail/trenz-electronic/te0714-02-35-2i</a>



## TE0714 TRM

**Revision:** V.27

**Date:** 07-Jun-2017 19:10

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## Overview

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Refer to <https://wiki.trenz-electronic.de/display/PD/TE0714+TRM> for the online version of this manual and the rest of available documentation.

The Trenz Electronic TE0714 is an industrial-grade SoM (System on Module) based on Xilinx Artix-7, 16 MByte Flash memory and powerful switching mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking strips. All modules in 4 x 5 cm form factor are mechanically compatible.

## Key Features

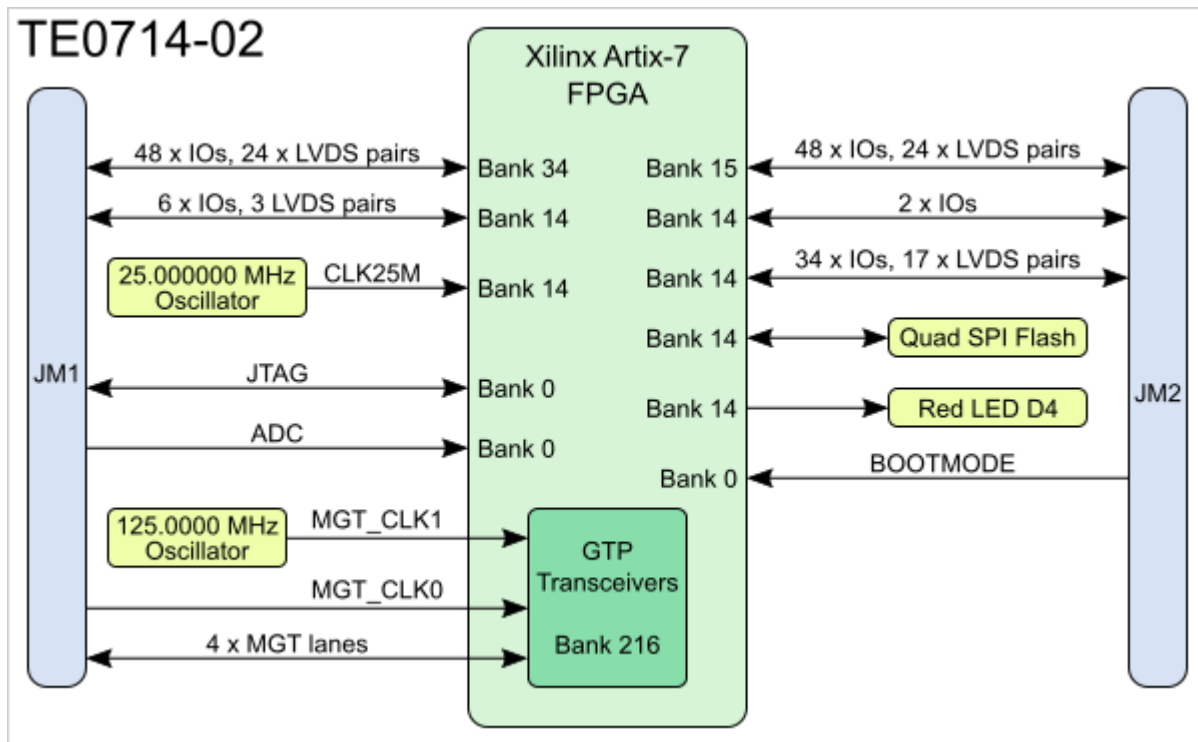
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- Xilinx Artix-7 FPGA (A15T, A35T, A50T)
- Rugged for shock and high vibration
- 16 MByte QSPI Flash memory
- Differential MEMS oscillator for MGT clocking
- MEMS oscillator for PL clocks (Optional)
- Plug-on module with 2 x 100-pin high-speed hermaphroditic strips
  - 144 FPGA I/O's (Max 68 differential)
  - XADC analog input
  - 4 GTP (high-performance transceiver) lanes
  - GT reference clock inputs
  - Optimized I/O and power pins for good signal integrity
- On-board high-efficiency DC-DC converters
- Power supply for all on-board components
- eFUSE bit-stream encryption (AES)
- One user configurable LED

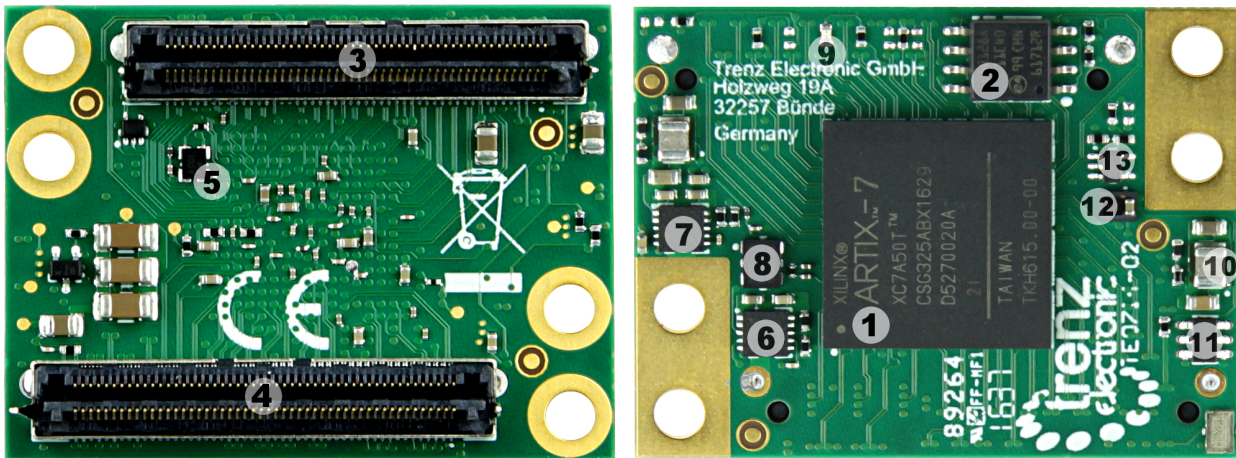
Different configurations for cost and performance optimization available upon request. Available options are:

- FPGA Type (A15T, A35T, A50T), temperature grade
- GT clock frequency (or none if not implemented)
- PL clock frequency and precision (or none if not implemented)
- Config and B14 bank Voltage: 1.8V or 3.3V
- SPI Flash type (or none if not implemented)
- LED Color (or none if not implemented)
- PUDC Pin strapping (pull high or pull down)
- GT power enable pin strapping (default power enabled or disabled)

## Block Diagram



## Main Components



1. Xilinx Artix-7 FPGA (XC7A series), U4
2. 16 MByte SPI Flash, U7
3. B2B connector Samtec Razor Beam™ LSHM-150, JM2
4. B2B connector Samtec Razor Beam™ LSHM-150, JM1
5. 25 MHz oscillator, U8
6. Single output low-dropout linear regulator (1.2V\_MGT) , U6
7. Single output low-dropout linear regulator (1.0V\_MGT) , U5
8. Low-jitter precision LVDS 125 MHz oscillator (GT Clock), U2
9. Red indication LED, D4
10. Step-down DC-DC converter (1.0V), U1
11. PFET load switch with configurable slew rate (3.3V), Q1
12. Low-power step-down DC-DC converter (1.8V), U3
13. Voltage detector for circuit initialization and timing supervision, U23

## Initial Delivery State

Storage device name	Content	Notes
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor
SPI Flash Quad Enable bit	Programmed	
SPI Flash main array	demo design	
eFUSE USER	Not programmed	
eFUSE Security	Not programmed	

## Signals, Interfaces and Pins

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### Board to Board (B2B) I/Os

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FPGA bank number and number of I/O signals connected to the B2B connector:

FPGA Bank	B2B Connector	I/O Signal Count	Voltage Level	Notes
14	JM1	6	VCCIO_0	
14	JM2	36	VCCIO_0	NB! 17 LVDS pairs possible.
15	JM2	48	VCCIO15	Supplied by the baseboard.
34	JM1	48	VCCIO34	Supplied by the baseboard.
216	JM1	16	MGT_AVCC MGT_AVTT	4 x GTP lanes.

Please refer to the [Pin-out](#) tables page for additional information.

### JTAG Interface

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JTAG access to the Xilinx Artix-7 FPGA device is provided through connector JM1.

Signal Name	B2B Pin
TCK	JM1:89
TDI	JM1:85
TDO	JM1:87
TMS	JM1:91

### On-board LED's

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There is one LED on TE0714 module:

LED	Color	FPGA	Notes
D4	Red	K18	

## Clocking

Clock	Default Frequency	IC	FPGA	Notes
CLK125MHz	25 MHz	U8	T14	Frequency depends on the module variant. Output is compatible to 3.3V and 1.8V I/O standard of the FPGA bank.
MGT_CLK	125MHz	U2	B6/B5	Frequency depends on the module variant




## Boot Process

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Boot mode is controlled by the MODE signal on the board to board (B2B) connector:

MODE signal State	Boot Mode
high or open	Master SPI, x4 Mode
low or ground	Slave SelectMAP

 SPI D2 and D3 have no pull-ups on the module so with PUDC=High option, those pins are floating if there are no pull-ups on baseboard. As those pins have SPI RESET function when Quad mode is not enabled, it is mandatory to either add pull-ups on user baseboard or program the Quad Enable bit in Flash nonvolatile status register.


## On-board Peripherals

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### 16 MByte Quad SPI Flash

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On-board SPI flash memory S25FL127S (U7) is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the bus width and clock frequency used.

 SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash. By default this bit is set to high at the manufacturing plant.

## Power and Power-On Sequence

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To power-up a module, power supply with minimum current capability of 1A is recommended.

### Power Supply

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TE0714 needs one single power supply with nominal of 3.3V.

### Power Consumption

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Test Condition (25 °C ambient)	VIN Current mA	Notes
TE0714-35, TEBT0714, empty design, GT not enabled	110mA	

Actual power consumption depends on the FPGA design and ambient temperature.

### Power-On Sequence

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There is no specific or special power-on sequence, single power source is needed as VIN, rest of the sequence is automatic.

### Bank Voltages

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Bank	Voltage	Notes
0 Config and B14	1.8V or 3.3V	Depends on module variant
15	User	Supplied from baseboard via B2B connector, max 3.3V
34	User	Supplied from baseboard via B2B connector, max 3.3V

## Board to Board Connectors

 Board to board connectors are hermaphroditic. Odd pin numbers are connected to even pin numbers on the mating connector and vice versa.

The Trenz Electronic modules use 100-pin REF-189016-02 and 60-pin REF-189017-02 connectors which are compatible with Samtec Razor Beam LSHM type connectors (see table below). When using the same type of connectors on baseboard, mating height will be 8mm. Other mating heights are possible by using connectors with a different height.

Baseboard Connector	Compatible Connector	Number of Pins	Mating height
REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	100 (2 x 50)	6.5 mm
LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	100 (2 x 50)	7.0 mm
REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	100 (2 x 50)	8.0 mm
LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	100 (2 x 50)	10.0mm
REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	60 (2 x 30)	6.5 mm
LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	60 (2 x 30)	7.0 mm
REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	60 (2 x 30)	8.0 mm
LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	60 (2 x 30)	10.0mm

Modules can be manufactured using different type of connectors upon request.

The LSHM connector speed rating depends on the stacking height:

Stacking Height	Speed Rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.9 GHz / 14 Gbps

## Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 3 hours 3 axis

## Manufacturer Documentation

Name	Version	Date
<a href="#">LSHM-1XX-XX.X-X-DV-A-X-X-TR-FOOTPRINT(1).pdf</a>	1	2017-01-11 13:54
<a href="#">LSHM-1XX-XX.X-XX-DV-A-X-X-TR-MKT.pdf</a>	1	2017-01-11 13:54
<a href="#">REF-189016-01.pdf</a>	1	2017-01-11 13:54
<a href="#">REF-189016-02.pdf</a>	1	2017-01-11 13:54
<a href="#">REF-189017-01.pdf</a>	1	2017-01-11 13:54
<a href="#">REF-189017-02.pdf</a>	1	2017-01-11 13:54
<a href="#">TC0923--2523_report_Rev_2_qua.pdf</a>	1	2017-01-11 13:54
<a href="#">hsc-report_lshm-lshm-05mm_web.pdf</a>	1	2017-01-11 13:54
<a href="#">lshm_dv.pdf</a>	1	2017-01-11 13:54
<a href="#">tc0929--2611_qua(1).pdf</a>	1	2017-01-11 13:54

## Variants Currently In Production

Module Variant	FPGA Chip Model	B14/Config Voltage [V]	R27 (VCCIO_0 on JM2 Pin 54)	SPI Flash
TE0714-02-35-2I	XC7A35T-2CSG325I	3.3	JM2 Pin 54 = VCCIO_0 (3.3 V)	S25FL127S
TE0714-02-35-2IC6	XC7A35T-2CSG325I	1.8	JM2 Pin 54 = Open	N25Q128
TE0714-02-50-2I	XC7A50T-2CSG325I	3.3	JM2 Pin 54 = VCCIO_0 (3.3 V)	S25FL127S
TE0714-02-50-2IC6	XC7A50T-2CSG325I	1.8	JM2 Pin 54 = Open	N25Q128



On REV 01 JM2 Pin 54 was connected to GND. When R27 is not populated, REV 02 is backwards compatible to REV 01. When R27 is set, check your baseboard to not connect this pin to GND. For all new baseboards JM2.54 should be used as VCCIO output (it will then be 1.8V or 3.3V depending the voltage settings on the module).

## Technical Specifications

### Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.1	6.0	V	-
HR I/O banks supply voltage (VCCO)	-0.5	3.6	V	Xilinx datasheet <a href="#">DS181</a>
HR I/O banks input voltage	-0.4	VCCO + 0.55	V	Xilinx datasheet <a href="#">DS181</a>
GTP transceivers Tx/Rx input voltage	-0.5	1.26	V	Xilinx datasheet <a href="#">DS181</a>
Voltage on module JTAG pins	-0.4	VCCO_0 + 0.55	V	Xilinx datasheet <a href="#">DS181</a>
Storage temperature	-40	+85	°C	-

### Recommended Operating Conditions

Parameter	Min	Max	Units	Notes
VIN supply voltage	3.135	3.45	V	-
HR I/O banks supply voltage (VCCO)	1.14	3.465	V	Xilinx datasheet <a href="#">DS181</a>
HR I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx datasheet <a href="#">DS181</a>
Voltage on module JTAG pins	3.135	3.465	V	Xilinx datasheet <a href="#">DS181</a>

### Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

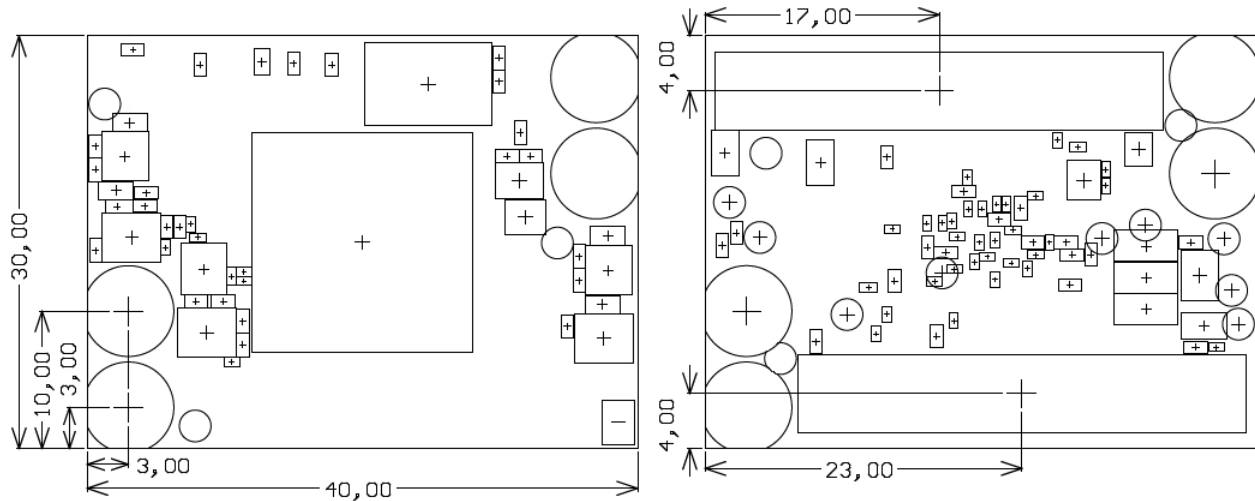


Please check Xilinx datasheet DS181 for complete list of absolute maximum and recommended operating ratings for the Artix-7.

## Physical Dimensions

- Module size: 40 mm x 30 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm
- PCB thickness: 1.6 mm
- Highest part on PCB: approximately 2.5 mm. Please download the step model for exact numbers.

All dimensions are shown in mm. Additional sketches, drawings and schematics can be found [here](#).



## Weight

Variant	Weight in g	Note
2IC6	8.3	Plain Module



# Revision History

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## Hardware Revision History

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Date	Revision	Notes	PCN Link	Documentation Link
2016-08-04	02	VCCIO0 added to B2B	<a href="#">PCN-20160815</a>	<a href="#">TE0714-02</a>
	01	-	-	<a href="#">TE0714-01</a>

Hardware revision number is printed on the PCB board next to the module model number separated by the dash.



## Document Change History

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Date	Revision	Authors	Description
2017-05-28	V.27	Jan Kumann	Board-to-Board I/O section added. New physical dimensions images. Documents sections rearranged.
2017-03-20	V.26	John Hartfiel	Notes on Clocking section.
2017-01-27	v.25	Jan Kumann	New block diagram.
2016-12-01	v.17	Jan Kumann	Changes in the document structure, few corrections.
2016-11-18	v.14	Thorsten Trenz, Emmanuel Vassilakis	Hardware revision 02 specific changes.
2016-06-01	v.9	Antti Lukats	Initial version.

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