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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl36z128vlh4

- 16-bit low-power timer (LPTMR)
- Real time clock

Security and integrity modules

- 80-bit unique identification number per chip

Ordering Information [1]

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL36Z64VLH4	64	8	54
MKL36Z128VLH4	128	16	54
MKL36Z256VLH4	256	32	54
MKL36Z256VMP4	256	32	54
MKL36Z64VLL4	64	8	84
MKL36Z128VLL4	128	16	84
MKL36Z256VLL4	256	32	84
MKL36Z128VMC4	128	16	84
MKL36Z256VMC4	256	32	84

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL36P121M48SF4RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL36P121M48SF4[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_*x*N40H[2]
Package drawing	Package dimensions are provided in package drawings.	LQFP 64-pin: 98ASS23234W[1] MAPBGA 64-pin: 98ASA00420D[1] LQFP 100-pin: 98ASS23308W[1] MAPBGA 121-pin: 98ASA00344D[1]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.
2. To find the associated resource, go to http://www.freescale.com and perform a search using this term with the "*x*" replaced by the revision of the device you are using.

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Table 7. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{OL}	Output low voltage — High drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	 — —	 0.5 0.5	 V V	1
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	3
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—		µA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	20	50	kΩ	4

1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLSx→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	1
	• VLLS0 → RUN	—	113	124	µs	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max	Unit	Note
I_{DD_LLS}	Low leakage stop mode current at 3.0 V	at 25 °C	2.00	2.7	µA	—
		at 50 °C	3.96	5.14	µA	
		at 70 °C	7.77	10.71	µA	
		at 85 °C	14.15	18.79	µA	
		at 105 °C	33.20	43.67	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V	at 25 °C	1.5	2.2	µA	—
		at 50 °C	2.83	3.55	µA	
		at 70 °C	5.53	7.26	µA	
		at 85 °C	9.92	12.71	µA	
		at 105 °C	22.90	29.23	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0V	at 25 °C	0.71	1.2	µA	—
		at 50 °C	1.27	1.9	µA	
		at 70 °C	2.48	3.51	µA	
		at 85 °C	4.65	6.29	µA	
		at 105 °C	11.55	14.34	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V	at 25 °C	0.41	0.9	µA	—
		at 50 °C	0.96	1.56	µA	
		at 70 °C	2.17	3.1	µA	
		at 85 °C	4.35	5.32	µA	
		at 105 °C	11.24	14.00	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V	at 25 °C	0.23	0.69	µA	7
		at 50 °C	0.77	1.35	µA	
		at 70 °C	1.98	2.52	µA	
		at 85 °C	4.16	5.14	µA	
		at 105 °C	11.05	13.80	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
6. MCG configured for BLPI mode.
7. No brownout.

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 14. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	52	452	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk128k}$	Read 1s Block execution time • 128 KB program flash	—	—	1.7	ms	—
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
$t_{ersblk128k}$	Erase Flash Block execution time • 128 KB program flash	—	88	600	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	—
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	175	1300	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.6.2 CMP and 6-bit DAC electrical specifications

Table 27. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

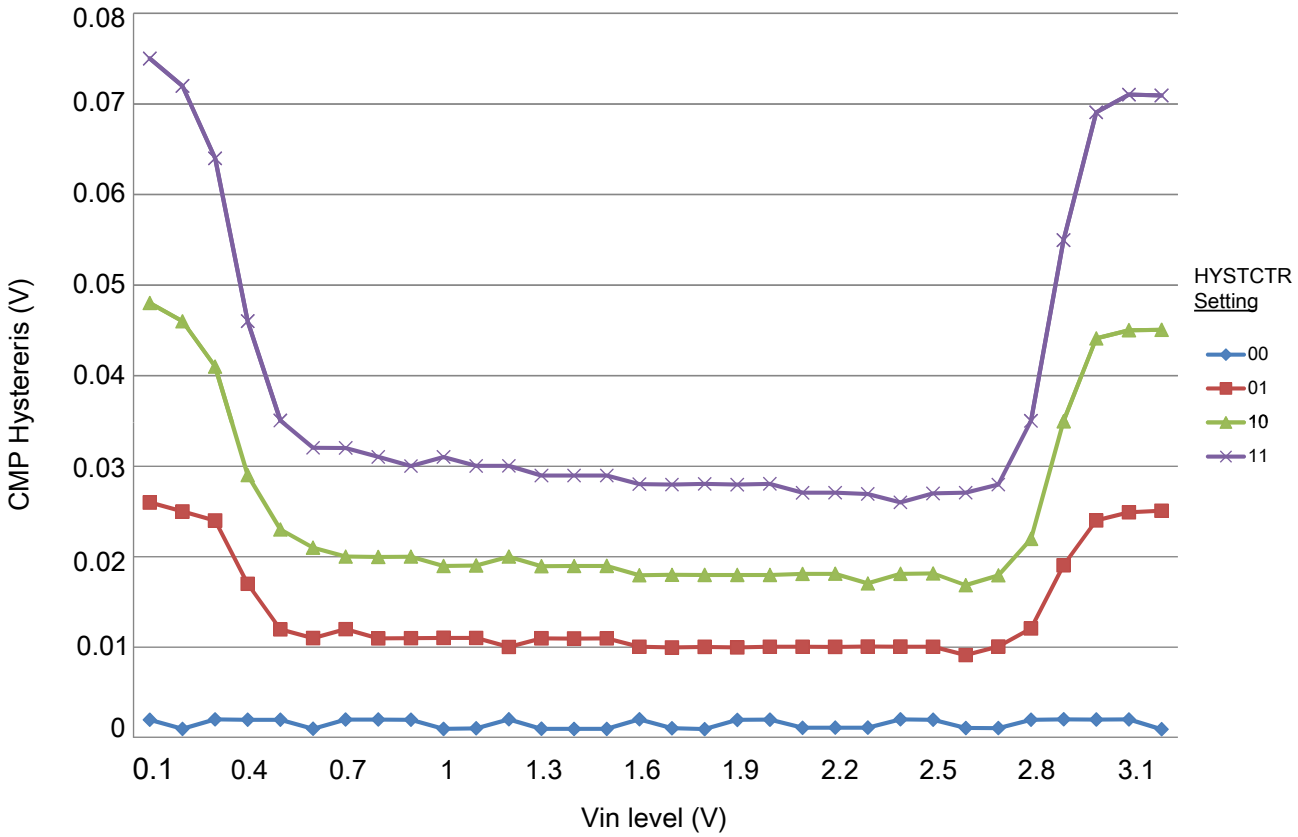


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

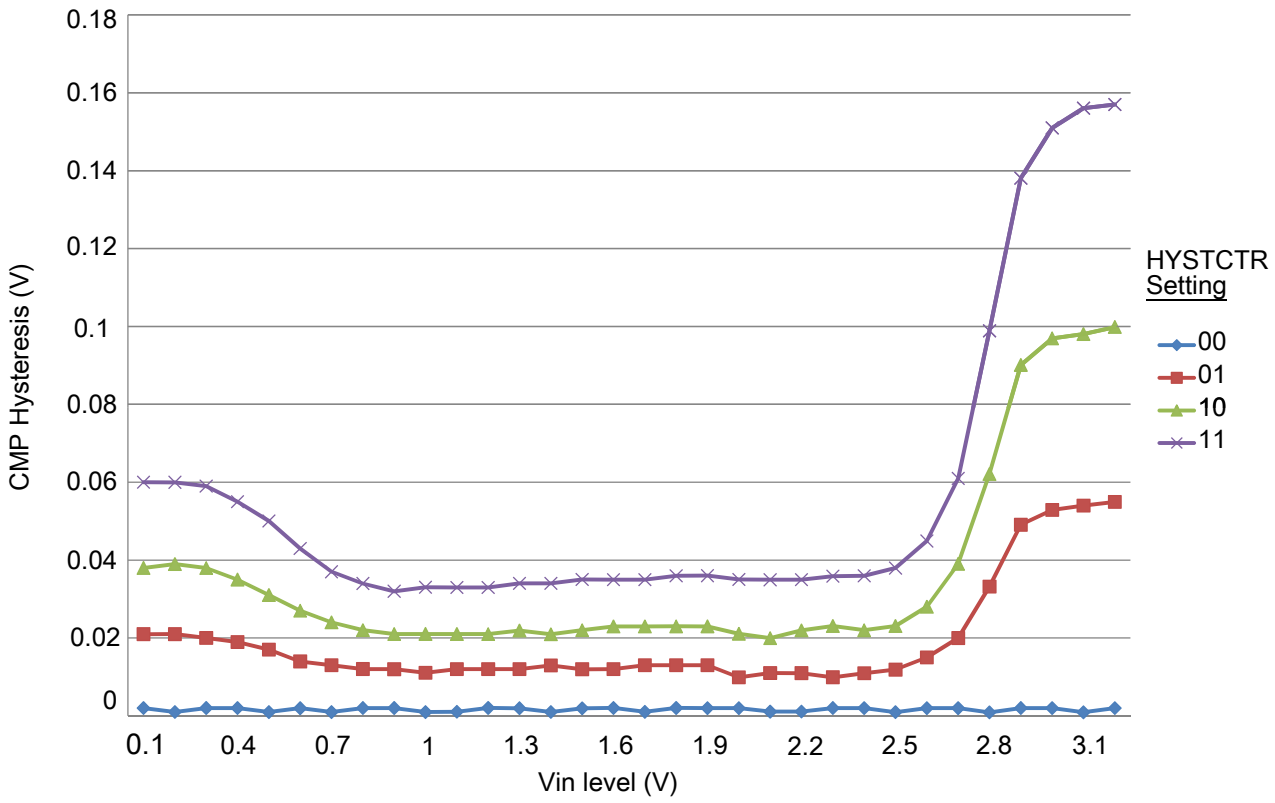


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 28. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

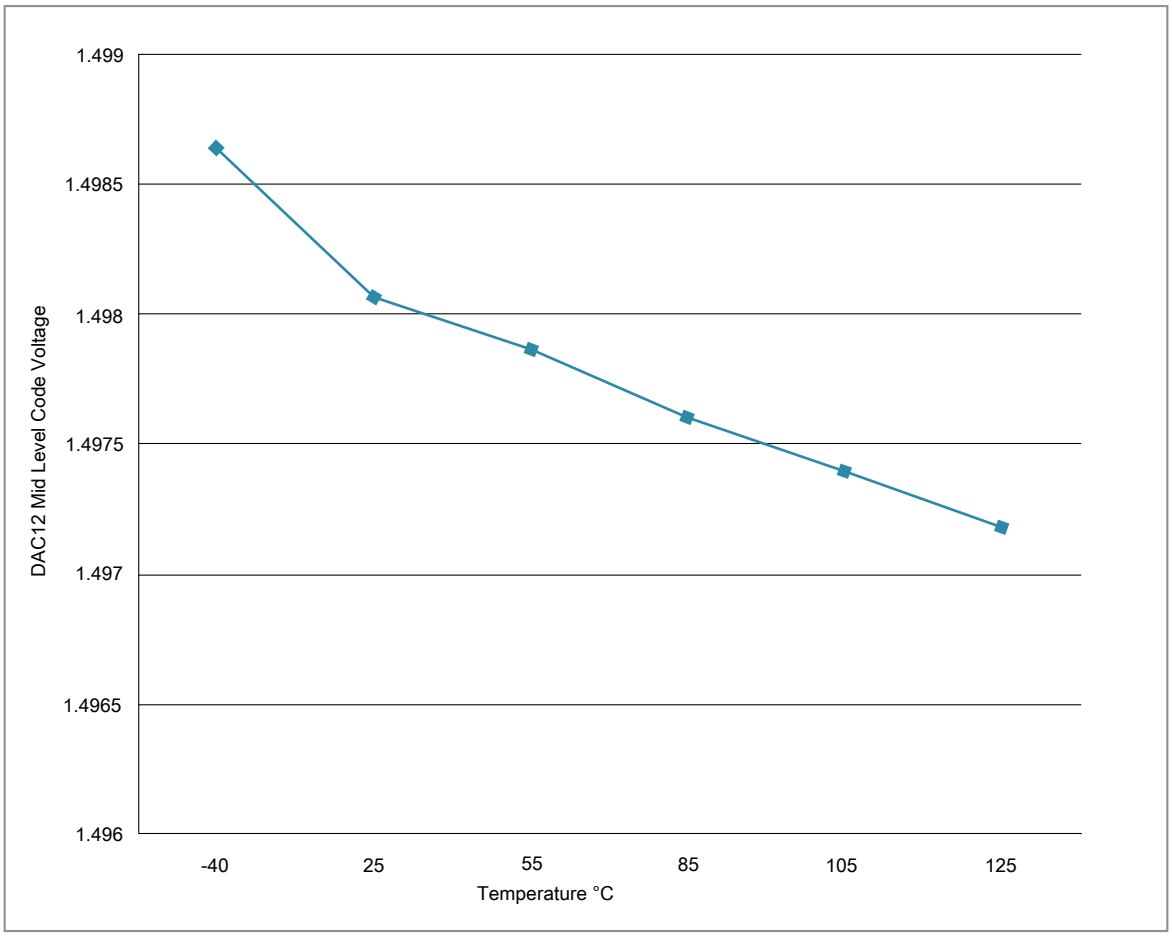


Figure 13. Offset at half scale vs. temperature

3.7 Timers

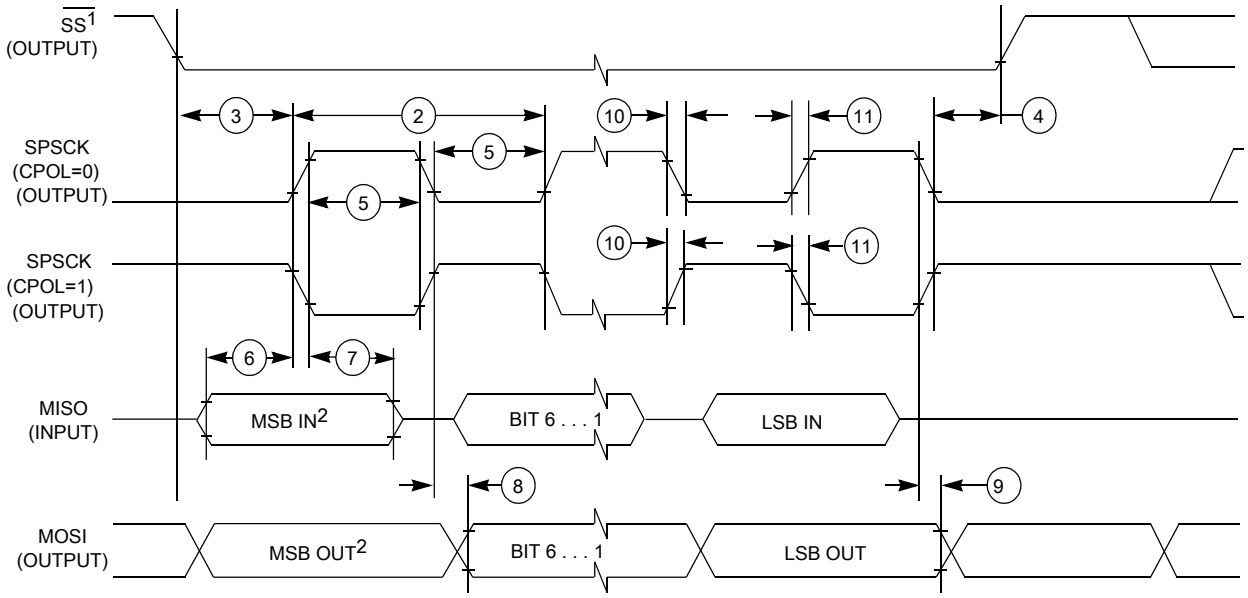
See General switching specifications.

3.8 Communication interfaces

Table 31. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA = 0)

Table 37. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

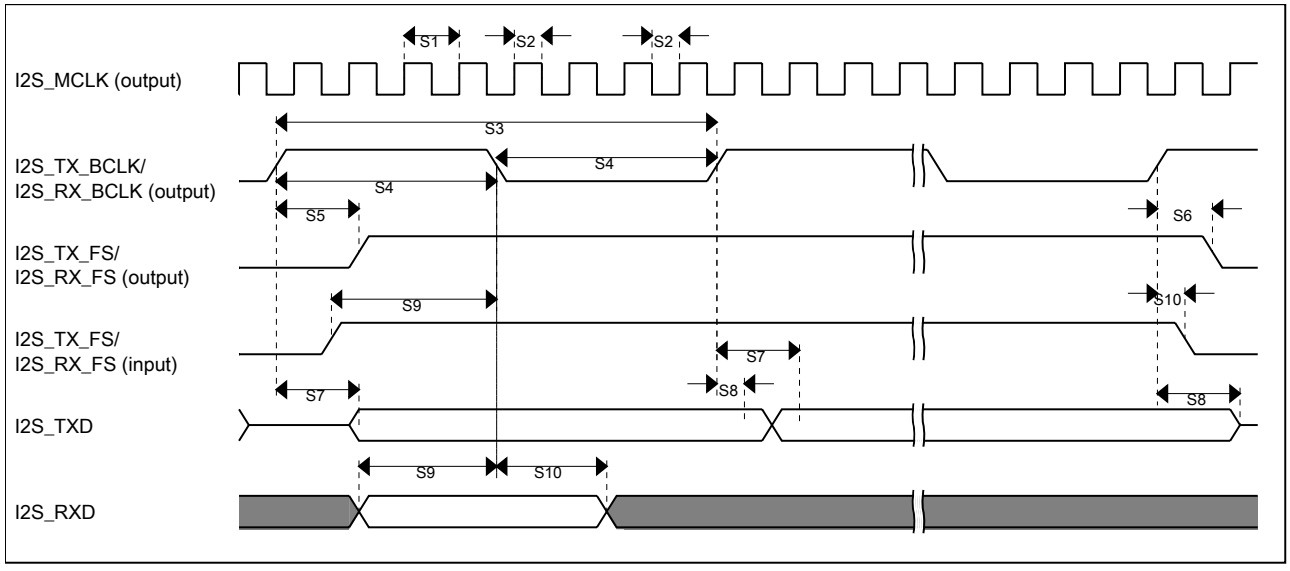


Figure 21. I2S/SAI timing — master modes

Table 38. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns

Table continues on the next page...

Table 38. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

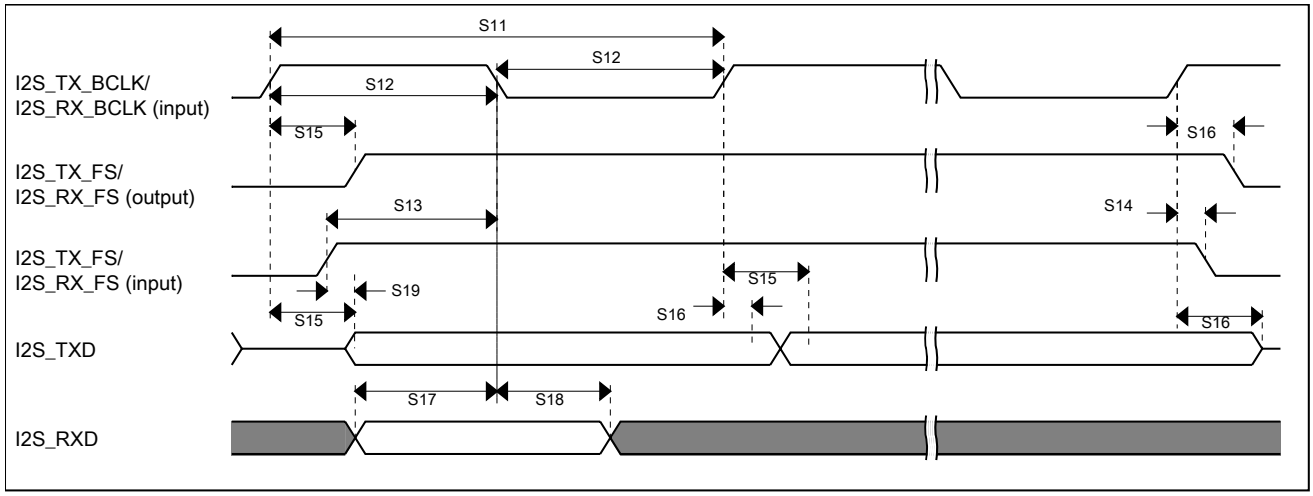


Figure 22. I2S/SAI timing — slave modes

3.9 Human-machine interfaces (HMI)

3.9.1 TSI electrical specifications

Table 39. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	µA

Table continues on the next page...

Table 40. LCD electricals (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• RVTRIM=0111	—	1.08	—		
	• RVTRIM=1111	—	1.09	—		
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	4
I_{RBIAS}	RBIAS current adder					
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	10	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	1	—	µA	
R_{RBIAS}	RBIAS resistor values					
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	0.28	—	MΩ	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	2.98	—	MΩ	
VLL1	VLL1 voltage	—	—	V_{IREG}	V	5
VLL2	VLL2 voltage	—	—	2 x V_{IREG}	V	5
VLL3	VLL3 voltage	—	—	3 x V_{IREG}	V	5
VLL1	VLL1 voltage	—	—	V_{DDA} / 3	V	6
VLL2	VLL2 voltage	—	—	V_{DDA} / 1.5	V	6
VLL3	VLL3 voltage	—	—	V_{DDA}	V	6

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V
4. 2000 pF load LCD, 32 Hz frame frequency
5. VLL1, VLL2 and VLL3 are a function of V_{IREG} only when the regulator is enabled (GCR[RVEN]=1) and the charge pump is enabled (GCR[CPSEL]=1).
6. VLL1, VLL2 and VLL3 are a function of V_{DDA} only under either of the following conditions:
   - The charge pump is enabled (GCR[CPSEL]=1), the regulator is disabled (GCR[RVEN]=0), and VLL3 = V_{DDA} through the internal power switch (GCR[VSUPPLY]=0).
   - The resistor bias string is enabled (GCR[CPSEL]=0), the regulator is disabled (GCR[RVEN]=0), and VLL3 is connected to V_{DDA} externally (GCR[VSUPPLY]=1).

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
A2	98	C1	62	PTD5	LCD_P45/ ADC0_SE6b	LCD_P45/ ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5			LCD_P45
B2	99	B2	63	PTD6/ LLWU_P15	LCD_P46/ ADC0_SE7b	LCD_P46/ ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	UART0_RX		SPI1_MISO		LCD_P46
A1	100	A2	64	PTD7	LCD_P47	LCD_P47	PTD7	SPI1_MISO	UART0_TX		SPI1_MOSI		LCD_P47
F1	10	—	—	NC	NC	NC							
F2	11	—	—	NC	NC	NC							
G1	12	—	—	NC	NC	NC							
G2	13	—	—	NC	NC	NC							
J3	—	—	—	NC	NC	NC							
H3	—	—	—	NC	NC	NC							
K4	—	—	—	NC	NC	NC							
L7	—	—	—	NC	NC	NC							
J9	—	—	—	NC	NC	NC							
J4	—	—	—	NC	NC	NC							
H11	—	—	—	NC	NC	NC							
F11	—	—	—	NC	NC	NC							
A5	—	—	—	NC	NC	NC							
B5	—	—	—	NC	NC	NC							
A4	—	—	—	NC	NC	NC							
B1	—	—	—	NC	NC	NC							
C2	—	—	—	NC	NC	NC							
C1	—	—	—	NC	NC	NC							
D2	—	—	—	NC	NC	NC							
D1	—	—	—	NC	NC	NC							
E1	—	—	—	NC	NC	NC							

5.2 KL36 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, ssee KL36 Signal Multiplexing and Pin Assignments.

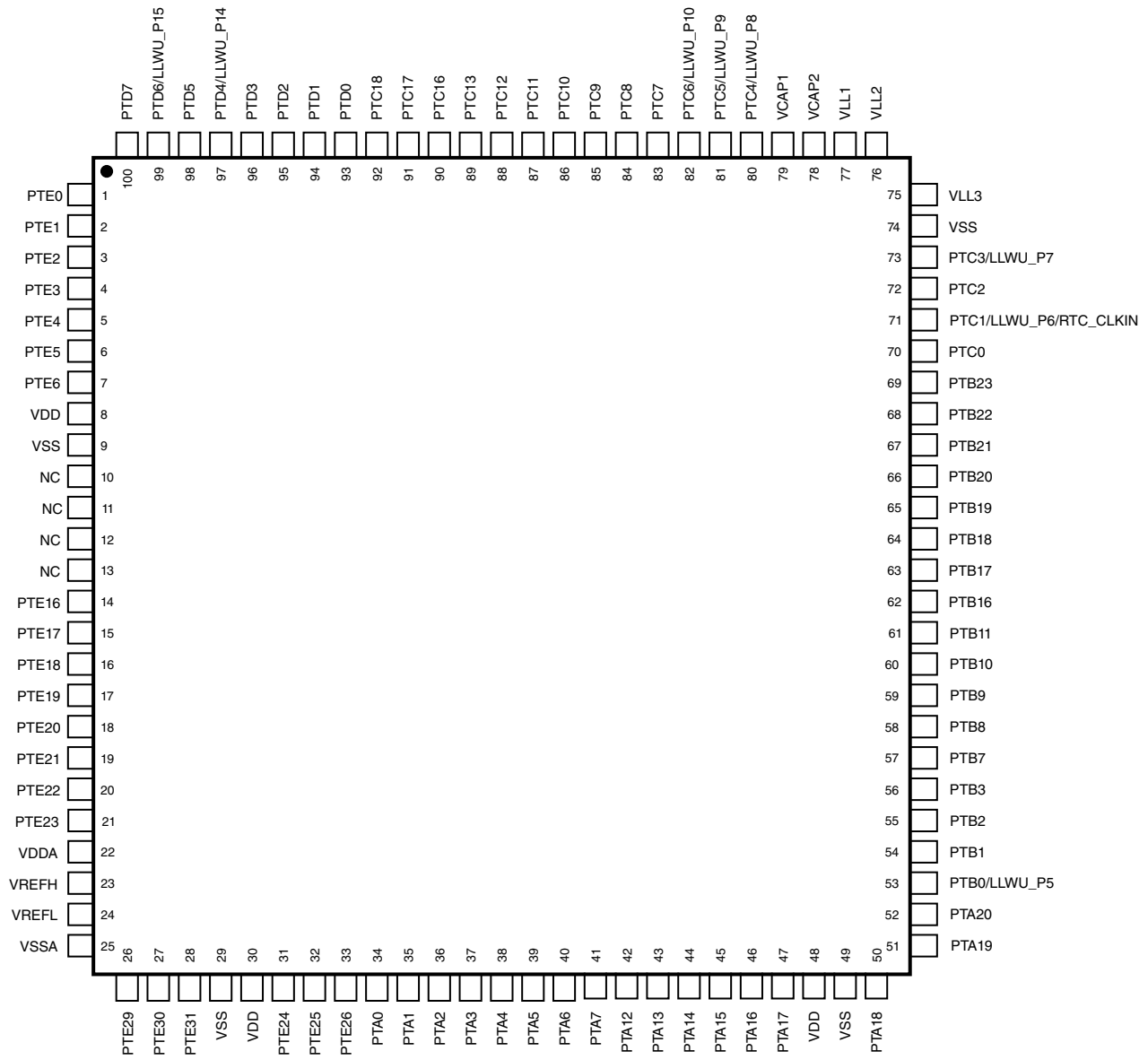


Figure 24. KL36 100-pin LQFP pinout diagram

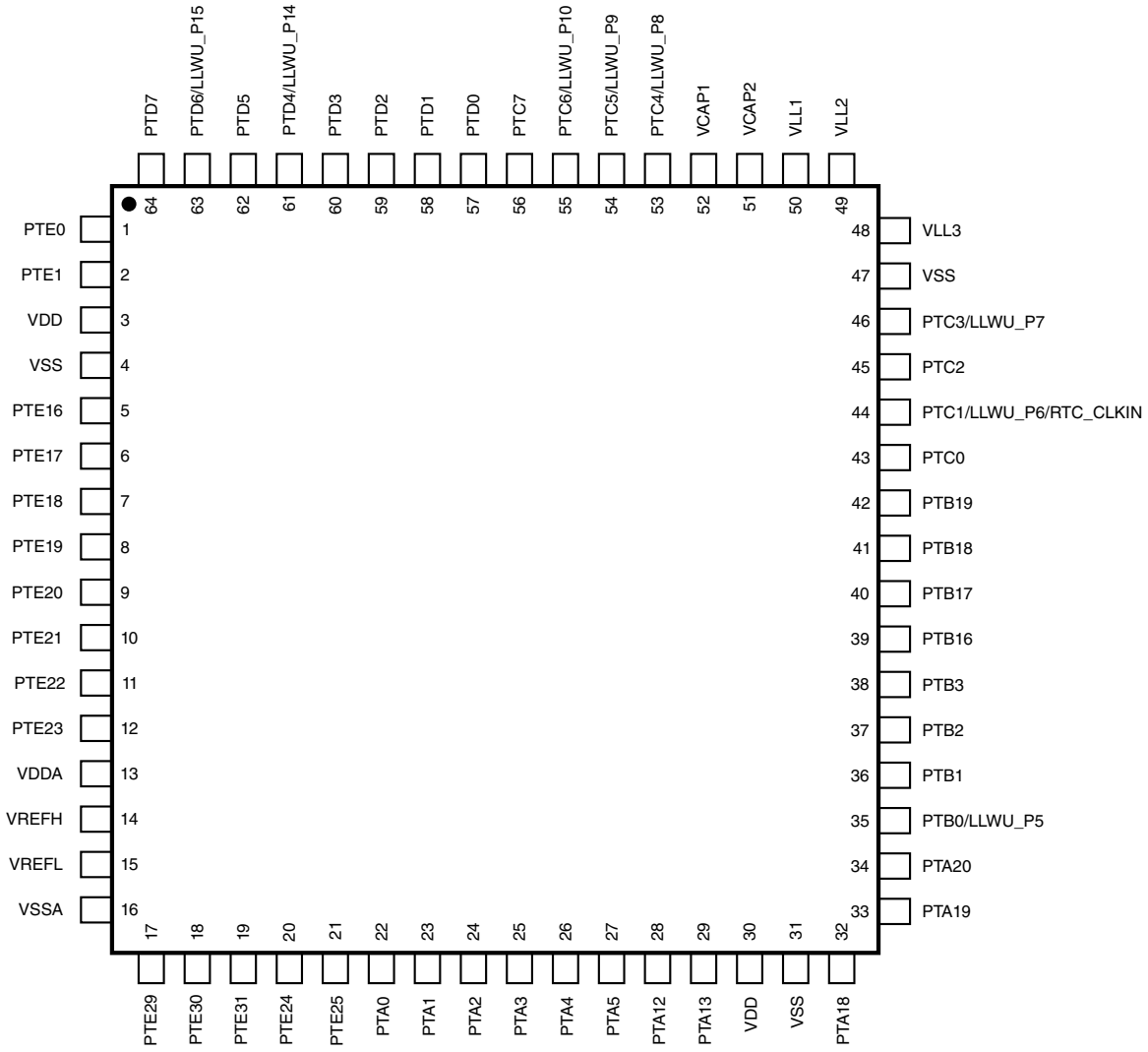


Figure 26. KL36 64-pin LQFP pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: PKL36 and MKL36

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

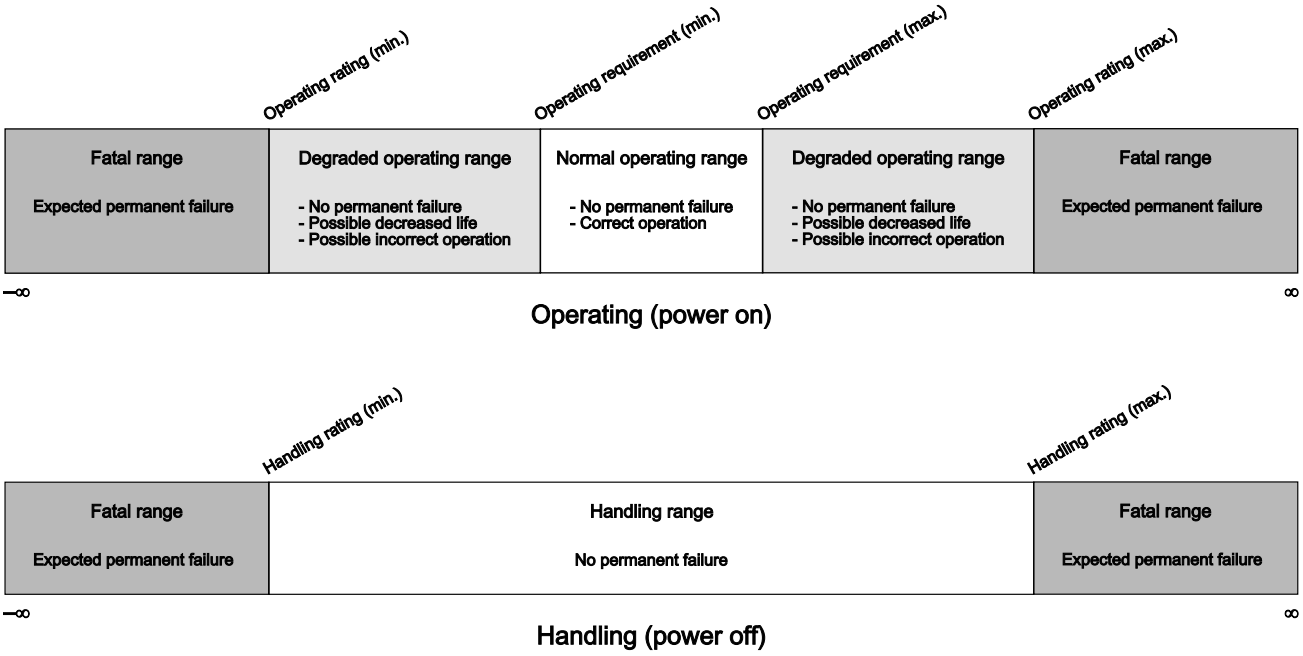
7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 41. Part number fields descriptions

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KL##	Kinetis family	• KL36
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 64 = 64 KB • 128 = 128 KB • 256 = 256 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel

8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

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Document Number KL36P121M48SF4
Revision 5 08/2014