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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl36z128vll4

- 16-bit low-power timer (LPTMR)
- Real time clock

Security and integrity modules
- 80-bit unique identification number per chip

Ordering Information [1]

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL36Z64VLH4	64	8	54
MKL36Z128VLH4	128	16	54
MKL36Z256VLH4	256	32	54
MKL36Z256VMP4	256	32	54
MKL36Z64VLL4	64	8	84
MKL36Z128VLL4	128	16	84
MKL36Z256VLL4	256	32	84
MKL36Z128VMC4	128	16	84
MKL36Z256VMC4	256	32	84

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL36P121M48SF4RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL36P121M48SF4[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_*x*N40H[2]
Package drawing	Package dimensions are provided in package drawings.	LQFP 64-pin: 98ASS23234W[1] MAPBGA 64-pin: 98ASA00420D[1] LQFP 100-pin: 98ASS23308W[1] MAPBGA 121-pin: 98ASA00344D[1]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.
2. To find the associated resource, go to http://www.freescale.com and perform a search using this term with the “*x*” replaced by the revision of the device you are using.

1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

Table 9. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max	Unit	Note
I_{DD_LLS}	Low leakage stop mode current at 3.0 V	at 25 °C	2.00	2.7	μA	—
		at 50 °C	3.96	5.14	μA	
		at 70 °C	7.77	10.71	μA	
		at 85 °C	14.15	18.79	μA	
		at 105 °C	33.20	43.67	μA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V	at 25 °C	1.5	2.2	μA	—
		at 50 °C	2.83	3.55	μA	
		at 70 °C	5.53	7.26	μA	
		at 85 °C	9.92	12.71	μA	
		at 105 °C	22.90	29.23	μA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0V	at 25 °C	0.71	1.2	μA	—
		at 50 °C	1.27	1.9	μA	
		at 70 °C	2.48	3.51	μA	
		at 85 °C	4.65	6.29	μA	
		at 105 °C	11.55	14.34	μA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V	at 25 °C	0.41	0.9	μA	—
		at 50 °C	0.96	1.56	μA	
		at 70 °C	2.17	3.1	μA	
		at 85 °C	4.35	5.32	μA	
		at 105 °C	11.24	14.00	μA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V	at 25 °C	0.23	0.69	μA	7
		at 50 °C	0.77	1.35	μA	
		at 70 °C	1.98	2.52	μA	
		at 85 °C	4.16	5.14	μA	
		at 105 °C	11.05	13.80	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
6. MCG configured for BLPI mode.
7. No brownout.

Table 10. Low power mode peripheral adders — typical value

Symbol	Description		Temperature (°C) -40	25	50	70	85	105	Unit
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.		56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.		52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.		206	228	237	245	251	258	µA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	VLLS1	440	490	540	560	570	580	nA
		VLLS3	440	490	540	560	570	580	
		LLS	490	490	540	560	570	680	
		VLPS	510	560	560	560	610	680	
		STOP	510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.		22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.		432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	µA
		OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	µA
		OSCERCLK (4 MHz external crystal)	235	256	265	274	280	287	

Table continues on the next page...

2.4.2 Thermal attributes

Table 16. Thermal attributes

Board type	Symbol	Description	121 MAPBGA	100 LQFP	64 LQFP	64 MAPBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	94	64	69	49.8	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	57	51	51	42.3	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	81	54	58	40.9	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	53	45	44	37.7	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	40	37	33	39.2	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	30	19	19	50.3	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	8	4	4	2.2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 17. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

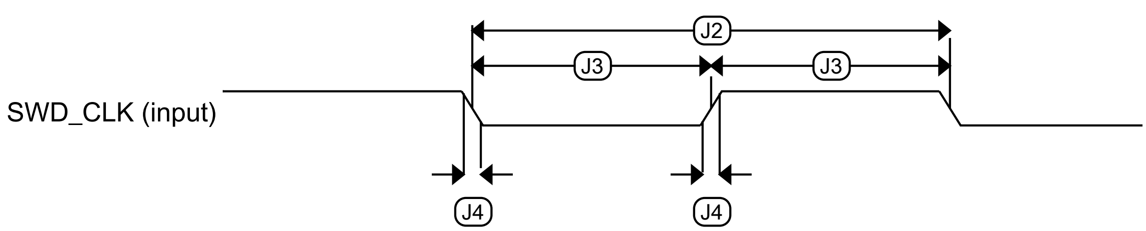


Figure 5. Serial wire clock input timing

3.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 25 and Table 26 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

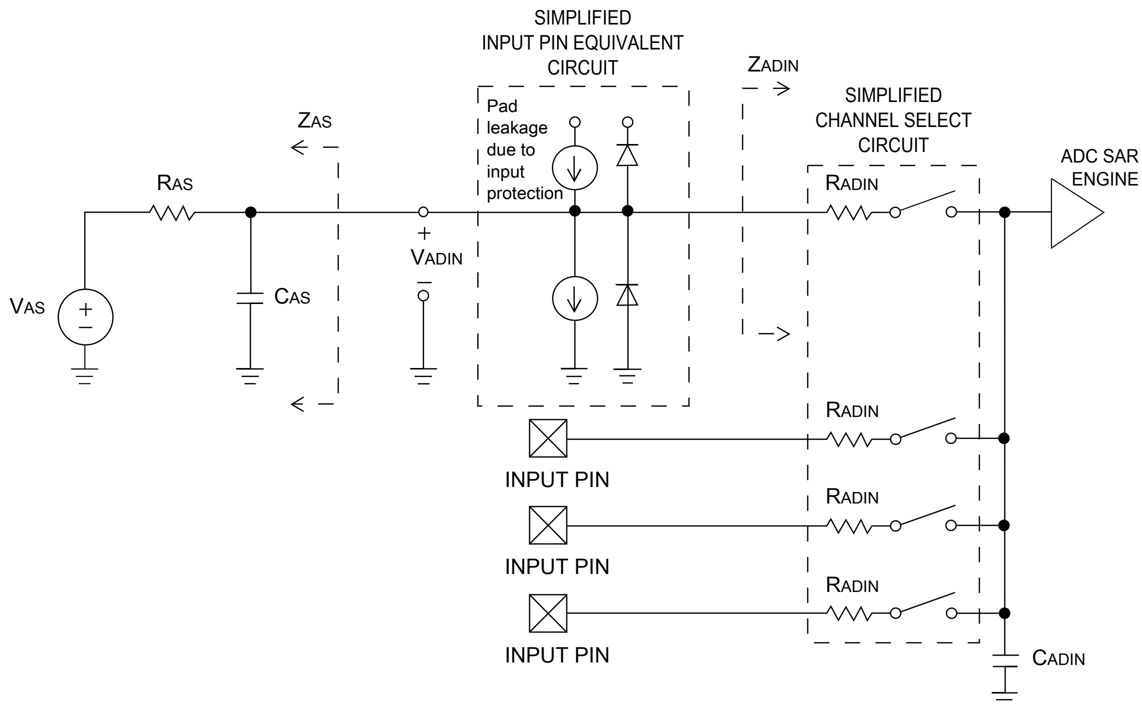


Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5

Table continues on the next page...

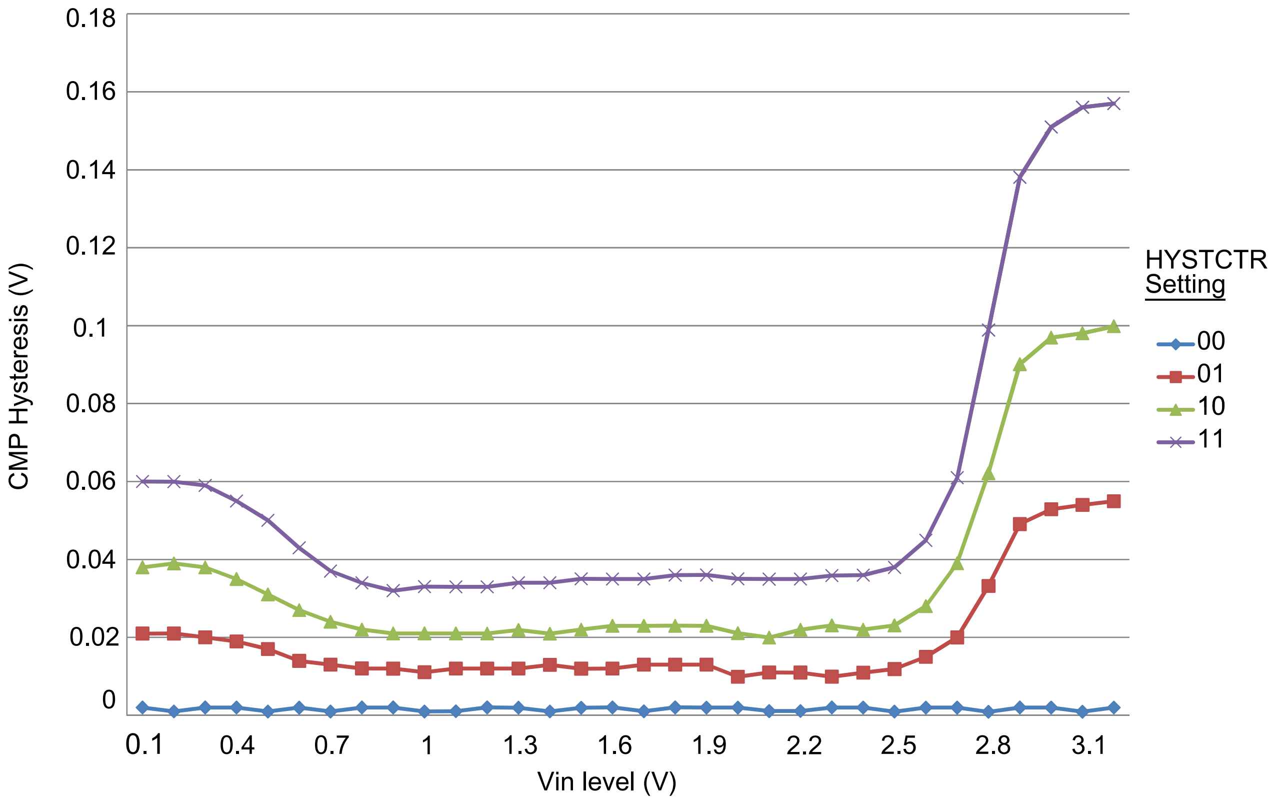


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 28. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 30. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	f_{periph}/2048	f_{periph}/2	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 31. SPI master mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	f_{periph}/2048	f_{periph}/2	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—

Table continues on the next page...

Table 36. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	33	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	28	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

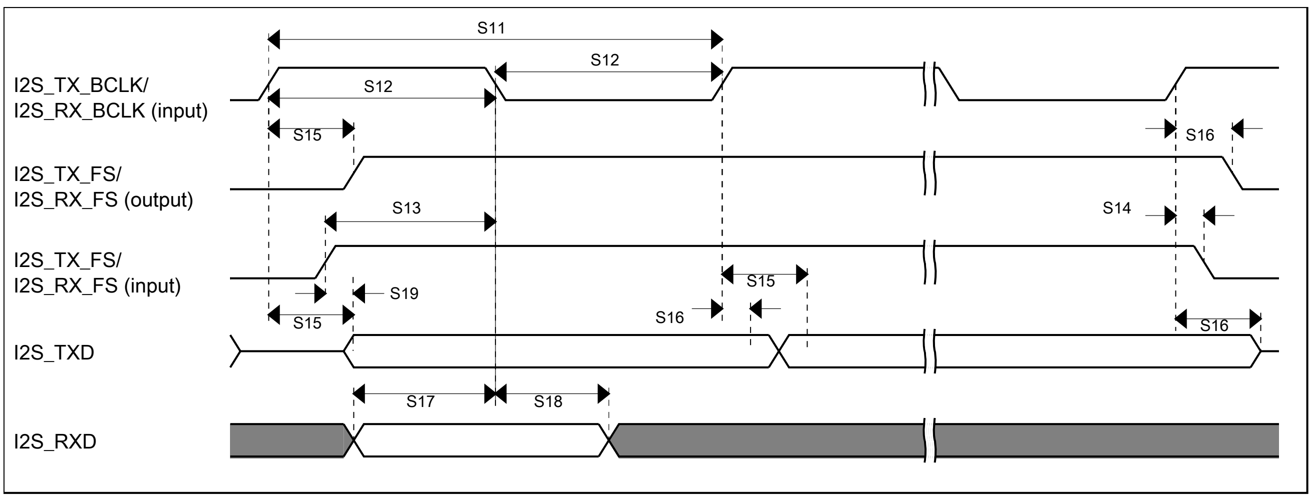


Figure 20. I2S/SAI timing — slave modes

3.8.4.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 39. TSI electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	µA
TSI_EN	Power consumption in enable mode	—	100	—	µA
TSI_DIS	Power consumption in disable mode	—	1.2	—	µA
TSI_TEN	TSI analog enable time	—	66	—	µs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V

3.9.2 LCD electrical characteristics

Table 40. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency					
	• GCR[FFR]=0	23.3	—	73.1	Hz	
	• GCR[FFR]=1	46.6	—	146.2	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}				V	3
	• RVTRIM=0000	—	0.91	—		
	• RVTRIM=1000	—	0.92	—		
	• RVTRIM=0100	—	0.93	—		
	• RVTRIM=1100	—	0.94	—		
	• RVTRIM=0010	—	0.96	—		
	• RVTRIM=1010	—	0.97	—		
	• RVTRIM=0110	—	0.98	—		
	• RVTRIM=1110	—	0.99	—		
	• RVTRIM=0001	—	1.01	—		
	• RVTRIM=1001	—	1.02	—		
	• RVTRIM=0101	—	1.03	—		
	• RVTRIM=1101	—	1.05	—		
	• RVTRIM=0011	—	1.06	—		
	• RVTRIM=1011	—	1.07	—		

Table continues on the next page...

Table 40. LCD electricals (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• RVTRIM=0111 • RVTRIM=1111	— —	1.08 1.09	— —		
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	μA	4
I_{RBIAS}	RBIAS current adder • LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF) • LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	 — —	 10 1	 — —	 μA μA	
R_{RBIAS}	RBIAS resistor values • LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF) • LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	 — —	 0.28 2.98	 — —	 MΩ MΩ	
VLL1	VLL1 voltage	—	—	V_{IREG}	V	5
VLL2	VLL2 voltage	—	—	2 x V_{IREG}	V	5
VLL3	VLL3 voltage	—	—	3 x V_{IREG}	V	5
VLL1	VLL1 voltage	—	—	V_{DDA} / 3	V	6
VLL2	VLL2 voltage	—	—	V_{DDA} / 1.5	V	6
VLL3	VLL3 voltage	—	—	V_{DDA}	V	6

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V
4. 2000 pF load LCD, 32 Hz frame frequency
5. VLL1, VLL2 and VLL3 are a function of V_{IREG} only when the regulator is enabled (GCR[RVEN]=1) and the charge pump is enabled (GCR[CPSEL]=1).
6. VLL1, VLL2 and VLL3 are a function of V_{DDA} only under either of the following conditions:
   - The charge pump is enabled (GCR[CPSEL]=1), the regulator is disabled (GCR[RVEN]=0), and VLL3 = V_{DDA} through the internal power switch (GCR[VSUPPLY]=0).
   - The resistor bias string is enabled (GCR[CPSEL]=0), the regulator is disabled (GCR[RVEN]=0), and VLL3 is connected to V_{DDA} externally (GCR[VSUPPLY]=1).

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D
100-pin LQFP	98ASS23308W
121-pin MAPBGA	98ASA00344D

5 Pinout

5.1 KL36 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
E4	1	A1	1	PTE0	DISABLED	LCD_P48	PTE0	SPI1_MISO	UART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	LCD_P48
E3	2	B1	2	PTE1	DISABLED	LCD_P49	PTE1	SPI1_MOSI	UART1_RX		SPI1_MISO	I2C1_SCL	LCD_P49
E2	3	—	—	PTE2	DISABLED	LCD_P50	PTE2	SPI1_SCK					LCD_P50
F4	4	—	—	PTE3	DISABLED	LCD_P51	PTE3	SPI1_MISO			SPI1_MOSI		LCD_P51
H7	5	—	—	PTE4	DISABLED	LCD_P52	PTE4	SPI1_PCS0					LCD_P52
G4	6	—	—	PTE5	DISABLED	LCD_P53	PTE5						LCD_P53
F3	7	—	—	PTE6	DISABLED	LCD_P54	PTE6			I2S0_MCLK	audioUSB_SOF_OUT		LCD_P54
E6	8	—	3	VDD	VDD	VDD							
G7	9	C4	4	VSS	VSS	VSS							
L6	—	—	—	VSS	VSS	VSS							
H1	14	E1	5	PTE16	ADC0_DP1/ ADC0_SE1	LCD_P55/ ADC0_DP1/ ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_CLKIN0			LCD_P55
H2	15	D1	6	PTE17	ADC0_DM1/ ADC0_SE5a	LCD_P56/ ADC0_DM1/ ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_CLKIN1		LPTMR0_ALT3	LCD_P56
J1	16	E2	7	PTE18	ADC0_DP2/ ADC0_SE2	LCD_P57/ ADC0_DP2/ ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO		LCD_P57

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
C8	72	B7	45	PTC2	LCD_P22/ ADC0_SE11/ TSI0_CH15	LCD_P22/ ADC0_SE11/ TSI0_CH15	PTC2	I2C1_SDA		TPM0_CH1		I2S0_TX_FS	LCD_P22
B8	73	C8	46	PTC3/ LLWU_P7	LCD_P23	LCD_P23	PTC3/ LLWU_P7		UART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_ BCLK	LCD_P23
F7	74	E3	47	VSS	VSS	VSS							
E7	—	E4	—	VDD	VDD	VDD							
A11	75	C5	48	VLL3	VLL3	VLL3							
A10	76	A6	49	VLL2	VLL2	VLL2/ LCD_P4	PTC20						LCD_P4
A9	77	B5	50	VLL1	VLL1	VLL1/ LCD_P5	PTC21						LCD_P5
B11	78	B4	51	VCAP2	VCAP2	VCAP2/ LCD_P6	PTC22						LCD_P6
C11	79	A5	52	VCAP1	VCAP1	VCAP1/ LCD_P39	PTC23						LCD_P39
A8	80	B8	53	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3	I2S0_MCLK		LCD_P24
D7	81	A8	54	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0		CMP0_OUT	LCD_P25
C7	82	A7	55	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_ BCLK	SPI0_MISO	I2S0_MCLK	LCD_P26
B7	83	B6	56	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_MISO	audioUSB_ SOF_OUT	I2S0_RX_FS	SPI0_MOSI		LCD_P27
A7	84	—	—	PTC8	LCD_P28/ CMP0_IN2	LCD_P28/ CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4	I2S0_MCLK			LCD_P28
D6	85	—	—	PTC9	LCD_P29/ CMP0_IN3	LCD_P29/ CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5	I2S0_RX_ BCLK			LCD_P29
C6	86	—	—	PTC10	LCD_P30	LCD_P30	PTC10	I2C1_SCL		I2S0_RX_FS			LCD_P30
C5	87	—	—	PTC11	LCD_P31	LCD_P31	PTC11	I2C1_SDA		I2S0_RXD0			LCD_P31
B6	88	—	—	PTC12	LCD_P32	LCD_P32	PTC12			TPM_ CLKIN0			LCD_P32
A6	89	—	—	PTC13	LCD_P33	LCD_P33	PTC13			TPM_ CLKIN1			LCD_P33
D5	90	—	—	PTC16	LCD_P36	LCD_P36	PTC16						LCD_P36
C4	91	—	—	PTC17	LCD_P37	LCD_P37	PTC17						LCD_P37
B4	92	—	—	PTC18	LCD_P38	LCD_P38	PTC18						LCD_P38
D4	93	C3	57	PTD0	LCD_P40	LCD_P40	PTD0	SPI0_PCS0		TPM0_CH0			LCD_P40
D3	94	A4	58	PTD1	LCD_P41/ ADC0_SE5b	LCD_P41/ ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1			LCD_P41
C3	95	C2	59	PTD2	LCD_P42	LCD_P42	PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO		LCD_P42
B3	96	B3	60	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI		LCD_P43
A3	97	A3	61	PTD4/ LLWU_P14	LCD_P44	LCD_P44	PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4			LCD_P44

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	NC	NC	PTC13	PTC8	PTC4/ LLWU_P8	VLL1	VLL2	VLL3	A
B	NC	PTD6/ LLWU_P15	PTD3	PTC18	NC	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	VCAP2	B
C	NC	NC	PTD2	PTC17	PTC11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	VCAP1	C
D	NC	NC	PTD1	PTD0	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6/ RTC_CLKIN	PTB18	PTB10	PTB8	D
E	NC	PTE2	PTE1	PTE0	VDD	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	NC	NC	PTE6	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	NC	F
G	NC	NC	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	PTE16	PTE17	NC	PTA7	PTE24	PTE26	PTE4	PTA1	PTA3	PTA17	NC	H
J	PTE18	PTE19	NC	NC	PTE25	PTA0	PTA2	PTA4	NC	PTA16	PTA20	J
K	PTE20	PTE21	PTA6	NC	PTE30	VDD	PTA5	PTA12	PTA14	VSS	PTA19	K
L	PTE22	PTE23	PTE29	PTE31	VSS	VSS	NC	PTA13	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 23. KL36 121-pin BGA pinout diagram

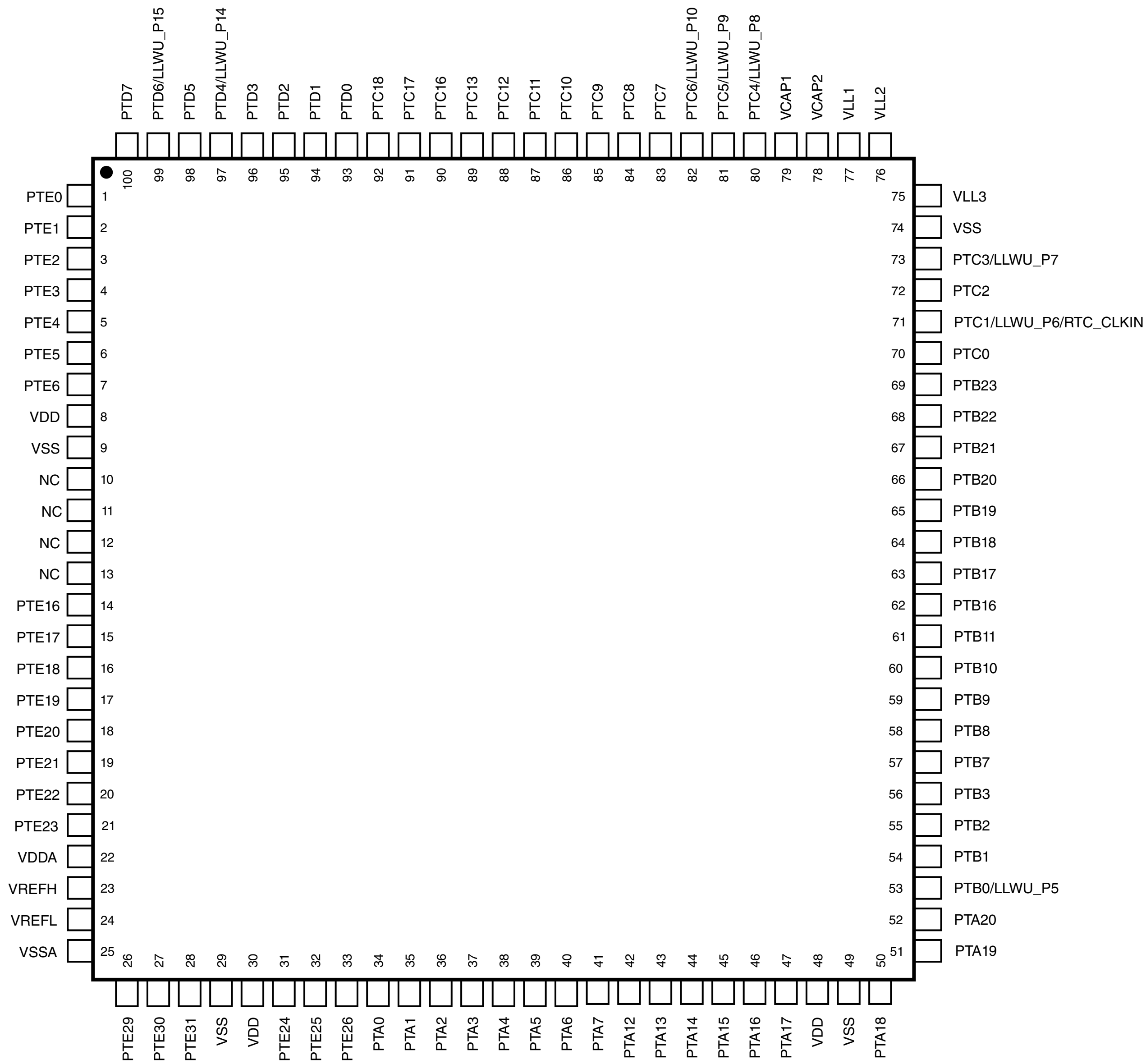


Figure 24. KL36 100-pin LQFP pinout diagram

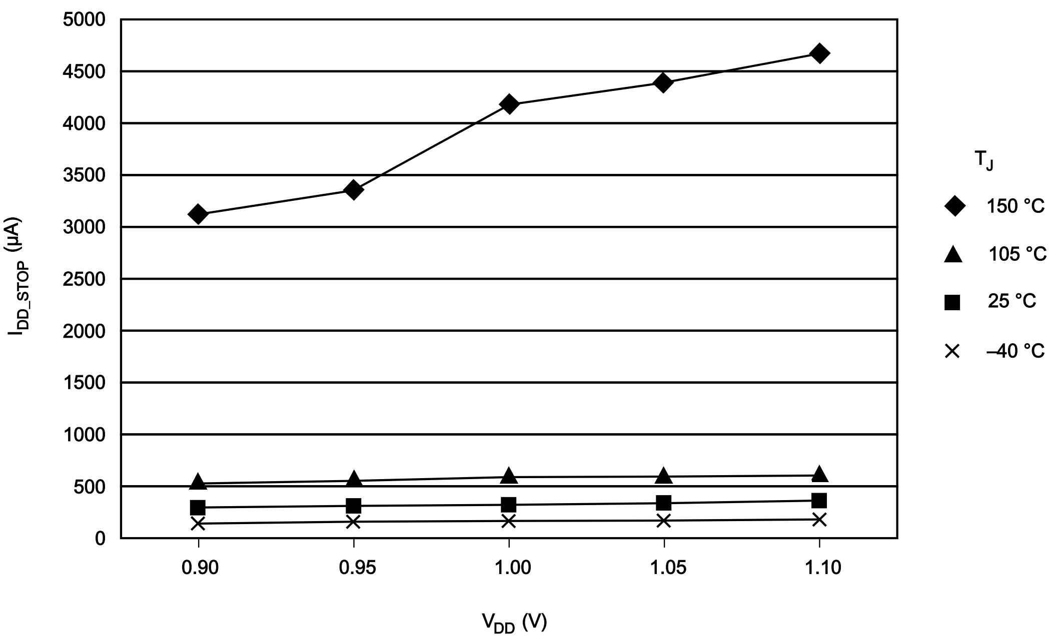
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 42. Typical value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 43. Revision history

Rev. No.	Date	Substantial Changes
3	3/2014	• Updated the front page and restructured the chapters • Updated Voltage and current operating behaviors • Updated EMC radiated emissions operating behaviors • Updated Power mode transition operating behaviors • Updated Capacitance attributes • Updated footnote in the Device clock specifications • Added thermal attributes of 64-pin MAPBGA in the Thermal attributes • Added V_{REFH} and V_{REFL} in the 16-bit ADC electrical characteristics • Updated footnote to the V_{DACR} in the 12-bit DAC operating requirements • Added Inter-Integrated Circuit Interface (I2C) timing
4	5/2014	• Updated Power consumption operating behaviors • Updated Definition: Operating behavior
5	08/2014	• Updated related source in the front page • Updated Power consumption operating behaviors

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