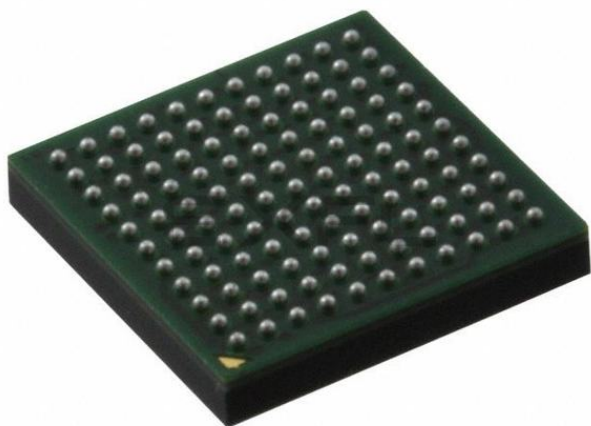




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl36z128vmc4

- 16-bit low-power timer (LPTMR)
- Real time clock

Security and integrity modules

- 80-bit unique identification number per chip

Ordering Information ¹

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MKL36Z64VLH4	64	8	54
MKL36Z128VLH4	128	16	54
MKL36Z256VLH4	256	32	54
MKL36Z256VMP4	256	32	54
MKL36Z64VLL4	64	8	84
MKL36Z128VLL4	128	16	84
MKL36Z256VLL4	256	32	84
MKL36Z128VMC4	128	16	84
MKL36Z256VMC4	256	32	84

1. To confirm current availability of orderable part numbers, go to <http://www.freescale.com> and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL36P121M48SF4RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL36P121M48SF4 ¹
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_xN40H ²
Package drawing	Package dimensions are provided in package drawings.	LQFP 64-pin: 98ASS23234W ¹ MAPBGA 64-pin: 98ASA00420D ¹ LQFP 100-pin: 98ASS23308W ¹ MAPBGA 121-pin: 98ASA00344D ¹

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.
2. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term with the “x” replaced by the revision of the device you are using.

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1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

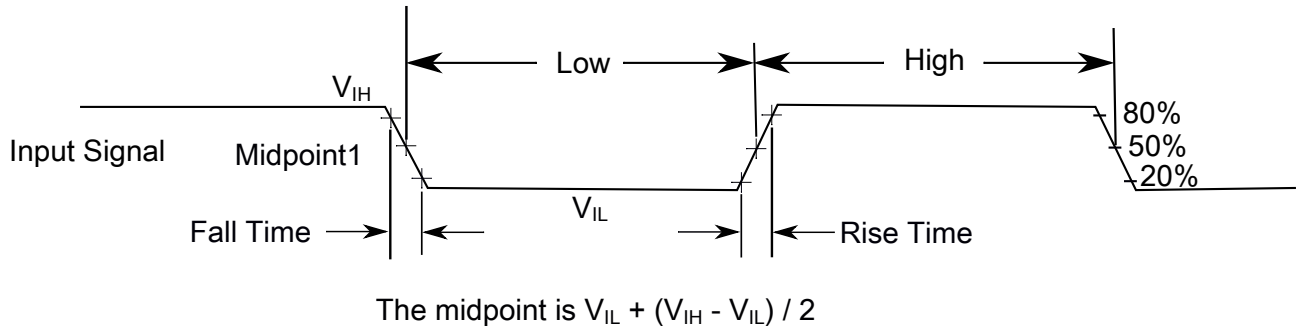


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L=30$ pF loads
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

Table 8. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLLS1 → RUN	—	112	124	μs	
	• VLLS3 → RUN	—	53	60	μs	
	• LLS → RUN	—	4.5	5.0	μs	
	• VLPS → RUN	—	4.5	5.0	μs	
	• STOP → RUN	—	4.5	5.0	μs	

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 9. Power consumption operating behaviors

Symbol	Description		Typ.	Max	Unit	Note
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUNCO_CM}	Run mode current in compute operation - 48 MHz core / 24 MHz flash/ bus disabled, LPTMR running using 4 MHz internal reference clock, CoreMark® benchmark code executing from flash, at 3.0 V	—	6.7	—	mA	2
I _{DD_RUNCO}	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash, at 3.0 V	—	4.5	5.1	mA	3
I _{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code executing from flash	at 1.8 V	5.6	6.3	mA	3
		at 3.0 V	5.4	6.0	mA	
I _{DD_RUN}	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 1.8 V	—	6.9	7.3	mA	3, 4
	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 25 °C	—	6.9	7.1	mA	
	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code executing from flash, at 3.0 V	at 125 °C	7.3	7.6	mA	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description		Typ.	Max	Unit	Note
I _{DD_LLS}	Low leakage stop mode current at 3.0 V	at 25 °C	2.00	2.7	μA	—
		at 50 °C	3.96	5.14	μA	
		at 70 °C	7.77	10.71	μA	
		at 85 °C	14.15	18.79	μA	
		at 105 °C	33.20	43.67	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V	at 25 °C	1.5	2.2	μA	—
		at 50 °C	2.83	3.55	μA	
		at 70 °C	5.53	7.26	μA	
		at 85 °C	9.92	12.71	μA	
		at 105 °C	22.90	29.23	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0V	at 25 °C	0.71	1.2	μA	—
		at 50 °C	1.27	1.9	μA	
		at 70 °C	2.48	3.51	μA	
		at 85 °C	4.65	6.29	μA	
		at 105 °C	11.55	14.34	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V	at 25 °C	0.41	0.9	μA	—
		at 50 °C	0.96	1.56	μA	
		at 70 °C	2.17	3.1	μA	
		at 85 °C	4.35	5.32	μA	
		at 105 °C	11.24	14.00	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V	at 25 °C	0.23	0.69	μA	7
		at 50 °C	0.77	1.35	μA	
		at 70 °C	1.98	2.52	μA	
		at 85 °C	4.16	5.14	μA	
		at 105 °C	11.05	13.80	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
6. MCG configured for BLPI mode.
7. No brownout.

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{IREFSTEN4MHz}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I _{IREFSTEN32KHz}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I _{REFSTEN4MHz}	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	μA
I _{REFSTEN32KHz}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	VLLS1	440	490	540	570	580	nA
		VLLS3	440	490	540	570	580	
		LLS	490	490	540	570	680	
		VLPS	510	560	560	610	680	
		STOP	510	560	560	610	680	
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	μA
		OSCERCLK (4 MHz external crystal)	214	237	246	254	260	
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	μA
		OSCERCLK (4 MHz external crystal)	235	256	265	274	280	

Table continues on the next page...

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 14. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T _J	Die junction temperature	−40	125	°C
T _A	Ambient temperature	−40	105	°C

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	μs	—
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{h\text{versblk}128\text{k}}$	Erase Block high-voltage time for 128 KB	—	52	452	ms	1
$t_{h\text{versall}}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{\text{rd}1\text{blk}128\text{k}}$	Read 1s Block execution time • 128 KB program flash	—	—	1.7	ms	—
$t_{\text{rd}1\text{sec}1\text{k}}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
$t_{\text{rd}r\text{src}}$	Read Resource execution time	—	—	30	μs	1
$t_{\text{pgm}4}$	Program Longword execution time	—	65	145	μs	—
$t_{\text{ersblk}128\text{k}}$	Erase Flash Block execution time • 128 KB program flash	—	88	600	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
$t_{\text{rd}1\text{all}}$	Read 1s All Blocks execution time	—	—	1.8	ms	—
$t_{\text{rd}o\text{nce}}$	Read Once execution time	—	—	25	μs	1
$t_{\text{pgm}o\text{nce}}$	Program Once execution time	—	65	—	μs	—
t_{ersall}	Erase All Blocks execution time	—	175	1300	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.6.1.1 16-bit ADC operating conditions

Table 25. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	16-bit differential mode - All other modes	V_{REFL} V_{REFL}	— —	31/32 * V_{REFH} V_{REFH}	V	—
C_{ADIN}	Input capacitance	16-bit mode 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	k Ω	—
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes $f_{ADCK} < 4$ MHz	—	—	5	k Ω	3
f_{ADCK}	ADC conversion clock frequency	$\leq$ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	$\leq$ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8 \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
INL	Integral non-linearity	12-bit modes <12-bit modes	—	±1.0	–2.7 to +1.9	LSB ⁴	5
E _{FS}	Full-scale error	12-bit modes <12-bit modes	—	–4	–5.4	LSB ⁴	$V_{ADIN} = V_{DDA}$ ⁵
E _Q	Quantization error	16-bit modes ≤13-bit modes	—	–1 to 0	—	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	–94 –85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	7
E _{IL}	Input leakage error		$I_{IN} \times R_{AS}$			mV	I_{IN} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

3.6.3.2 12-bit DAC operating behaviors

Table 29. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2 V$	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4 V$	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu V/C$	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
R_{op}	Output resistance (load = 3 k Ω)	—	—	250	Ω	
SR	Slew rate -80h $\rightarrow$ F7Fh $\rightarrow$ 80h - High power (SP_{HP}) - Low power (SP_{LP})	1.2 0.05	1.7 0.12	— —	V/ μs	
BW	3dB bandwidth - High power (SP_{HP}) - Low power (SP_{LP})	550 40	— —	— —	kHz	

- Settling within ± 1 LSB
- The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4 V$
- Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
- $V_{DDA} = 3.0 V$, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

Table 33. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	$4 \times t_{periph}$	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

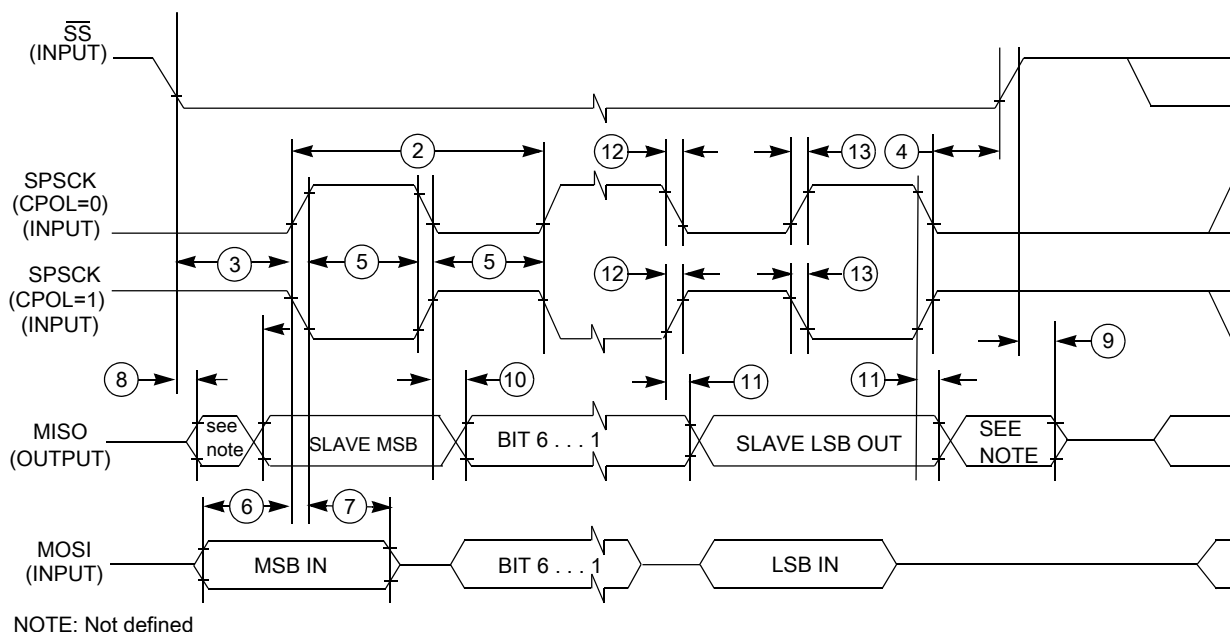


Figure 16. SPI slave mode timing (CPHA = 0)

Table 38. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

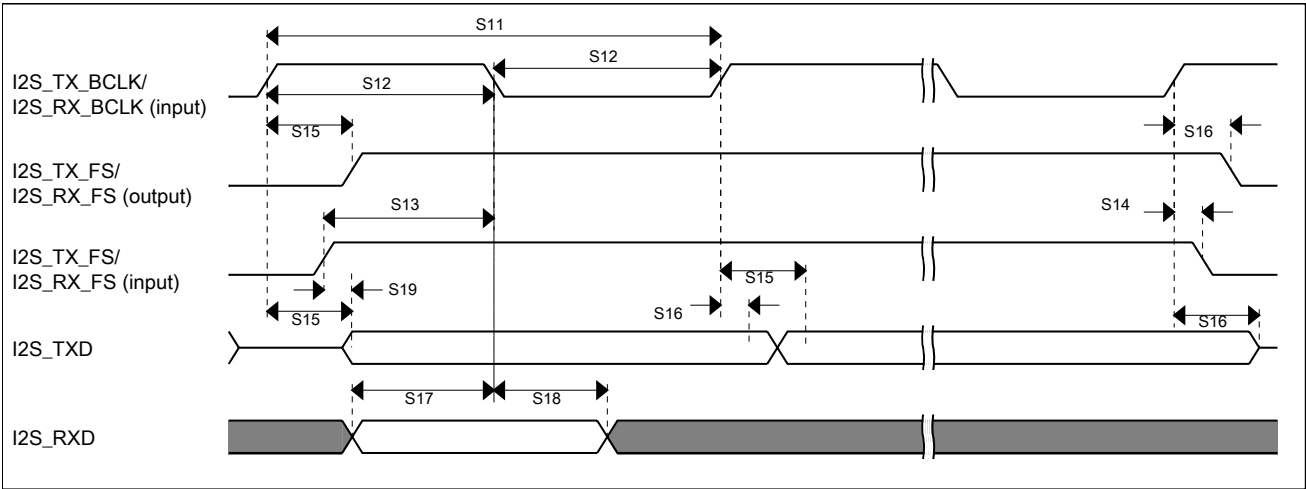


Figure 22. I2S/SAI timing — slave modes

3.9 Human-machine interfaces (HMI)

3.9.1 TSI electrical specifications

Table 39. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA

Table continues on the next page...

Pinout

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
C8	72	B7	45	PTC2	LCD_P22/ ADC0_SE11/ TSIO_CH15	LCD_P22/ ADC0_SE11/ TSIO_CH15	PTC2	I2C1_SDA		TPM0_CH1		I2S0_TX_FS	LCD_P22
B8	73	C8	46	PTC3/ LLWU_P7	LCD_P23	LCD_P23	PTC3/ LLWU_P7		UART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_ BCLK	LCD_P23
F7	74	E3	47	VSS	VSS	VSS							
E7	—	E4	—	VDD	VDD	VDD							
A11	75	C5	48	VLL3	VLL3	VLL3							
A10	76	A6	49	VLL2	VLL2	VLL2/ LCD_P4	PTC20						LCD_P4
A9	77	B5	50	VLL1	VLL1	VLL1/ LCD_P5	PTC21						LCD_P5
B11	78	B4	51	VCAP2	VCAP2	VCAP2/ LCD_P6	PTC22						LCD_P6
C11	79	A5	52	VCAP1	VCAP1	VCAP1/ LCD_P39	PTC23						LCD_P39
A8	80	B8	53	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3	I2S0_MCLK		LCD_P24
D7	81	A8	54	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0		CMP0_OUT	LCD_P25
C7	82	A7	55	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_ BCLK	SPI0_MISO	I2S0_MCLK	LCD_P26
B7	83	B6	56	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_MISO	audioUSB_ SOF_OUT	I2S0_RX_FS	SPI0_MOSI		LCD_P27
A7	84	—	—	PTC8	LCD_P28/ CMP0_IN2	LCD_P28/ CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4	I2S0_MCLK			LCD_P28
D6	85	—	—	PTC9	LCD_P29/ CMP0_IN3	LCD_P29/ CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5	I2S0_RX_ BCLK			LCD_P29
C6	86	—	—	PTC10	LCD_P30	LCD_P30	PTC10	I2C1_SCL		I2S0_RX_FS			LCD_P30
C5	87	—	—	PTC11	LCD_P31	LCD_P31	PTC11	I2C1_SDA		I2S0_RXD0			LCD_P31
B6	88	—	—	PTC12	LCD_P32	LCD_P32	PTC12			TPM_ CLKIN0			LCD_P32
A6	89	—	—	PTC13	LCD_P33	LCD_P33	PTC13			TPM_ CLKIN1			LCD_P33
D5	90	—	—	PTC16	LCD_P36	LCD_P36	PTC16						LCD_P36
C4	91	—	—	PTC17	LCD_P37	LCD_P37	PTC17						LCD_P37
B4	92	—	—	PTC18	LCD_P38	LCD_P38	PTC18						LCD_P38
D4	93	C3	57	PTD0	LCD_P40	LCD_P40	PTD0	SPI0_PCS0		TPM0_CH0			LCD_P40
D3	94	A4	58	PTD1	LCD_P41/ ADC0_SE5b	LCD_P41/ ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1			LCD_P41
C3	95	C2	59	PTD2	LCD_P42	LCD_P42	PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO		LCD_P42
B3	96	B3	60	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI		LCD_P43
A3	97	A3	61	PTD4/ LLWU_P14	LCD_P44	LCD_P44	PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4			LCD_P44

121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
A2	98	C1	62	PTD5	LCD_P45/ ADC0_SE6b	LCD_P45/ ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5			LCD_P45
B2	99	B2	63	PTD6/ LLWU_P15	LCD_P46/ ADC0_SE7b	LCD_P46/ ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	UART0_RX		SPI1_MISO		LCD_P46
A1	100	A2	64	PTD7	LCD_P47	LCD_P47	PTD7	SPI1_MISO	UART0_TX		SPI1_MOSI		LCD_P47
F1	10	—	—	NC	NC	NC							
F2	11	—	—	NC	NC	NC							
G1	12	—	—	NC	NC	NC							
G2	13	—	—	NC	NC	NC							
J3	—	—	—	NC	NC	NC							
H3	—	—	—	NC	NC	NC							
K4	—	—	—	NC	NC	NC							
L7	—	—	—	NC	NC	NC							
J9	—	—	—	NC	NC	NC							
J4	—	—	—	NC	NC	NC							
H11	—	—	—	NC	NC	NC							
F11	—	—	—	NC	NC	NC							
A5	—	—	—	NC	NC	NC							
B5	—	—	—	NC	NC	NC							
A4	—	—	—	NC	NC	NC							
B1	—	—	—	NC	NC	NC							
C2	—	—	—	NC	NC	NC							
C1	—	—	—	NC	NC	NC							
D2	—	—	—	NC	NC	NC							
D1	—	—	—	NC	NC	NC							
E1	—	—	—	NC	NC	NC							

5.2 KL36 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [KL36 Signal Multiplexing and Pin Assignments](#).

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	NC	NC	PTC13	PTC8	PTC4/ LLWU_P8	VLL1	VLL2	VLL3	A
B	NC	PTD6/ LLWU_P15	PTD3	PTC18	NC	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	VCAP2	B
C	NC	NC	PTD2	PTC17	PTC11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	VCAP1	C
D	NC	NC	PTD1	PTD0	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6/ RTC_CLKIN	PTB18	PTB10	PTB8	D
E	NC	PTE2	PTE1	PTE0	VDD	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	NC	NC	PTE6	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	NC	F
G	NC	NC	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	PTE16	PTE17	NC	PTA7	PTE24	PTE26	PTE4	PTA1	PTA3	PTA17	NC	H
J	PTE18	PTE19	NC	NC	PTE25	PTA0	PTA2	PTA4	NC	PTA16	PTA20	J
K	PTE20	PTE21	PTA6	NC	PTE30	VDD	PTA5	PTA12	PTA14	VSS	PTA19	K
L	PTE22	PTE23	PTE29	PTE31	VSS	VSS	NC	PTA13	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 23. KL36 121-pin BGA pinout diagram

	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	VCAP1	VLL2	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1	PTD6/ LLWU_P15	PTD3	VCAP2	VLL1	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2	PTD0	VSS	VLL3	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	C
D	PTE17	PTE19	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
E	PTE16	PTE18	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH	PTA4	PTA13	VDD	PTA19	G
H	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 25. KL36 64-pin BGA pinout diagram

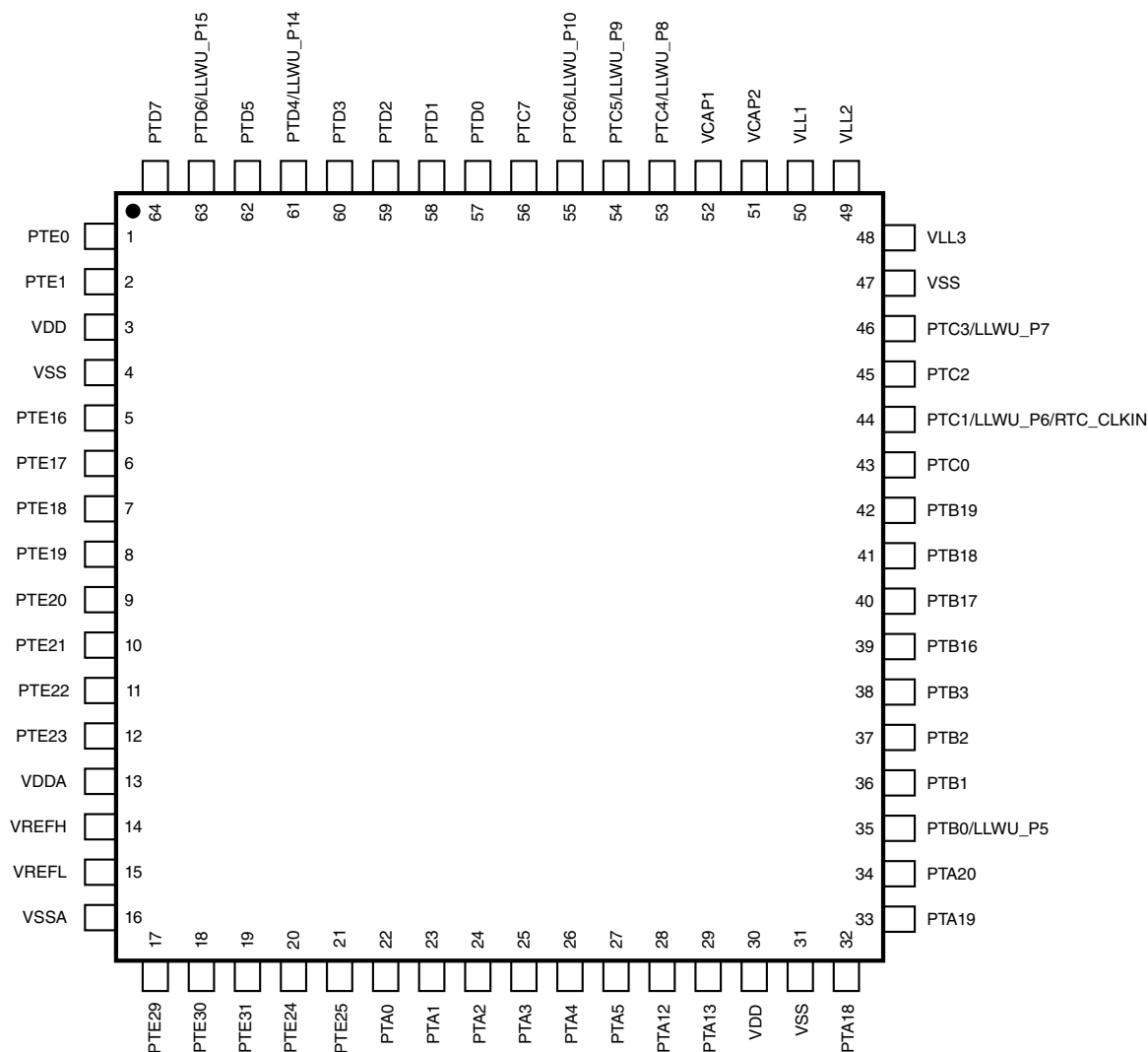


Figure 26. KL36 64-pin LQFP pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PKL36 and MKL36

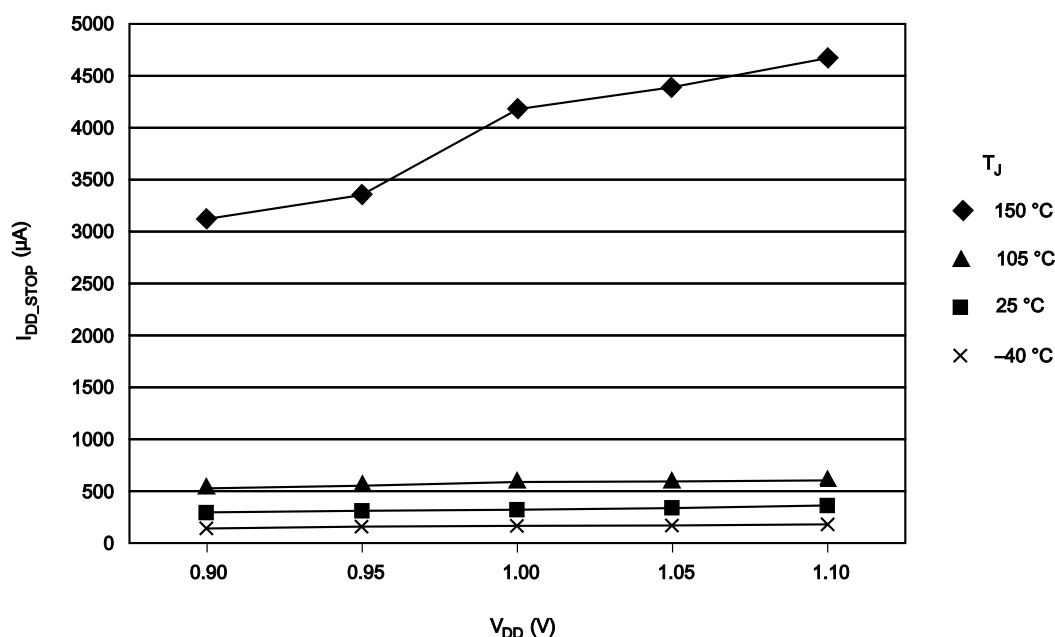
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 42. Typical value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision history

The following table provides a revision history for this document.

Table 43. Revision history

Rev. No.	Date	Substantial Changes
3	3/2014	- Updated the front page and restructured the chapters - Updated Voltage and current operating behaviors - Updated EMC radiated emissions operating behaviors - Updated Power mode transition operating behaviors - Updated Capacitance attributes - Updated footnote in the Device clock specifications - Added thermal attributes of 64-pin MAPBGA in the Thermal attributes - Added V_{REFH} and V_{REFL} in the 16-bit ADC electrical characteristics - Updated footnote to the V_{DACR} in the 12-bit DAC operating requirements - Added Inter-Integrated Circuit Interface (I2C) timing
4	5/2014	- Updated Power consumption operating behaviors - Updated Definition: Operating behavior
5	08/2014	- Updated related source in the front page - Updated Power consumption operating behaviors