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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D - 16bit; D/A - 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nexperia/mkl36z256vll4

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1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current	—	120	mA
V _{IO}	IO pin input voltage	-0.3	V _{DD} + 0.3	V
۱ _D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L=30 \text{ pF loads}$
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

Kinetis KL36 Sub-Family, Rev5 08/2014.



Voltage and current operating requirements 2.2.1

Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	
V _{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	
V _{IH}	Input high voltage				
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	$0.7 \times V_{DD}$	—	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	$0.75 \times V_{DD}$	—	V	
V _{IL}	Input low voltage				
	• 2.7 V \leq V _{DD} \leq 3.6 V	_	$0.35 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	—	$0.3 \times V_{DD}$	V	
V _{HYS}	Input hysteresis	$0.06 \times V_{DD}$	_	V	
I _{ICIO}	 IO pin negative DC injection current — single pin V_{IN} < V_{SS}-0.3V 	-3	_	mA	1
I _{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	_	mA	
V _{ODPU}	Open drain pullup voltage level	V _{DD}	V _{DD}	V	2
V _{RAM}	V _{DD} voltage required to retain RAM	1.2	_	V	

Table 5. Voltage and current operating requirements

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO MIN} - V_{IN})/|I_{ICIO}|$.

2. Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{POR}	Falling V _{DD} POR detect voltage	0.8	1.1	1.5	V	—
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1



Symbol	Description			٦	empera	ature (°0	C)		Unit
			-40	25	50	70	85	105	
I _{IREFSTEN4MHz}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.		56	56	56	56	56	56	μA
I _{IREFSTEN32KHz}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.		52	52	52	52	52	52	μA
I _{EREFSTEN4MHz}	External 4 MHz crystal clock a Measured by entering STOP o with the crystal enabled.	dder. r VLPS mode	206	228	237	245	251	258	μA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock	VLLS1	440	490	540	560	570	580	nA
	adder by means of the	VLLS3	440	490	540	560	570	580	
	EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	LLS	490	490	540	560	570	680	
		VLPS	510	560	560	560	610	680	
		STOP	510	560	560	560	610	680	1
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.		22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption		432	357	388	475	532	810	nA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μΑ
	115200 baud rate. Includes selected clock source power consumption.	OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I _{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	μΑ
	compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.	OSCERCLK (4 MHz external crystal)	235	256	265	274	280	287	

Table 10. Low power mode peripheral adders — typical value



Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	μA
I _{LCD}	LCD peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the OSC0_CR[EREFSTEN, EREFSTEN] bits. VIREG disabled, resistor bias network enabled, 1/8 duty cycle, 8 x 36 configuration for driving 288 Segments, 32 Hz frame rate, no LCD glass connected. Includes ERCLK32K (32 kHz external crystal) power consumption.	5	5	5	5	5	5	μA

 Table 10.
 Low power mode peripheral adders — typical value (continued)

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA





Figure 3. Run mode supply current vs. core frequency



3.1.1 SWD electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation			
	Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width			
	Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

Table 17. SWD full voltage range electricals



Figure 5. Serial wire clock input timing





Figure 6. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 18. MCG specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C	_	32.768	—	kHz	
f _{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	_	39.0625	kHz	
$\Delta_{fdco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM]	—	± 0.3	± 0.6	%f _{dco}	1



- 3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
- 4. When low power mode is selected, R_F is integrated and must not be attached externally.
- 5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications Table 20. Oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low- frequency mode (MCG_C2[RANGE]=00)	32	_	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high- frequency mode (low range) (MCG_C2[RANGE]=01)	3		8	MHz	
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8		32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	_	—	48	MHz	1, 2
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	_	750	_	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	_	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	_	0.6	_	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	_	1	_	ms	

- 1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
- 2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
- 3. Proper PC board layout procedures must be followed to achieve specifications.
- 4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.





Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
	ADC	• ADLPC = 1, ADHSC =	1.2	2.4	3.9	MHz	t _{ADACK} =
	asynchronous clock source	0	2.4	4.0	6.1	MHz	1/f _{ADACK}
		• ADLPC = 1, ADHSC =	3.0	5.2	7.3	MHz	
f _{ADACK}		• ADLPC = 0, ADHSC = 0	4.4	6.2	9.5	MHz	
		• ADLPC = 0, ADHSC = 1					
	Sample Time	See Reference Manual chapte	r for sample	times			
TUE	Total unadjusted	12-bit modes	—	±4	±6.8	LSB ⁴	5
	error	12-bit modes	—	±1.4	±2.1		
DNL	Differential non- linearity	12-bit modes	—	±0.7	-1.1 to +1.9	LSB ⁴	5
		<12-bit modes	_	±0.2	-0.3 to 0.5		

Table 26.	16-bit ADC	characteristics	(V _{REFH} =	V_{DDA} ,	$V_{REFL} = V$	V _{SSA})
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- 1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
- 2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{\text{REFH}} V_{\text{REFL}})/2^{N}$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- 8. ADC conversion clock < 3 MHz













Symbol	Description	Min.	Тур.	Max.	Unit
V _{DD}	Supply voltage	1.71	_	3.6	V
I _{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I _{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	_	_	20	μA
V _{AIN}	Analog input voltage	$V_{SS} - 0.3$	_	V _{DD}	V
V _{AIO}	Analog input offset voltage	_	_	20	mV
V _H	Analog comparator hysteresis ¹				
	 CR0[HYSTCTR] = 00 	—	5	—	mV
	• CR0[HYSTCTR] = 01	_	10	_	mV
	• CR0[HYSTCTR] = 10	_	20	_	mV
	 CR0[HYSTCTR] = 11 	—	30	_	mV
V _{CMPOh}	Output high	V _{DD} – 0.5	_	—	V
V _{CMPOI}	Output low	_	_	0.5	V
t _{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t _{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	_	_	40	μs
I _{DAC6b}	6-bit DAC current adder (enabled)	_	7	—	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3		0.3	LSB

3.6.2 CMP and 6-bit DAC electrical specifications Table 27. Comparator and 6-bit DAC electrical specifications

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD} -0.6 V.

 Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.

3. 1 LSB = V_{reference}/64



Peripheral operating requirements and behaviors



Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)



3.6.3.2 12-bit DAC operating behaviors Table 29. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA_DACL}	Supply current — low-power mode	_	—	250	μΑ	
I _{DDA_DACH}	Supply current — high-speed mode		—	900	μΑ	
t _{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode		100	200	μs	1
t _{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	_	15	30	μs	1
t _{CCDACLP}	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode		0.7	1	μs	1
V _{dacoutl}	DAC output voltage range low — high- speed mode, no load, DAC set to 0x000		—	100	mV	
V _{dacouth}	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V _{DACR} -100	_	V _{DACR}	mV	
INL	Integral non-linearity error — high speed mode	_	_	±8	LSB	2
DNL	Differential non-linearity error — V _{DACR} > 2 V		_	±1	LSB	3
DNL	Differential non-linearity error — V _{DACR} = VREF_OUT	_	_	±1	LSB	4
VOFFSET	Offset error	—	±0.4	±0.8	%FSR	5
E _G	Gain error	_	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \ge 2.4 V$	60	—	90	dB	
T _{CO}	Temperature coefficient offset voltage	—	3.7	_	μV/C	6
T _{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = $3 \text{ k}\Omega$)	—	—	250	Ω	
SR	Slew rate -80h \rightarrow F7Fh \rightarrow 80h				V/µs	
	 High power (SP_{HP}) 	1.2	1.7			
	 Low power (SP_{LP}) 	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	• High power (SP _{HP})	550	_	_		
	• Low power (SP _{LP})	40	-	—		

1. Settling within ± 1 LSB

2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV

3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV

4. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V 5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} – 100 mV

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

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1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI master mode timing (CPHA = 1)

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f _{op}	Frequency of operation	0	f _{periph} /4	Hz	1
2	t _{SPSCK}	SPSCK period	4 x t _{periph}	_	ns	2
3	t _{Lead}	Enable lead time	1	_	t _{periph}	
4	t _{Lag}	Enable lag time	1	—	t _{periph}	—
5	t _{WSPSCK}	Clock (SPSCK) high or low time	t _{periph} - 30	—	ns	—
6	t _{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t _{HI}	Data hold time (inputs)	3.5	—	ns	—
8	ta	Slave access time	—	t _{periph}	ns	3
9	t _{dis}	Slave MISO disable time	—	t _{periph}	ns	4
10	t _v	Data valid (after SPSCK edge)	_	31	ns	—
11	t _{HO}	Data hold time (outputs)	0	—	ns	—
12	t _{RI}	Rise time input	—	t _{periph} - 25	ns	—
	t _{FI}	Fall time input				
13	t _{RO}	Rise time output	_	25	ns	_
	t _{FO}	Fall time output				

Table 32. SPI slave mode timing on slew rate disabled pads

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).

- 2. $t_{periph} = 1/f_{periph}$
- 3. Time to data active from high-impedance state
- 4. Hold time to high-impedance state



3.8.4.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	_	15.5	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	_	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	19	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	26	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	_	ns







121 BGA	100 LQFP	64 BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
L9	45	_	_	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0	
J10	46	_	_	PTA16	DISABLED		PTA16	SPI0_MOSI			SPI0_MISO	I2S0_RX_FS	I2S0_RXD0
H10	47	_	_	PTA17	DISABLED		PTA17	SPI0_MISO			SPI0_MOSI	I2S0_MCLK	
L10	48	G7	30	VDD	VDD	VDD							
K10	49	H7	31	VSS	VSS	VSS							
L11	50	H8	32	PTA18	EXTAL0	EXTAL0	PTA18		UART1_RX	TPM_ CLKIN0			
K11	51	G8	33	PTA19	XTAL0	XTAL0	PTA19		UART1_TX	TPM_ CLKIN1		LPTMR0_ ALT1	
J11	52	F8	34	PTA20	RESET_b		PTA20						RESET_b
G11	53	F7	35	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8/ TSI0_CH0	LCD_P0/ ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				LCD_P0
G10	54	F6	36	PTB1	LCD_P1/ ADC0_SE9/ TSI0_CH6	LCD_P1/ ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	TPM1_CH1				LCD_P1
G9	55	E7	37	PTB2	LCD_P2/ ADC0_SE12/ TSI0_CH7	LCD_P2/ ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	TPM2_CH0				LCD_P2
G8	56	E8	38	PTB3	LCD_P3/ ADC0_SE13/ TSI0_CH8	LCD_P3/ ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	TPM2_CH1				LCD_P3
E11	57	-	_	PTB7	LCD_P7	LCD_P7	PTB7						LCD_P7
D11	58	-	-	PTB8	LCD_P8	LCD_P8	PTB8	SPI1_PCS0	EXTRG_IN				LCD_P8
E10	59	_	_	PTB9	LCD_P9	LCD_P9	PTB9	SPI1_SCK					LCD_P9
D10	60	-	-	PTB10	LCD_P10	LCD_P10	PTB10	SPI1_PCS0					LCD_P10
C10	61	_	_	PTB11	LCD_P11	LCD_P11	PTB11	SPI1_SCK					LCD_P11
B10	62	E6	39	PTB16	LCD_P12/ TSI0_CH9	LCD_P12/ TSI0_CH9	PTB16	SPI1_MOSI	UART0_RX	TPM_ CLKIN0	SPI1_MISO		LCD_P12
E9	63	D7	40	PTB17	LCD_P13/ TSI0_CH10	LCD_P13/ TSI0_CH10	PTB17	SPI1_MISO	UART0_TX	TPM_ CLKIN1	SPI1_MOSI		LCD_P13
D9	64	D6	41	PTB18	LCD_P14/ TSI0_CH11	LCD_P14/ TSI0_CH11	PTB18		TPM2_CH0	I2S0_TX_ BCLK			LCD_P14
C9	65	C7	42	PTB19	LCD_P15/ TSI0_CH12	LCD_P15/ TSI0_CH12	PTB19		TPM2_CH1	I2S0_TX_FS			LCD_P15
F10	66	-	-	PTB20	LCD_P16	LCD_P16	PTB20					CMP0_OUT	LCD_P16
F9	67	—	—	PTB21	LCD_P17	LCD_P17	PTB21						LCD_P17
F8	68	—	—	PTB22	LCD_P18	LCD_P18	PTB22						LCD_P18
E8	69	-	-	PTB23	LCD_P19	LCD_P19	PTB23						LCD_P19
B9	70	D8	43	PTC0	LCD_P20/ ADC0_SE14/ TSI0_CH13	LCD_P20/ ADC0_SE14/ TSI0_CH13	PTC0		EXTRG_IN	audioUSB_ SOF_OUT	CMP0_OUT	12S0_TXD0	LCD_P20
D8	71	C6	44	PTC1/ LLWU_P6/ RTC_CLKIN	LCD_P21/ ADC0_SE15/ TSI0_CH14	LCD_P21/ ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6/ RTC_CLKIN	12C1_SCL		TPM0_CH0		I2S0_TXD0	LCD_P21

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	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	NC	NC	PTC13	PTC8	PTC4/ LLWU_P8	VLL1	VLL2	VLL3	A
в	NC	PTD6/ LLWU_P15	PTD3	PTC18	NC	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	VCAP2	в
с	NC	NC	PTD2	PTC17	PTC11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	VCAP1	с
D	NC	NC	PTD1	PTD0	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6/ RTC_CLKIN	PTB18	PTB10	PTB8	D
E	NC	PTE2	PTE1	PTE0	VDD	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	NC	NC	PTE6	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	NC	F
G	NC	NC	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
н	PTE16	PTE17	NC	PTA7	PTE24	PTE26	PTE4	PTA1	PTA3	PTA17	NC	н
J	PTE18	PTE19	NC	NC	PTE25	PTA0	PTA2	PTA4	NC	PTA16	PTA20	J
к	PTE20	PTE21	PTA6	NC	PTE30	VDD	PTA5	PTA12	PTA14	VSS	PTA19	к
L	PTE22	PTE23	PTE29	PTE31	VSS	VSS	NC	PTA13	PTA15	VDD	PTA18	L
I	1	2	3	4	5	6	7	8	9	10	11	I

Figure 23. KL36 121-pin BGA pinout diagram





Figure 24. KL36 100-pin LQFP pinout diagram



	1	2	3	4	5	6	7	8	
А	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	VCAP1	VLL2	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
в	PTE1	PTD6/ LLWU_P15	PTD3	VCAP2	VLL1	PTC7	PTC2	PTC4/ LLWU_P8	в
с	PTD5	PTD2	PTD0	VSS	VLL3	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	с
D	PTE17	PTE19	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
Е	PTE16	PTE18	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH	PTA4	PTA13	VDD	PTA19	G
н	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	н
	1	2	3	4	5	6	7	8	

Figure 25. KL36 64-pin BGA pinout diagram





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