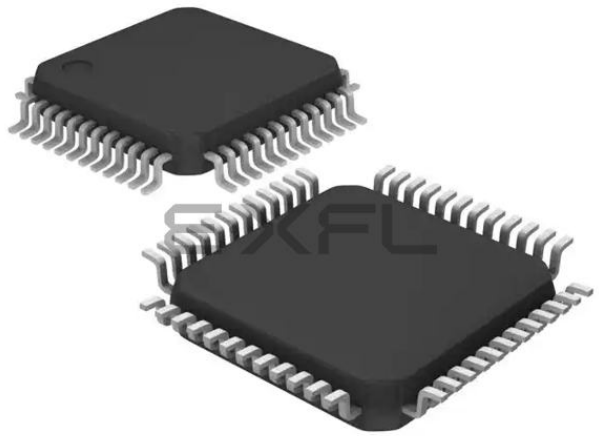

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1315fbd48-551

- Debug options:
  - Standard JTAG test interface for BSDL.
  - Serial Wire Debug.
  - Support for ETM ARM Cortex-M3 debug time stamping.
- Digital peripherals:
  - Up to 51 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, input inverter, and pseudo open-drain mode. Eight pins support programmable glitch filter.
  - Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - High-current source output driver (20 mA) on one pin (P0_7).
  - High-current sink driver (20 mA) on true open-drain pins (P0_4 and P0_5).
  - Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a internal low-power WatchDog Oscillator (WDO).
  - Repetitive Interrupt Timer (RI Timer).
- Analog peripherals:
  - 12-bit ADC with eight input channels and sampling rates of up to 500 kSamples/s.
- Serial interfaces:
  - USB 2.0 full-speed device controller (LPC1345/46/47) with on-chip ROM-based USB driver library.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator) with failure detector.
  - 12 MHz high-frequency Internal RC oscillator (IRC) trimmed to 1 % accuracy over the entire voltage and temperature range. The IRC can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB (LPC1345/46/47).
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Power profiles residing in boot ROM allow optimized performance and minimized power consumption for any given application through one simple function call.

6. Pinning information

6.1 Pinning

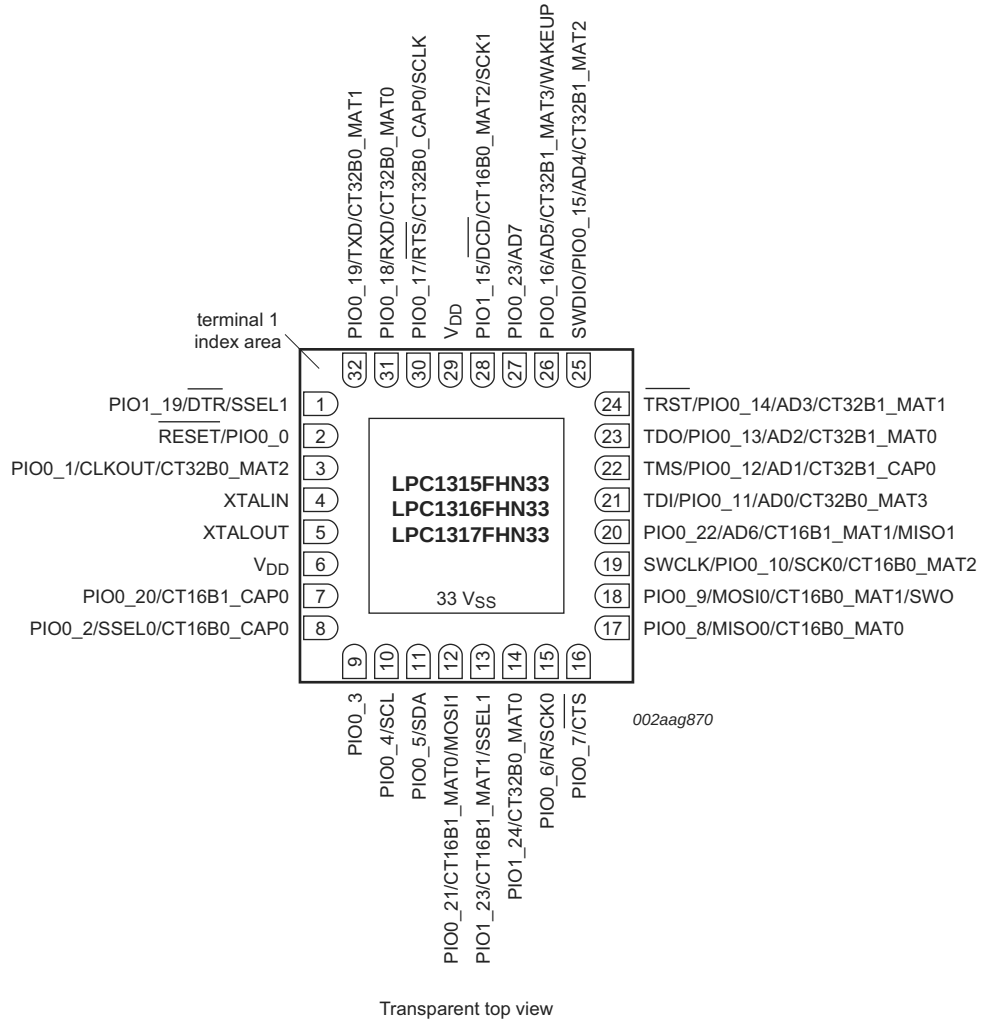
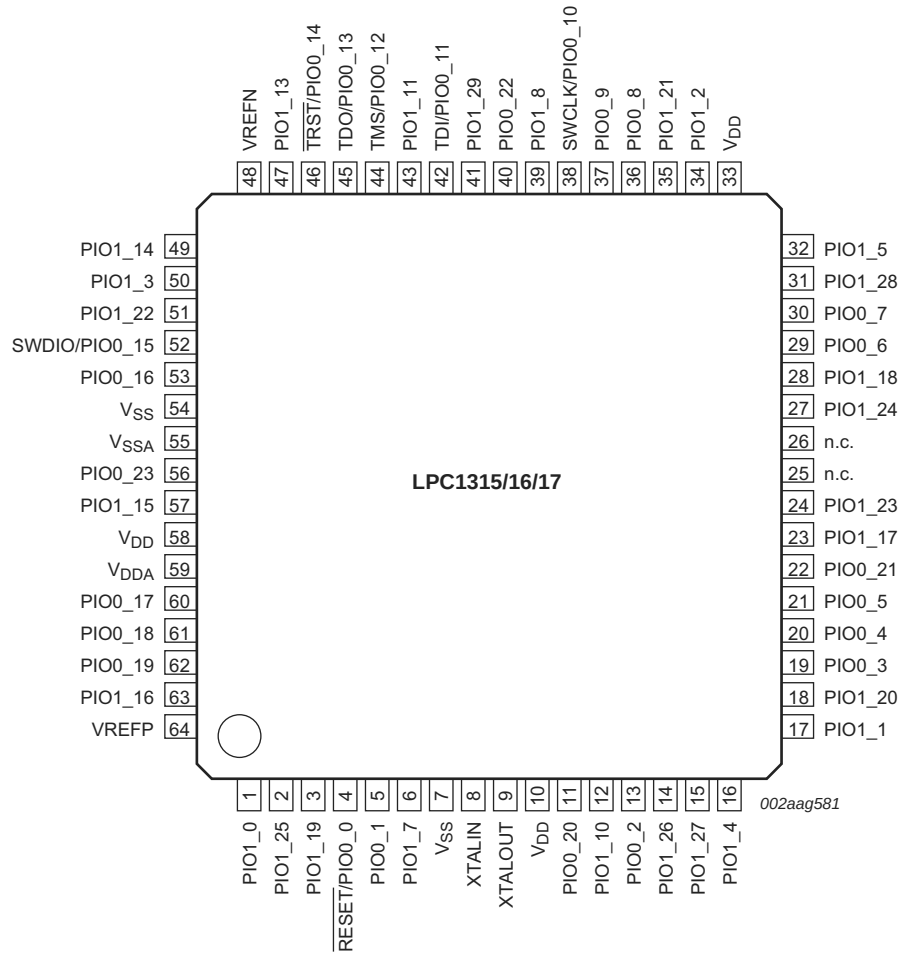


Fig 2. Pin configuration HVQFN33 package (LPC1315/16/17 - no USB)



See Table 3 for the full pin name.

Fig 6. Pin configuration LQFP64 package (LPC1315/16/17 - no USB)

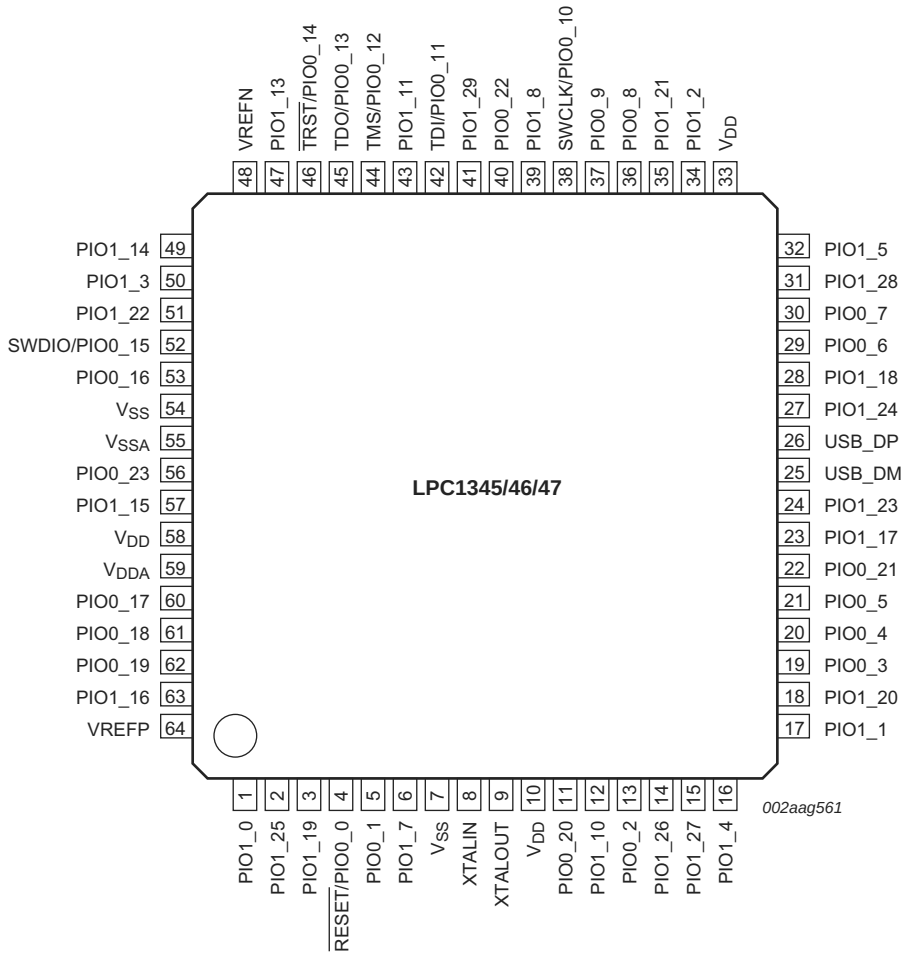


Fig 7. Pin configuration LQFP64 package (LPC1345/46/47 - with USB)

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO0_18/RXD/ CT32B0_MAT0	61	46	31	[3]	I; PU	I/O	**PIO0_18 —** General purpose digital input/output pin.
					-	I	**RXD —** Receiver input for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19/TXD/ CT32B0_MAT1	62	47	32	[3]	I; PU	I/O	**PIO0_19 —** General purpose digital input/output pin.
					-	O	**TXD —** Transmitter output for USART. Used in UART ISP mode.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20/CT16B1_CAP0	11	9	7	[3]	I; PU	I/O	**PIO0_20 —** General purpose digital input/output pin.
					-	I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO0_21/CT16B1_MAT0/ MOSI1	22	17	12	[3]	I; PU	I/O	**PIO0_21 —** General purpose digital input/output pin.
					-	O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
					-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO0_22/AD6/ CT16B1_MAT1/MISO1	40	30	20	[6]	I; PU	I/O	**PIO0_22 —** General purpose digital input/output pin.
					-	I	**AD6 —** A/D converter, input 6.
					-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO0_23/AD7	56	42	27	[6]	I; PU	I/O	**PIO0_23 —** General purpose digital input/output pin.
					-	I	**AD7 —** A/D converter, input 7.
PIO1_0/CT32B1_MAT0	1	-	-	[3]	I; PU	I/O	**PIO1_0 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
PIO1_1/CT32B1_MAT1	17	-	-	[3]	I; PU	I/O	**PIO1_1 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
PIO1_2/CT32B1_MAT2	34	-	-	[3]	I; PU	I/O	**PIO1_2 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_3/CT32B1_MAT3	50	-	-	[3]	I; PU	I/O	**PIO1_3 —** General purpose digital input/output pin.
					-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_4/CT32B1_CAP0	16	-	-	[3]	I; PU	I/O	**PIO1_4 —** General purpose digital input/output pin.
					-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
PIO1_5/CT32B1_CAP1	32	-	-	[3]	I; PU	I/O	**PIO1_5 —** General purpose digital input/output pin.
					-	I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
PIO1_7	6	-	-	[3]	I; PU	I/O	**PIO1_7 —** General purpose digital input/output pin.
PIO1_8	39	-	-	[3]	I; PU	I/O	**PIO1_8 —** General purpose digital input/output pin.
PIO1_10	12	-	-	[3]	I; PU	I/O	**PIO1_10 —** General purpose digital input/output pin.
PIO1_11	43	-	-	[3]	I; PU	I/O	**PIO1_11 —** General purpose digital input/output pin.

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO1_25/CT32B0_MAT1	2	1	-	[3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD	14	11	-	[3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_27/CT32B0_MAT3/ TXD	15	12	-	[3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
PIO1_28/CT32B0_CAP0/ SCLK	31	24	-	[3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	41	31	-	[3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	25	-	[3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
n.c.	25	19	-		-	-	Not connected.
n.c.	26	20	-		-	-	Not connected.
XTALIN	8	6	4	[8]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	9	7	5	[8]	-	-	Output from the oscillator amplifier.
V_{DDA}	59	-	-		-	-	Analog 3.3 V pad supply voltage: This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is used to power the ADC. This pin should be tied to 3.3 V if the ADC is not used.
VREFN	48	-	-		-	-	ADC negative reference voltage: This should be nominally the same voltage as V_{SS} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC.

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33	Reset state[1]	Type	Description
VREFP	64	-	-	-	-	ADC positive reference voltage: This should be nominally the same voltage as V_{DDA} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC. This pin should be tied to 3.3 V if the ADC is not used.
V_{SSA}	55	-	-	-	-	Analog ground: 0 V reference. This should nominally be the same voltage as V_{SS}Product data sheet but should be isolated to minimize noise and error.
V_{DD}	10; 33; 58	8; 44	6; 29	-	-	Supply voltage to the internal regulator and the external rail. On LQFP48 and HVQFN33 packages, this pin is also connected to the 3.3 V ADC supply and reference voltage.
V_{SS}	7; 54	5; 41	33	-	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] See Figure 33 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32).

[4] I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 32); includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes programmable digital input glitch filter.

[7] WAKEUP pin. 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 32); includes digital input glitch filter.

[8] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO0_9/MOSI0/ CT16B0_MAT1/ SWO	37	28	18	[3]	I; PU	I/O	**PIO0_9 —** General purpose digital input/output pin.
					-	I/O	**MOSI0 —** Master Out Slave In for SSP0.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	O	**SWO —** Serial wire trace output.
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	38	29	19	[3]	I; PU	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
					-	I/O	**PIO0_10 —** General purpose digital input/output pin.
					-	O	**SCK0 —** Serial clock for SSP0.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	42	32	21	[6]	I; PU	I	**TDI —** Test Data In for JTAG interface.
					-	I/O	**PIO0_11 —** General purpose digital input/output pin.
					-	I	**AD0 —** A/D converter, input 0.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/ CT32B1_CAP0	44	33	22	[6]	I; PU	I	**TMS —** Test Mode Select for JTAG interface.
					-	I/O	**PIO_12 —** General purpose digital input/output pin.
					-	I	**AD1 —** A/D converter, input 1.
					-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	45	34	23	[6]	I; PU	O	**TDO —** Test Data Out for JTAG interface.
					-	I/O	**PIO0_13 —** General purpose digital input/output pin.
					-	I	**AD2 —** A/D converter, input 2.
					-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	46	35	24	[6]	I; PU	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
					-	I/O	**PIO0_14 —** General purpose digital input/output pin.
					-	I	**AD3 —** A/D converter, input 3.
					-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	52	39	25	[6]	I; PU	I/O	**SWDIO —** Serial wire debug input/output.
					-	I/O	**PIO0_15 —** General purpose digital input/output pin.
					-	I	**AD4 —** A/D converter, input 4.
					-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO0_16/AD5/ CT32B1_MAT3/WAKEUP	53	40	26	[7]	I; PU	I/O	**PIO0_16 —** General purpose digital input/output pin.
					-	I	**AD5 —** A/D converter, input 5.
					-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
					-	I	**WAKEUP —** Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO1_10	12	-	-	[3]	I; PU	I/O	**PIO1_10 —** General purpose digital input/output pin.
PIO1_11	43	-	-	[3]	I; PU	I/O	**PIO1_11 —** General purpose digital input/output pin.
PIO1_13/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD	47	36	-	[3]	I; PU	I/O	**PIO1_13 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
PIO1_14/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD	49	37	-	[3]	I; PU	I/O	**PIO1_14 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					-	O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_15/$\overline{\text{DCD}}$/ CT16B0_MAT2/SCK1	57	43	28	[3]	I; PU	I/O	**PIO1_15 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
					-	I/O	**SCK1 —** Serial clock for SSP1.
PIO1_16/$\overline{\text{RI}}$/CT16B0_CAP0	63	48	-	[3]	I; PU	I/O	**PIO1_16 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{RI}}$ —** Ring Indicator input for USART.
					-	I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO1_17/CT16B0_CAP1/ RXD	23	-	-	[3]	I; PU	I/O	**PIO1_17 —** General purpose digital input/output pin.
					-	I	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_18/CT16B1_CAP1/ TXD	28	-	-	[3]	I; PU	I/O	**PIO1_18 —** General purpose digital input/output pin.
					-	I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
					-	O	**TXD —** Transmitter output for USART.
PIO1_19/$\overline{\text{DTR}}$/SSEL1	3	2	1	[3]	I; PU	I/O	**PIO1_19 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for USART.
					-	I/O	**SSEL1 —** Slave select for SSP1.
PIO1_20/$\overline{\text{DSR}}$/SCK1	18	13	-	[3]	I; PU	I/O	**PIO1_20 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DSR}}$ —** Data Set Ready input for USART.
					-	I/O	**SCK1 —** Serial clock for SSP1.
PIO1_21/$\overline{\text{DCD}}$/MISO1	35	26	-	[3]	I; PU	I/O	**PIO1_21 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for USART.
					-	I/O	**MISO1 —** Master In Slave Out for SSP1.
PIO1_22/$\overline{\text{RI}}$/MOSI1	51	38	-	[3]	I; PU	I/O	**PIO1_22 —** General purpose digital input/output pin.
					-	I	**$\overline{\text{RI}}$ —** Ring Indicator input for USART.
					-	I/O	**MOSI1 —** Master Out Slave In for SSP1.
PIO1_23/CT16B1_MAT1/ SSEL1	24	18	-	[3]	I; PU	I/O	**PIO1_23 —** General purpose digital input/output pin.
					-	O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
					-	I/O	**SSEL1 —** Slave select for SSP1.

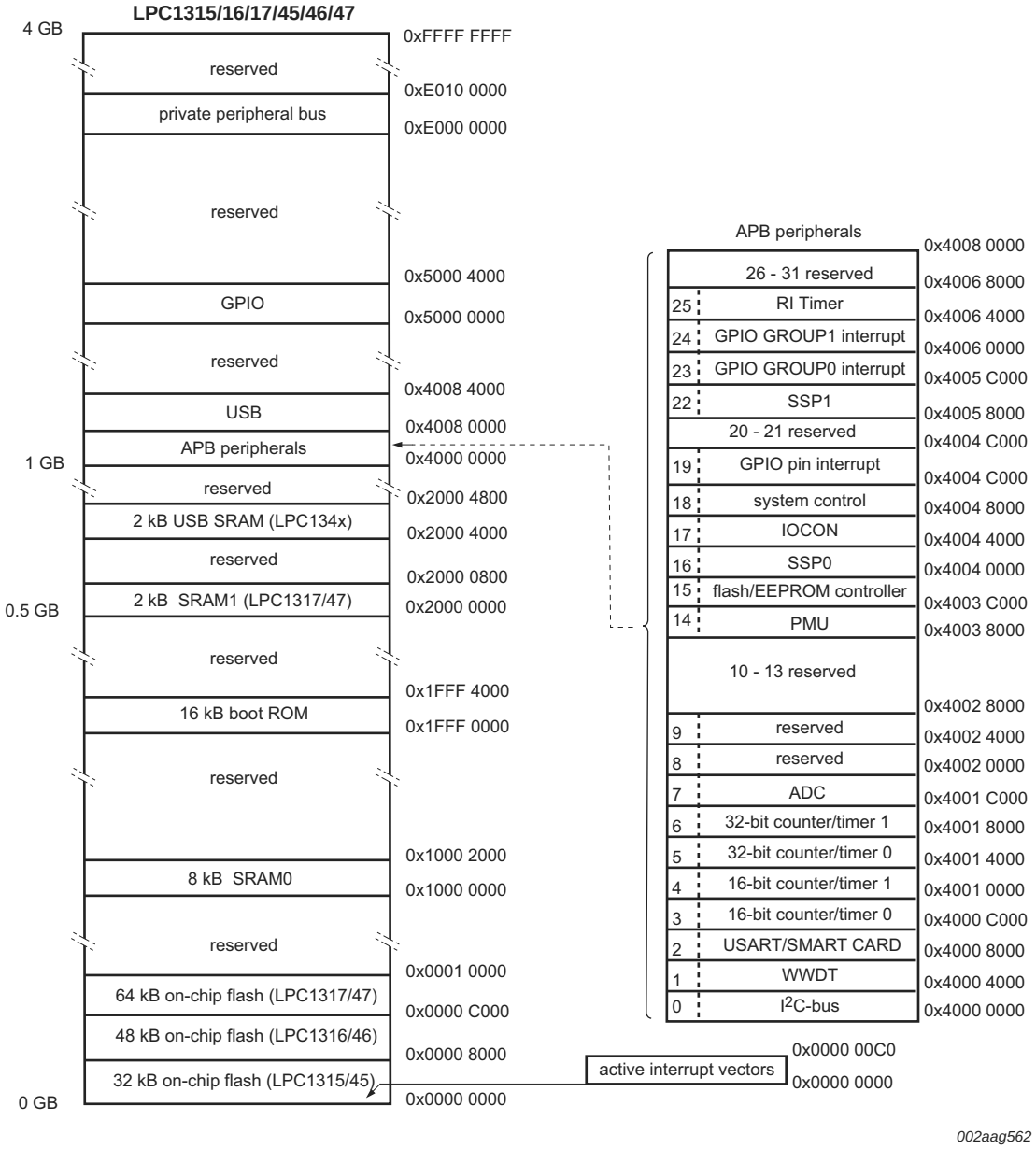


Fig 8. LPC1315/16/17/45/46/47 memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC1315/16/17/45/46/47, the NVIC supports up to 32 vectored interrupts.
- Eight programmable interrupt priority levels with hardware priority level masking.

- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

7.7 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable 10-ns glitch filter on pins PIO0_22, PIO0_23, and PIO0_11 to PIO0_16. The glitch filter is turned off by default.
- Programmable hysteresis.
- Programmable input inverter.

7.8 General Purpose Input/Output GPIO

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC1315/16/17/45/46/47 use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Any GPIO pin providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

The GPIO block consists of three parts:

1. The GPIO ports.
2. The GPIO pin interrupt block to control eight GPIO pins selected as pin interrupts.
3. Two GPIO group interrupt blocks to control two combined interrupts from all GPIO pins.

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	μA
		2.0 V < V_{DD} ≤ 3.6 V					
		V_{DD} = 2.0 V		−10	−50	−85	μA
		V_{DD} < V_I < 5 V		0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins		3.5	-	-	mA
		2.5 V ≤ V_{DD} ≤ 3.6 V					
		2.0 V ≤ V_{DD} < 2.5 V		3.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins		20	-	-	mA
		2.5 V ≤ V_{DD} ≤ 3.6 V					
		2.0 V ≤ V_{DD} < 2.5 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[16]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[2]	-	-	±10	μA
V_{BUS}	bus supply voltage		[2]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[2]	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	[2]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[2]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage	for low-/full-speed; R_L of 1.5 kΩ to 3.6 V	[2]	-	-	0.18	V
V_{OH}	HIGH-level output voltage	driven; for low-/full-speed; R_L of 15 kΩ to GND	[2]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[2]	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[17][2]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For USB operation 3.0 V ≤ V_{DD} ≤ 3.6 V. Guaranteed by design.

10. Dynamic characteristics

10.1 Flash/EEPROM memory

Table 9. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 10. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency		200	375	400	kHz
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		unpowered	150	300	-	years
t_{er}	erase time	64 bytes	-	1.8	-	ms
t_{prog}	programming time	64 bytes	-	1.1	-	ms

10.2 External clock

Table 11. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

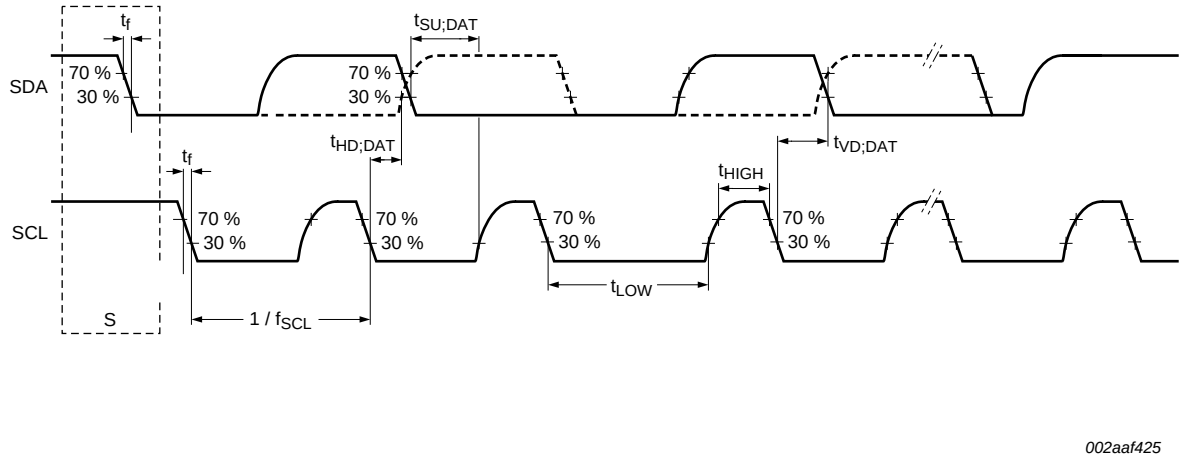


Fig 24. I^2C-bus pins clock timing

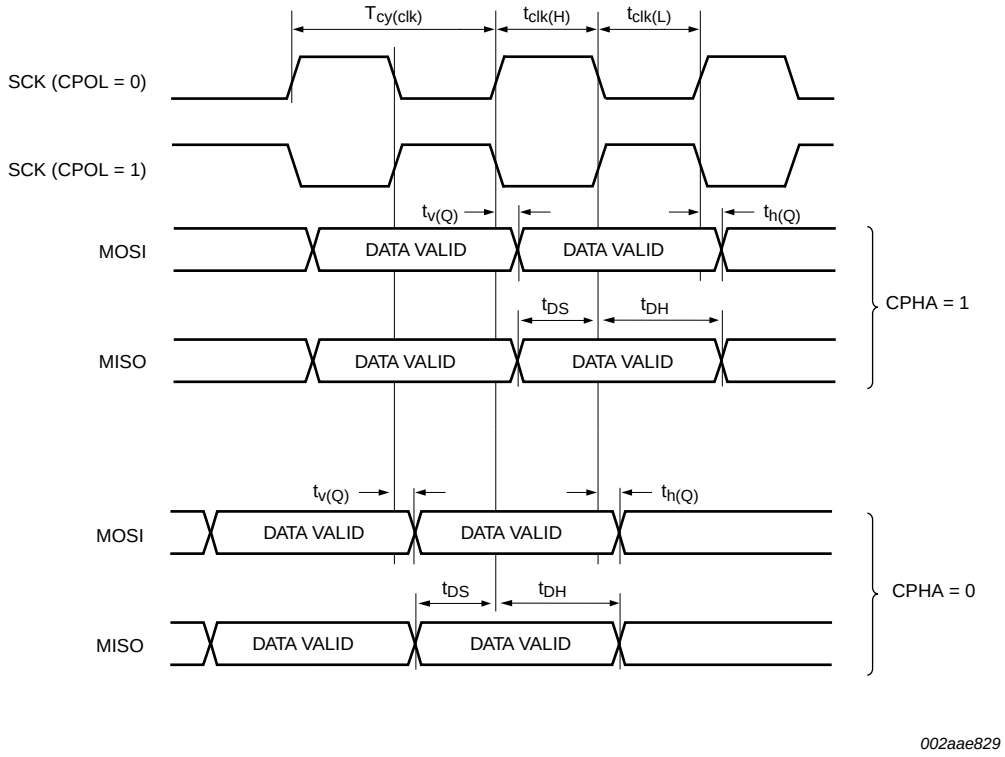


Fig 25. SSP master timing in SPI mode

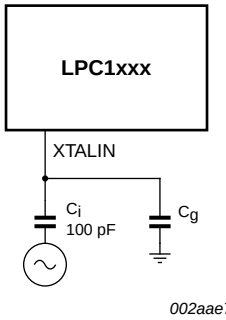


Fig 30. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 30), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 31 and in Table 18 and Table 19. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 31 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

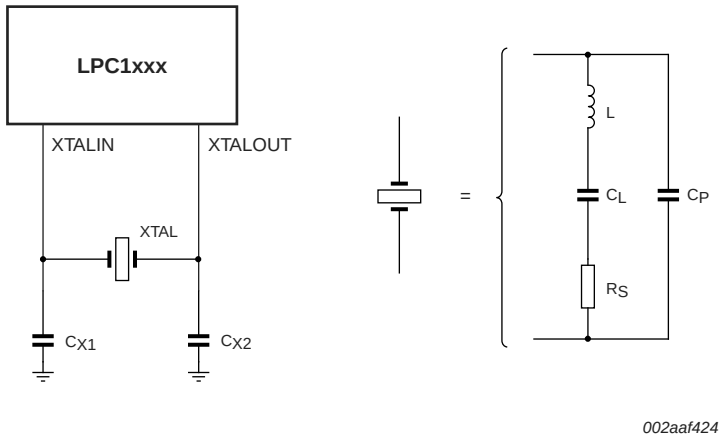


Fig 31. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF

12.5 Reset pad configuration

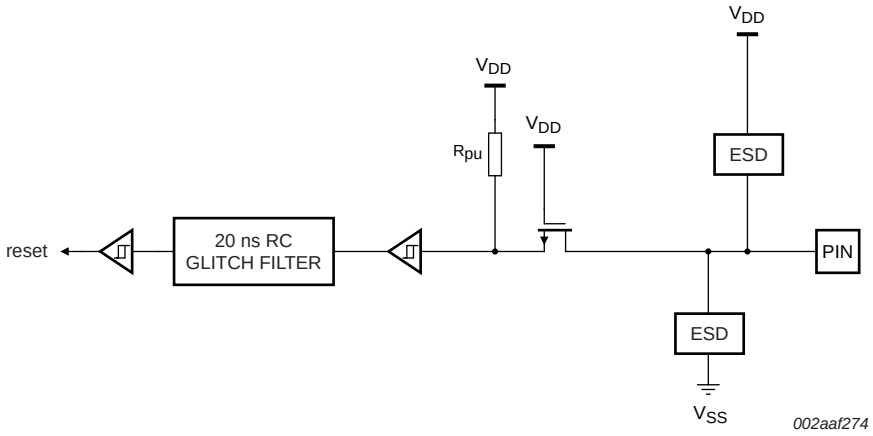


Fig 33. Reset pad configuration

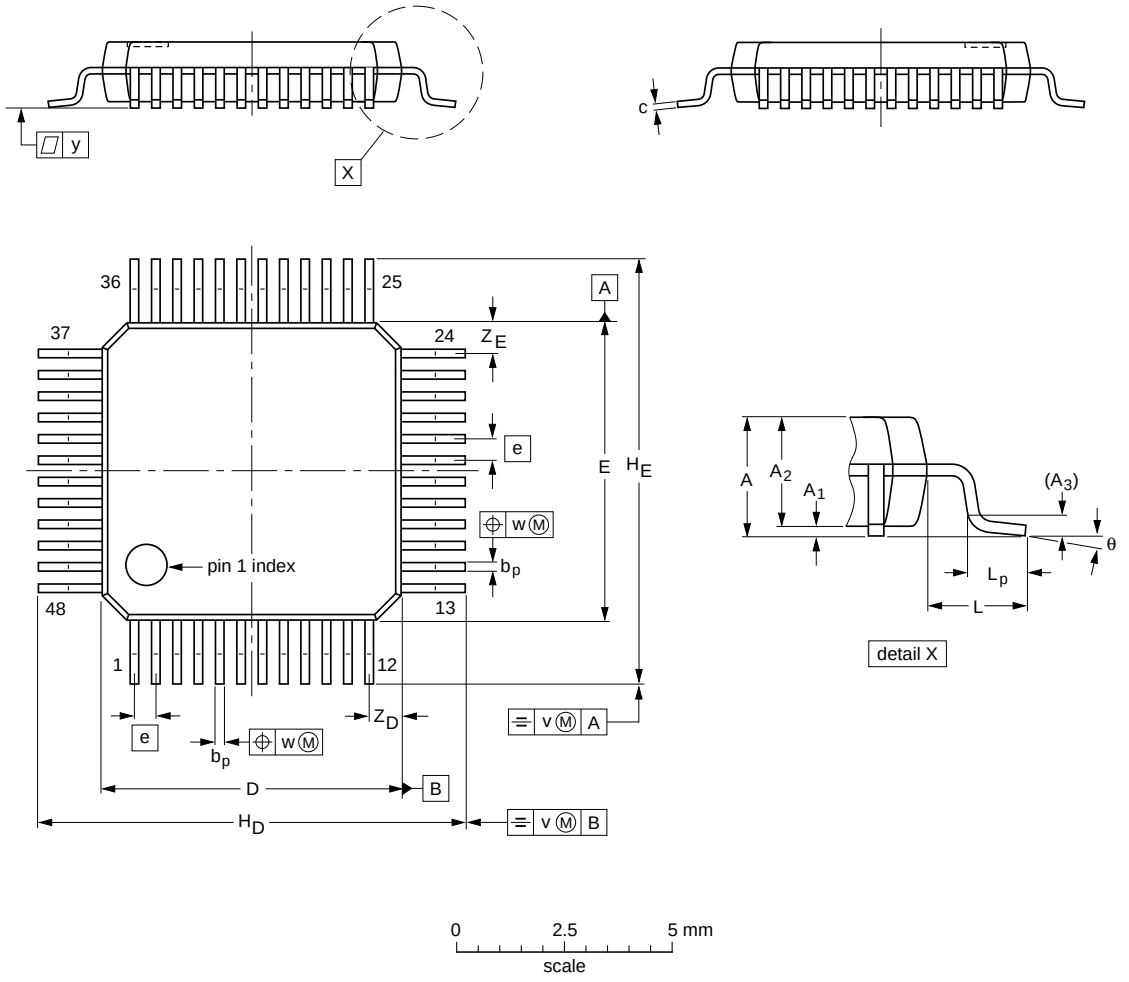
12.6 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 17:

- The ADC input trace must be short and as close as possible to the LPC1315/16/17/45/46/47 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

Remark: On the LQFP64 package, the analog power supply and the reference voltage can be connected on separate pins for better noise immunity.

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 35. Package outline LQFP48 (SOT313-2)

14. Soldering

Footprint information for reflow soldering of HVQFN33 package

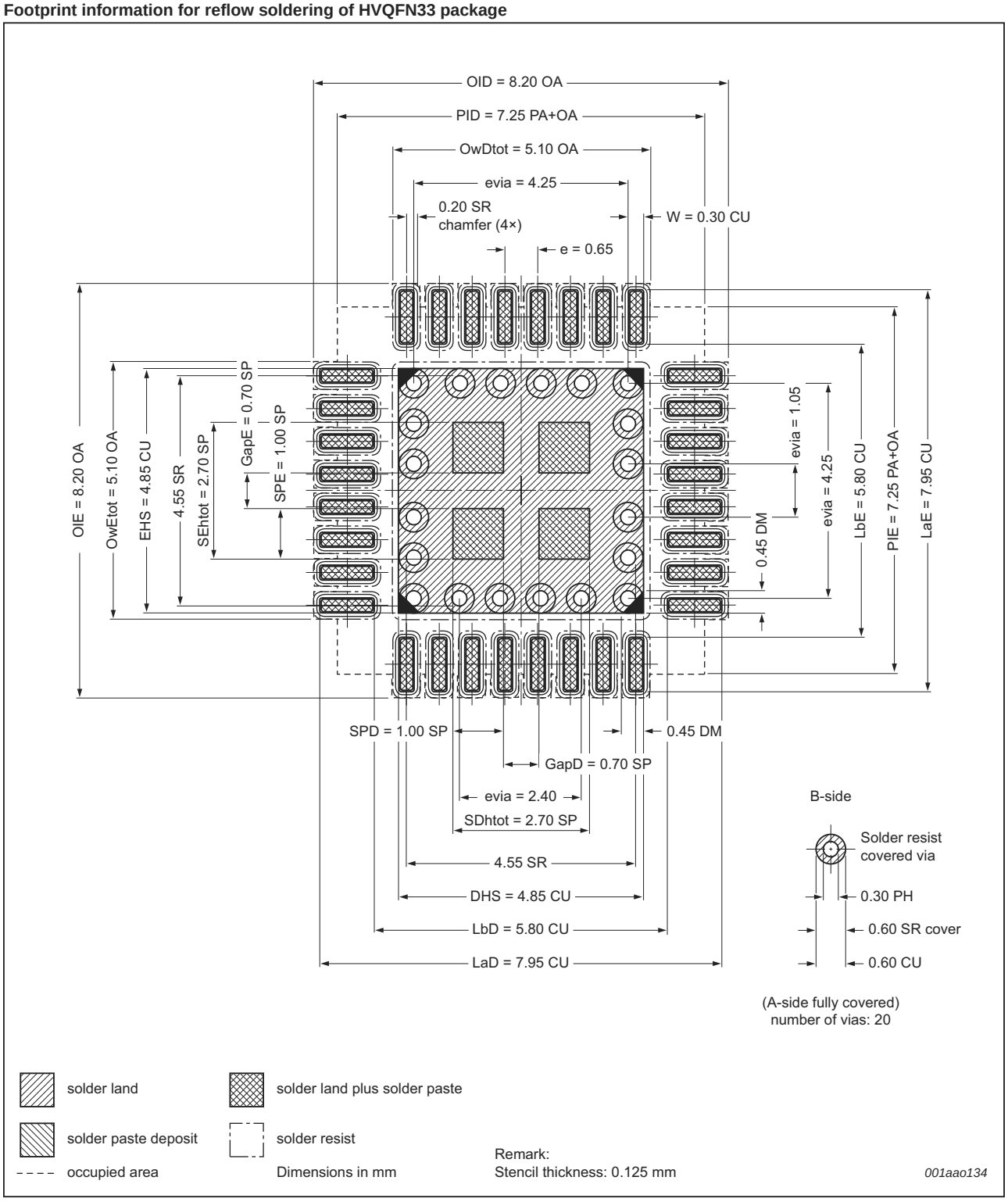
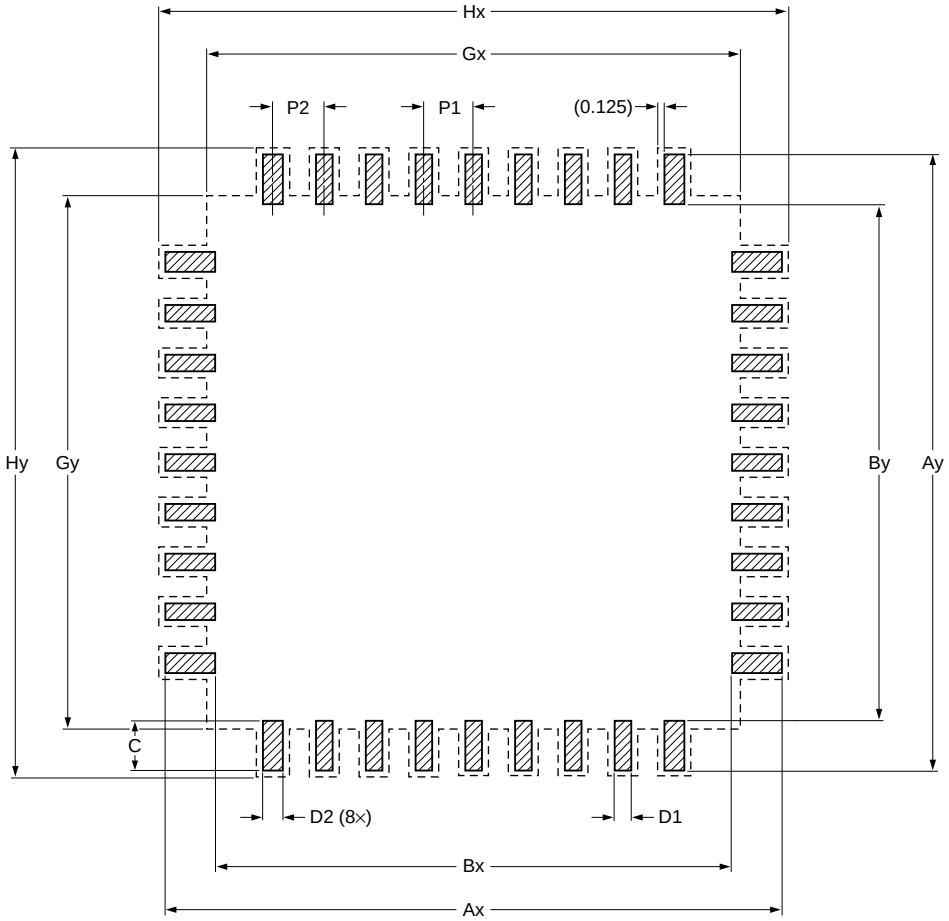


Fig 37. Reflow soldering of the HVQFN33 package

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 39. Reflow soldering of the LQFP64 package