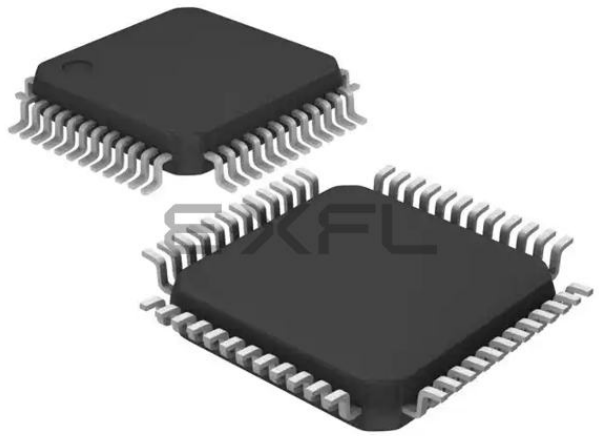

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	40
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1316fbd48-551

- Debug options:
  - Standard JTAG test interface for BSDL.
  - Serial Wire Debug.
  - Support for ETM ARM Cortex-M3 debug time stamping.
- Digital peripherals:
  - Up to 51 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, repeater mode, input inverter, and pseudo open-drain mode. Eight pins support programmable glitch filter.
  - Up to 8 GPIO pins can be selected as edge and level sensitive interrupt sources.
  - Two GPIO grouped interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - High-current source output driver (20 mA) on one pin (P0_7).
  - High-current sink driver (20 mA) on true open-drain pins (P0_4 and P0_5).
  - Four general purpose counter/timers with a total of up to 8 capture inputs and 13 match outputs.
  - Programmable Windowed WatchDog Timer (WWDT) with a internal low-power WatchDog Oscillator (WDO).
  - Repetitive Interrupt Timer (RI Timer).
- Analog peripherals:
  - 12-bit ADC with eight input channels and sampling rates of up to 500 kSamples/s.
- Serial interfaces:
  - USB 2.0 full-speed device controller (LPC1345/46/47) with on-chip ROM-based USB driver library.
  - USART with fractional baud rate generation, internal FIFO, a full modem control handshake interface, and support for RS-485/9-bit mode and synchronous mode. USART supports an asynchronous smart card interface (ISO 7816-3).
  - Two SSP controllers with FIFO and multi-protocol capabilities.
  - I^2C-bus interface supporting the full I^2C-bus specification and Fast-mode Plus with a data rate of up to 1 Mbit/s with multiple address recognition and monitor mode.
- Clock generation:
  - Crystal Oscillator with an operating range of 1 MHz to 25 MHz (system oscillator) with failure detector.
  - 12 MHz high-frequency Internal RC oscillator (IRC) trimmed to 1 % accuracy over the entire voltage and temperature range. The IRC can optionally be used as a system clock.
  - Internal low-power, low-frequency WatchDog Oscillator (WDO) with programmable frequency output.
  - PLL allows CPU operation up to the maximum CPU rate with the system oscillator or the IRC as clock sources.
  - A second, dedicated PLL is provided for USB (LPC1345/46/47).
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Power profiles residing in boot ROM allow optimized performance and minimized power consumption for any given application through one simple function call.

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
SWCLK/PIO0_10/SCK0/ CT16B0_MAT2	38	29	19	[3]	I; PU	I	**SWCLK —** Serial wire clock and test clock TCK for JTAG interface.
					-	I/O	**PIO0_10 —** General purpose digital input/output pin.
					-	O	**SCK0 —** Serial clock for SSP0.
					-	O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
TDI/PIO0_11/AD0/ CT32B0_MAT3	42	32	21	[6]	I; PU	I	**TDI —** Test Data In for JTAG interface.
					-	I/O	**PIO0_11 —** General purpose digital input/output pin.
					-	I	**AD0 —** A/D converter, input 0.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
TMS/PIO0_12/AD1/ CT32B1_CAP0	44	33	22	[6]	I; PU	I	**TMS —** Test Mode Select for JTAG interface.
					-	I/O	**PIO_12 —** General purpose digital input/output pin.
					-	I	**AD1 —** A/D converter, input 1.
					-	I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
TDO/PIO0_13/AD2/ CT32B1_MAT0	45	34	23	[6]	I; PU	O	**TDO —** Test Data Out for JTAG interface.
					-	I/O	**PIO0_13 —** General purpose digital input/output pin.
					-	I	**AD2 —** A/D converter, input 2.
					-	O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
$\overline{\text{TRST}}$/PIO0_14/AD3/ CT32B1_MAT1	46	35	24	[6]	I; PU	I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
					-	I/O	**PIO0_14 —** General purpose digital input/output pin.
					-	I	**AD3 —** A/D converter, input 3.
					-	O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO0_15/AD4/ CT32B1_MAT2	52	39	25	[6]	I; PU	I/O	**SWDIO —** Serial wire debug input/output.
					-	I/O	**PIO0_15 —** General purpose digital input/output pin.
					-	I	**AD4 —** A/D converter, input 4.
					-	O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO0_16/AD5/ CT32B1_MAT3/WAKEUP	53	40	26	[7]	I; PU	I/O	**PIO0_16 —** General purpose digital input/output pin.
					-	I	**AD5 —** A/D converter, input 5.
					-	O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
					-	I	**WAKEUP —** Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
PIO0_17/$\overline{\text{RTS}}$/ CT32B0_CAP0/SCLK	60	45	30	[3]	I; PU	I/O	**PIO0_17 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{RTS}}$ —** Request To Send output for USART.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.

Table 3. Pin description (LPC1315/16/17 - no USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
PIO1_25/CT32B0_MAT1	2	1	-	[3]	I; PU	I/O	**PIO1_25 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_26/CT32B0_MAT2/ RXD	14	11	-	[3]	I; PU	I/O	**PIO1_26 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	I	**RXD —** Receiver input for USART.
PIO1_27/CT32B0_MAT3/ TXD	15	12	-	[3]	I; PU	I/O	**PIO1_27 —** General purpose digital input/output pin.
					-	O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
					-	O	**TXD —** Transmitter output for USART.
PIO1_28/CT32B0_CAP0/ SCLK	31	24	-	[3]	I; PU	I/O	**PIO1_28 —** General purpose digital input/output pin.
					-	I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
					-	I/O	**SCLK —** Serial clock input/output for USART in synchronous mode.
PIO1_29/SCK0/ CT32B0_CAP1	41	31	-	[3]	I; PU	I/O	**PIO1_29 —** General purpose digital input/output pin.
					-	I/O	**SCK0 —** Serial clock for SSP0.
					-	I	**CT32B0_CAP1 —** Capture input 1 for 32-bit timer 0.
PIO1_31	-	25	-	[3]	I; PU	I/O	**PIO1_31 —** General purpose digital input/output pin.
n.c.	25	19	-		-	-	Not connected.
n.c.	26	20	-		-	-	Not connected.
XTALIN	8	6	4	[8]	-	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	9	7	5	[8]	-	-	Output from the oscillator amplifier.
V_{DDA}	59	-	-		-	-	Analog 3.3 V pad supply voltage: This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is used to power the ADC. This pin should be tied to 3.3 V if the ADC is not used.
VREFN	48	-	-		-	-	ADC negative reference voltage: This should be nominally the same voltage as V_{SS} but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC.

Table 4. Pin description (LPC1345/46/47 - with USB)

Symbol	LQFP64	LQFP48	HVQFN33		Reset state[1]	Type	Description
$\overline{\text{RESET}}$/PIO0_0	4	3	2	[2]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
					-	I/O	**PIO0_0 —** General purpose digital input/output pin.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	5	4	3	[3]	I; PU	I/O	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration.
					-	O	**CLKOUT —** Clockout pin.
					-	O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
					-	O	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal.
PIO0_2/SSEL0/ CT16B0_CAP0	13	10	8	[3]	I; PU	I/O	**PIO0_2 —** General purpose digital input/output pin.
						I/O	**SSEL0 —** Slave select for SSP0.
						I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	19	14	9	[3]	I; PU	I/O	**PIO0_3 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler. A HIGH level during reset starts the USB device enumeration.
					-	I	**USB_VBUS —** Monitors the presence of USB bus power.
PIO0_4/SCL	20	15	10	[4]	IA	I/O	**PIO0_4 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	21	16	11	[4]	IA	I/O	**PIO0_5 —** General purpose digital input/output pin (open-drain).
					-	I/O	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/$\overline{\text{USB_CONNECT}}$/ SCK0	29	22	15	[3]	I; PU	I/O	**PIO0_6 —** General purpose digital input/output pin.
					-	O	**$\overline{\text{USB_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
					-	I/O	**SCK0 —** Serial clock for SSP0.
PIO0_7/$\overline{\text{CTS}}$	30	23	16	[5]	I; PU	I/O	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
					-	I	**$\overline{\text{CTS}}$ —** Clear To Send input for USART.
PIO0_8/MISO0/ CT16B0_MAT0	36	27	17	[3]	I; PU	I/O	**PIO0_8 —** General purpose digital input/output pin.
					-	I/O	**MISO0 —** Master In Slave Out for SSP0.
					-	O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.

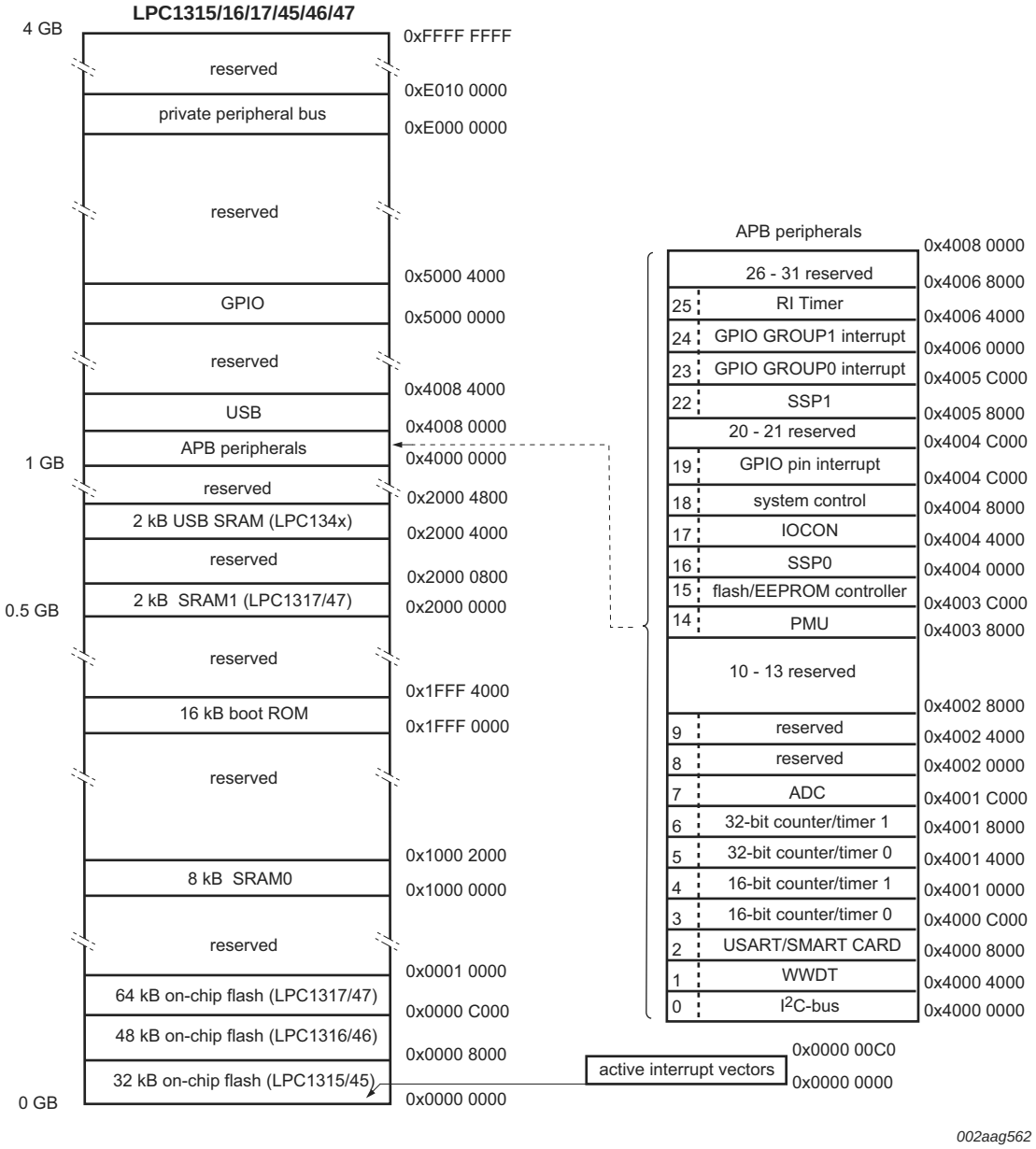


Fig 8. LPC1315/16/17/45/46/47 memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC1315/16/17/45/46/47, the NVIC supports up to 32 vectored interrupts.
- Eight programmable interrupt priority levels with hardware priority level masking.

The USART includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- Maximum USART data bit rate of 3.125 Mbit/s.
- 16-byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface (ISO 7816-3).

7.11 SSP serial I/O controller

The SSP controllers are capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I^2C-bus serial I/O controller

The LPC1315/16/17/45/46/47 contain one I^2C-bus controller.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or

7.14.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.

7.15 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 48-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.15.1 Features

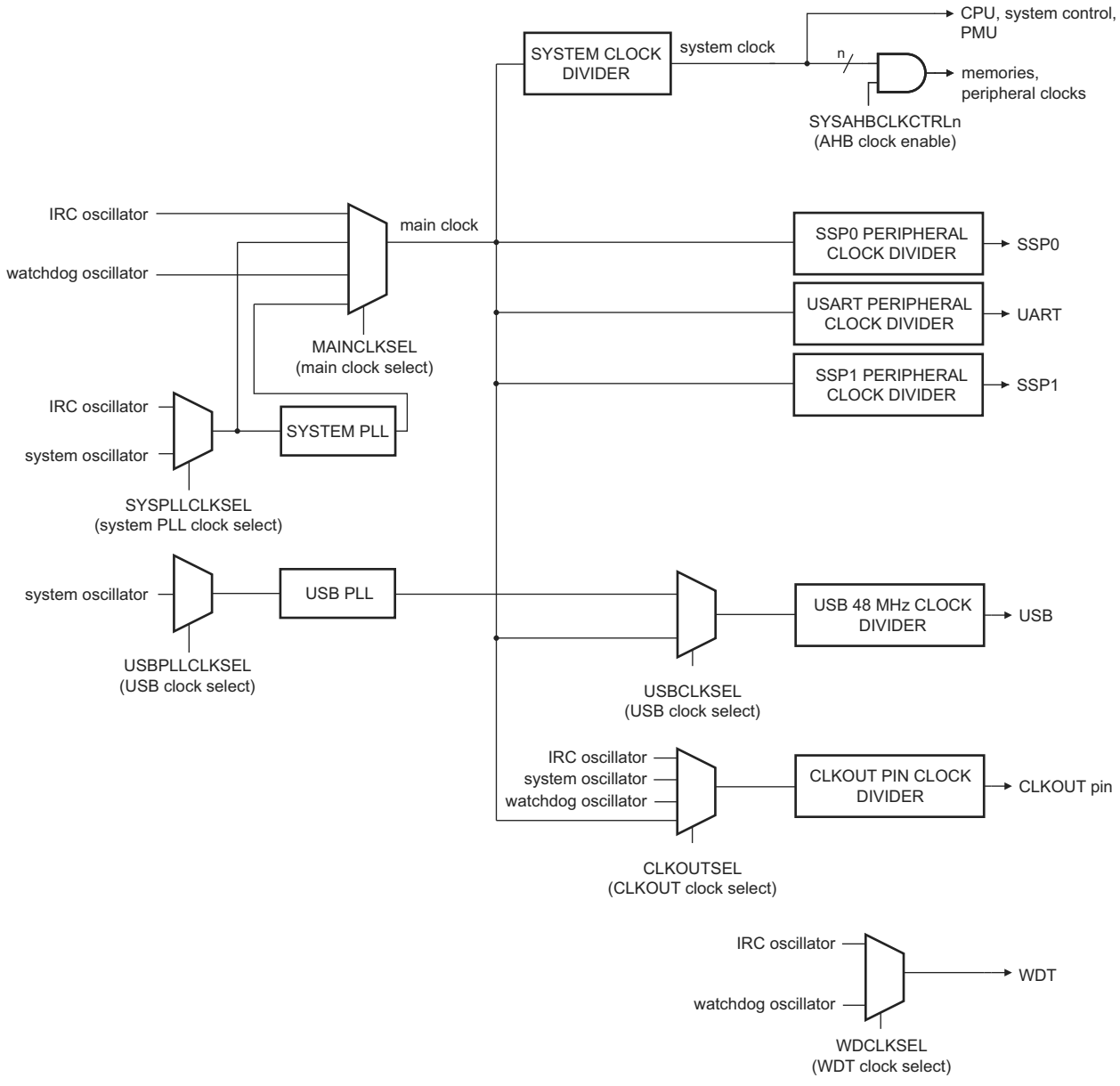
- 48-bit counter running from the main clock. Counter can be free-running or can be reset when an RIT interrupt is generated.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.
- Support for ETM timestamp generator.

7.16 System tick timer

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.17 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.



The USB clock divider is available on parts LPC1345/46/47 only.

Fig 9. LPC1315/16/17/45/46/47 clocking generation block diagram

7.18.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

7.18.6.3 Code security (Code Read Protection - CRP)

This feature of the LPC1315/16/17/45/46/47 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the LPC1315/16/17/45/46/47 *user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the LPC1315/16/17/45/46/47 *user manual*.

7.18.6.4 APB interface

The APB peripherals are located on one APB bus.

7.18.6.5 AHBLite

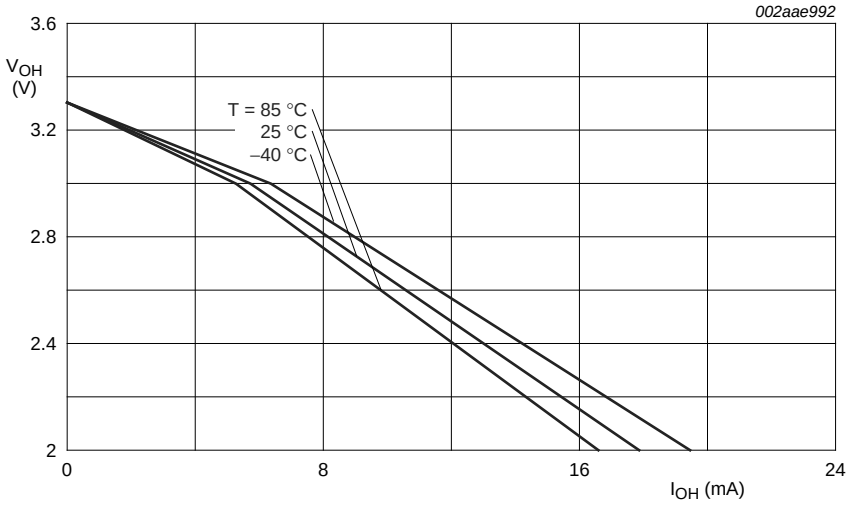
The AHBLite connects the CPU bus of the ARM Cortex-M3 to the flash memory, the main static RAM, and the ROM.

7.18.6.6 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs.

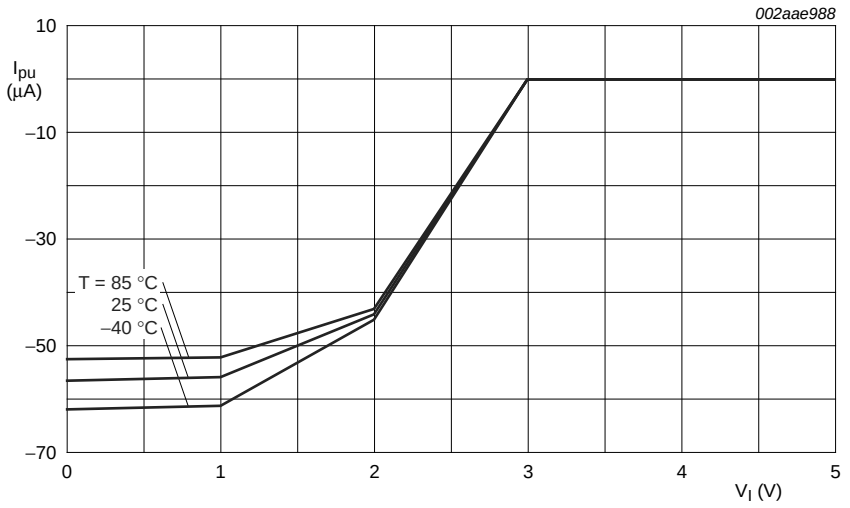
7.19 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M3. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0 is configured to support up to four breakpoints and two watch points.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 19. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 20. Typical pull-up current I_{pu} versus input voltage V_I

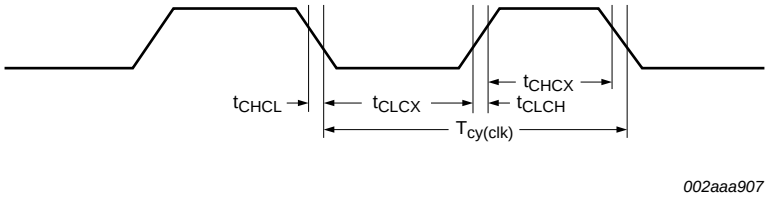


Fig 22. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

10.4 I/O pins

Table 14. Dynamic characteristics: I/O pins[1]
T_{amb} = −40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.5 I²C-bus

Table 15. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

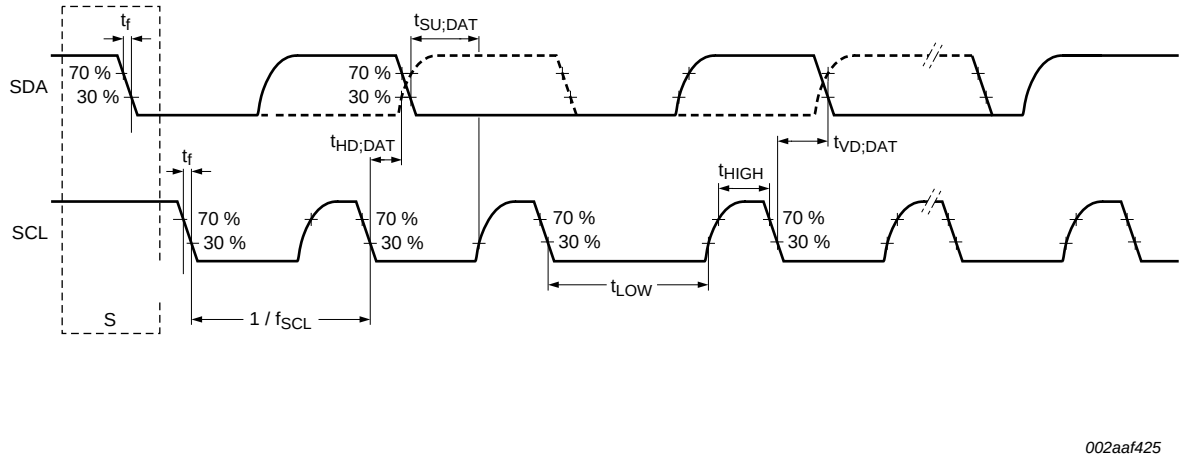


Fig 24. I^2C-bus pins clock timing

Table 18. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

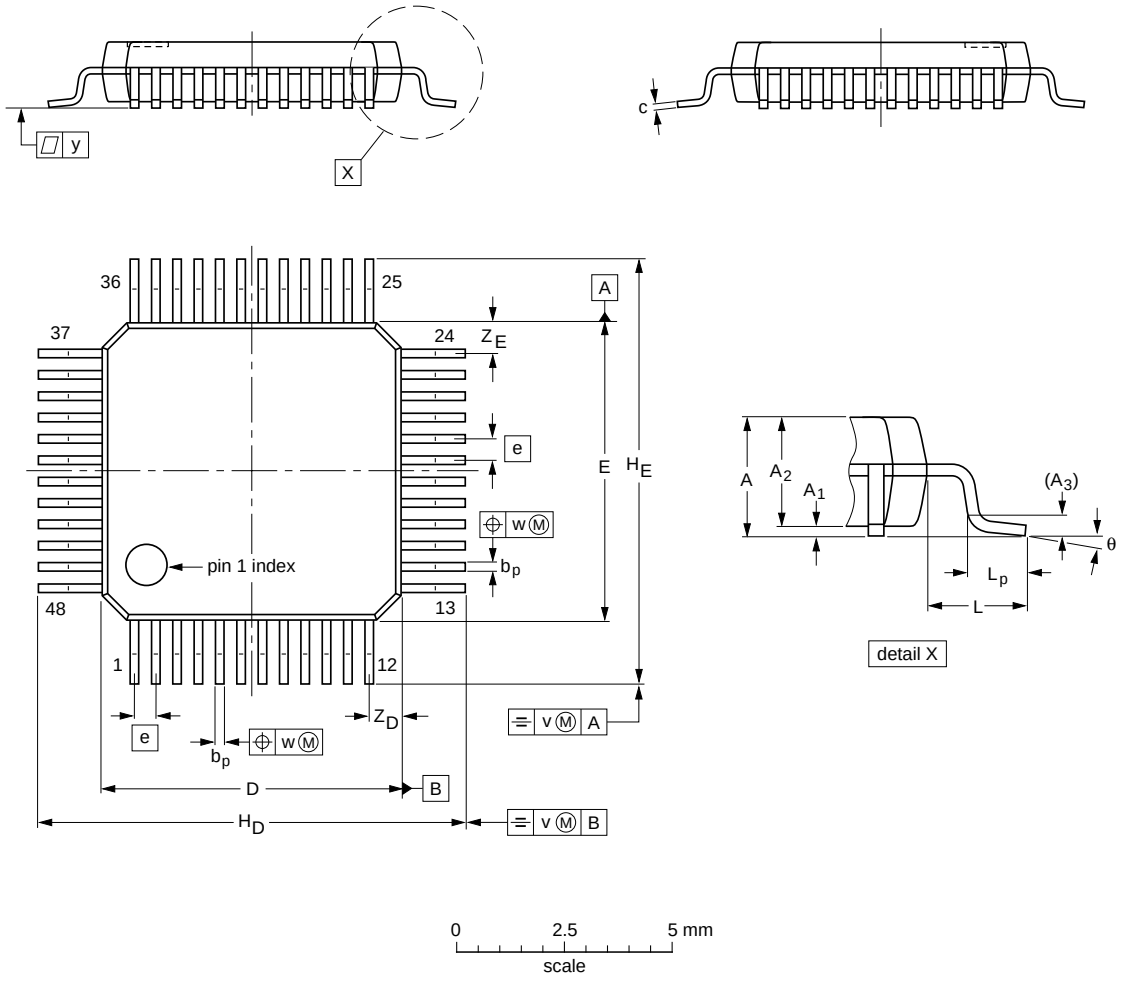
Table 19. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

12.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

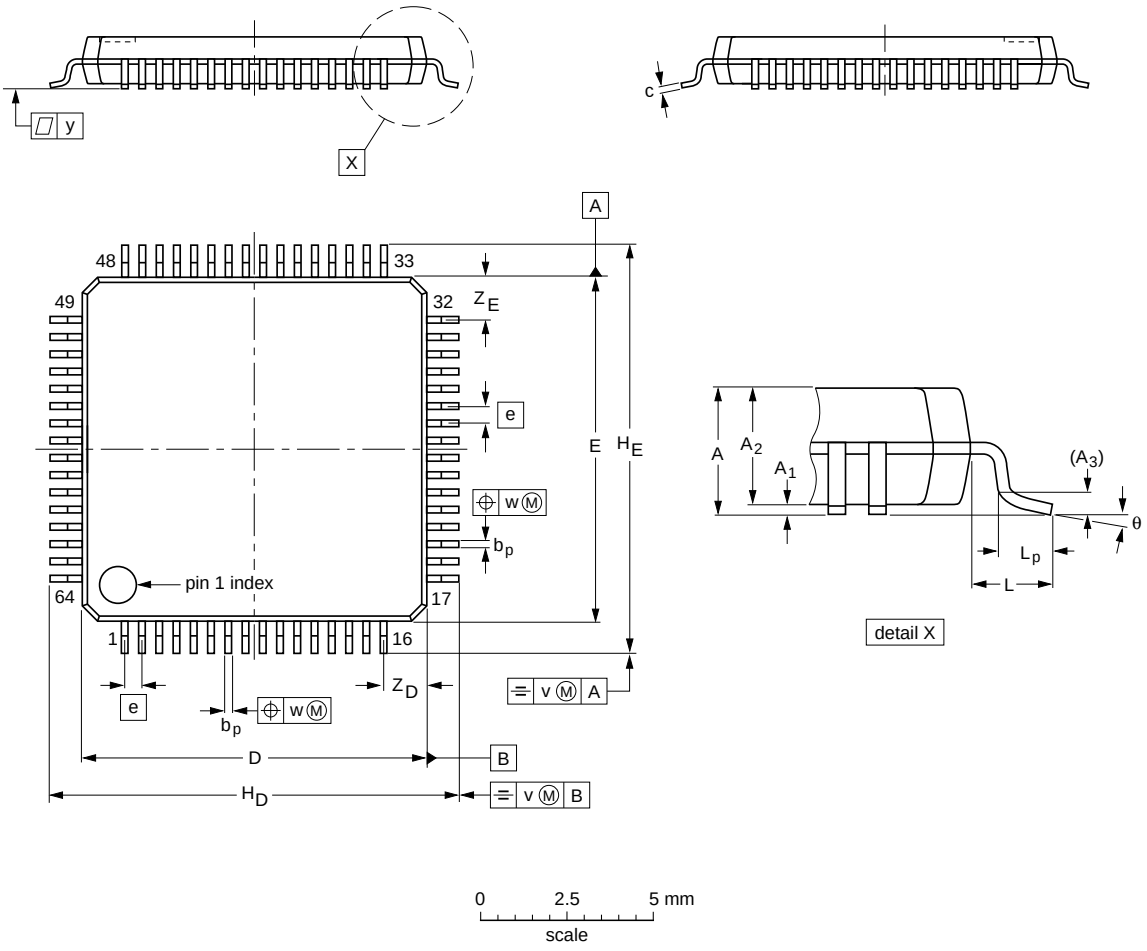
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 35. Package outline LQFP48 (SOT313-2)

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 36. Package outline LQFP64 (SOT314-2)

14. Soldering

Footprint information for reflow soldering of HVQFN33 package

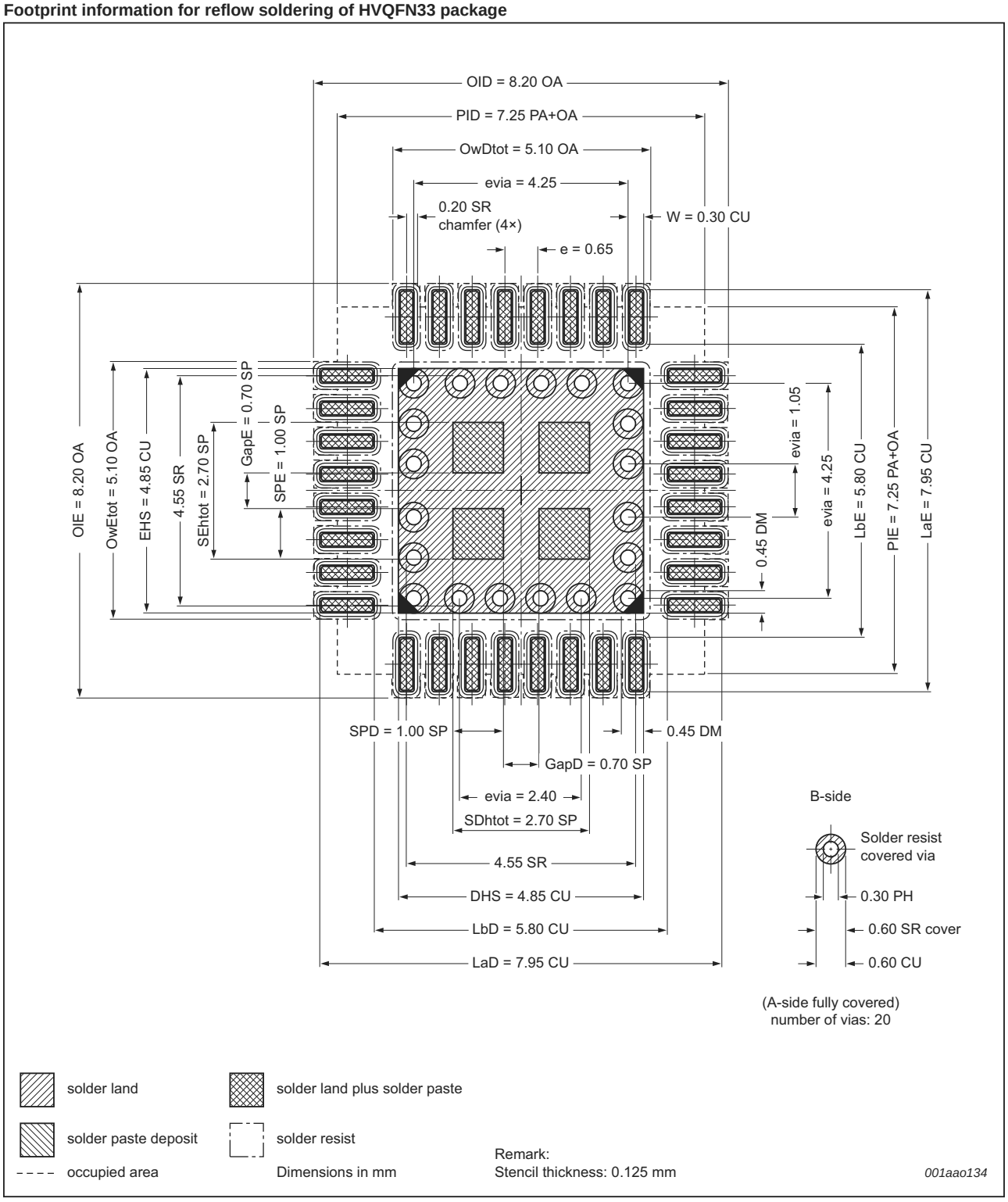


Fig 37. Reflow soldering of the HVQFN33 package

15. Abbreviations

Table 20. Abbreviations

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CDC	Communication Device Class
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
HID	Human Interface Device
JTAG	Joint Test Action Group
MSC	Mass Storage Class
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TAP	Test Access Port
USART	Universal Synchronous Asynchronous Receiver/Transmitter

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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